ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 3, March 2015

Design of Carry Select Adder for FIR Filter

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ABSTRACT: A fast and power efficient adder is always needed in electronic industry and is one of the vast area of research in VLSI system design. In this paper, design of two different Carry Select Adder (CSLA) are presented, one by using multiple pairs of RCA and another by using D-latch logic. Designing Carry Select Adder with RCA slightly increases the delay. To overcome this problem, CSLA is improved by replacing one of the RCA by D-latch. The performance of this CSLA is evaluated by implementing an FIR Filter by using CSLA in the adder part of filter. This work focuses on the performance of CSLA in terms of delay and power.

KEYWORDS: CSLA, RCA, D-Latch, FIR Filter, Low power and high speed.

I.INTRODUCTION

Adders are very important in variety of digital system. Many fast adder exits, but adding fast with low delay and power is still challenging. In many computers and other kind of processor adders are used not only in the arithmetic logic units, but also in other part of processor, where they are used to calculate addresses, table indices, and similar operations. On the basis of requirements such as area, delay and power consumption there are some complex adders such as Ripple Carry Adder, Carry look-Ahead Adder and Carry Select Adder. Ripple Carry Adder (RCA) shows the compact design but their computation time is longer. Applications that has time as a critical factor make use of Carry Look-Ahead Adder (CLA) to derive fast results but it leads to increase in area. But the carry select adder provides a compromise between the small areas but longer delay of RCA and large area with small delay of Carry Look Ahead adder.

The CSLA is used in many computational systems to improve the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. However, the CSLA is not area efficient because it uses multiple pairs of RCA to generate partial sum and carry by considering carry in 0 and carry in 1, then the final sum and carry are selected by the multiplexers (mux). Now a day an electronics industry focuses on high speed application with low power consumption. Battery life in portable electronic device is limited. Low power design leads to increase in battery life. If delay is less, application will work fast and ultimately power consumption is low. So, there is a need to work on delay.

II. LITERATURE SURVEY

Akhilash Tyagi introduced a scheme to generate carry bits with block carry in 1 from the carries of a block with block with block carry in 0.This scheme is then applied to carry select and parallel-prefix adders to derive a more area-efficient implementation for both the cases [1]. Chang and Hsiao proposed that instead of using dual RCA a CSLA scheme using an add one circuit to replace one RCA, here it reduces fewer transistors [2]. Yajuan He et al proposed an area efficient square root carry select adder scheme based on a new first zero detection logic. The proposed CSL witnesses a notable power-delay and area-delay performance improvement by virtue of proper exploitation of logic structure and circuit technique [3]. Padma Devi et al proposed modified CSLA designed in different stages which reduces the area [4]. Ramkumar and Harish propose BEC technique which is a simple and efficient gate level modification to significantly reduce the area and power of square root CSLA [5]. Sajesh Kumar U, Mohamed Salih K. and Sajith K propose carry select adder without using multiplexer which reduce area and power consumption. The Kogge Stone parallel approach will give option to generate fast carry for intermediate stages [6].

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III. REGULAR 16-BIT CARRY SELECT ADDER

Carry Select Adder is a logic element that computes (n+ 1) bit sum of two n-bit numbers. Carry Select Adder is high speed adder. The Carry Select Adder consists of two Ripple Carry Adder and multiplexer. Adding two n-bit number in carry select adder requires two Ripple Carry Adder in order to perform operation twice, one time with assuming carry equal to zero and other assuming one. After the two results are calculated the final sum as well as final carry is selected by multiplexers. The structure of 16-bit regular CSLA is shown in Fig. 1.

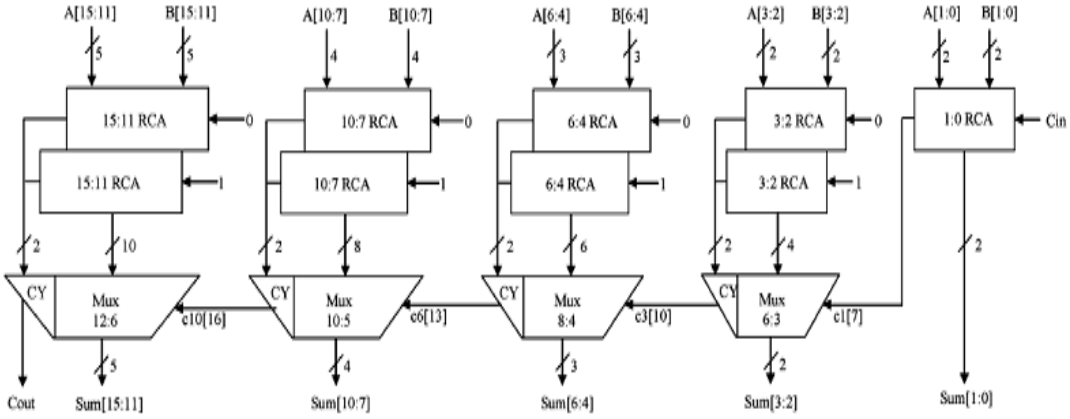

Fig. 1 16-bit regular Carry Select Adder

A Carry Select Adder has 5 groups of different size RCA. Each group consist of dual RCA and MUX. The upper RCA has carry-in of zero and lower RCA has carry-in of one. If cin =0, the sum and carry out of the upper RCA is selected. If cin=1, the sum and carry out of lower RCA is selected. The carry out calculated from the least significant bit stage i.e. last stage is used to select the actual values of the sum and carry out. The final selection is done by multiplexer. This adder has one disadvantage that is increase in delay. Ripple Carry Adder is constructed by cascading full adder, every full adder has to wait for the incoming carry before an outgoing carry is generated. The carry out of one stage is fed directly to the carry-in of the next stage. Delay increases with bit length.

IV. MODIFIED 16-BIT CARRY SELECT ADDER

Due to RCA there is slight increase in delay. So, we can modify the above structure in term of delay and power by replacing RCA with cin=1 by parallel structure of D-Latch. Latch is used to store one bit of information. When latch is enabled, outputs changes immediately according to inputs. If the data on D line changes its state, when enable is high then the output Q follows the input line D. When enable is low, the last stage of D-Latch input is trapped and held in latch. Fig. 2 shows a logic diagram of D-latch.

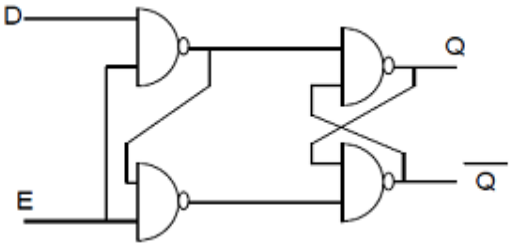

Fig. 2 D-Latch

An modified 16-bit Carry Select Adder is shown Fig. 3. This is a 16-bit adder in which least significant bit adder is RCA, which is 2 bit wide. The upper half of the adder i.e most significant bit is 14-bit wide which works according to

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the clock. Whenever clock goes high addition for carry input one is performed. When clock goes low addition for carry input zero is assumed and sum is stored in adder itself. The latch is used to store sum and carry for cin=1. Carry out from the previous stage i.e least significant bit adder is used as control signal for multiplexer to select final output carry and sum of the 16-bit adder. Cout is the output carry.

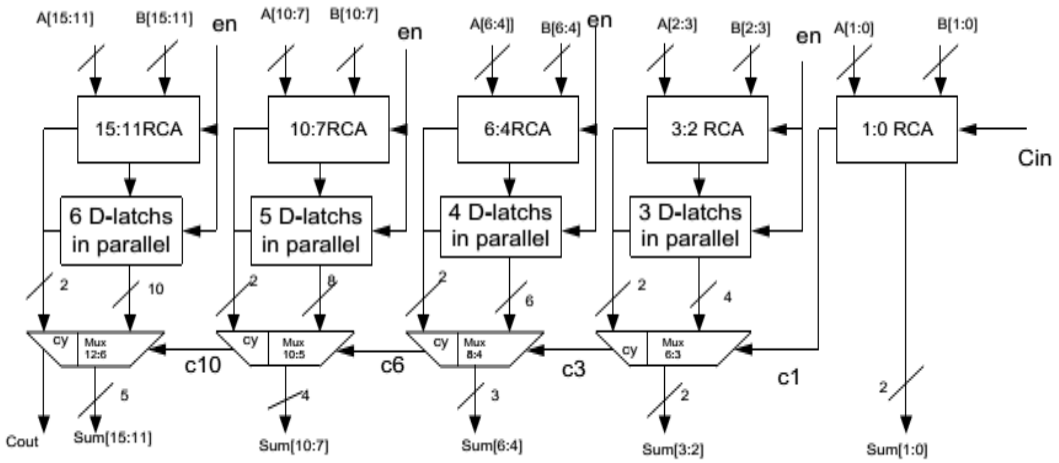

Fig. 3 16-bit modified Carry Select Adder

Initially when en=1, the output of RCA is fed as input to the D-Latch and the output of D-Latch follows the input and given as an input to the multiplexer. When en=0, the last state of D-Latch input is trapped and held in latch itself and therefore output from a RCA is fed directly as an input to the mux without any delay. Now the mux selects the sum bit according to the input carry which is the selection bit and the inputs of the mux are the outputs obtained when en=1 and en=0.

V. FIR FILTER IMPLEMENTATION USING CARRY SELECT ADDER

Adders are one of the widely used digital components in digital signal processing system. So there is need to design high speed adders. Direct form N-tap FIR filter consists of N delay elements, N multipliers and N-1 adders or accumulators as shown in Fig. 4. The impulse response of the FIR filter can be directly incidental from the tap coefficients b_k. The FIR Filter is implemented using both regular Carry Select Adder and modified Carry Select Adder and then comparing both the results in terms of delay and power.

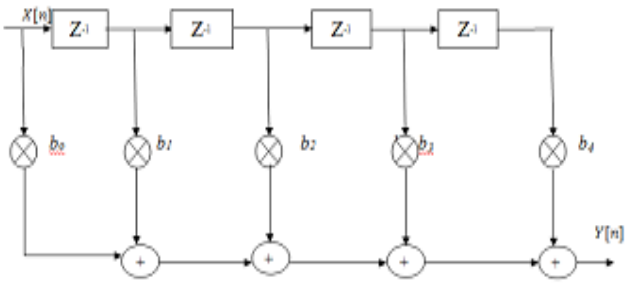

Fig. 4 FIR Filter

The adder part of FIR Filter is replaced with the regular and modified CSLA. Here we use a 4-tap FIR Filter implementation using regular and modified CSLA [9].

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VI. COMPARISON OF ADDERS FOR DELAY

The Fig.5 compares the adder circuit for delay comparison. When compare with regular CSLA, the modified CSLA gives less delay.

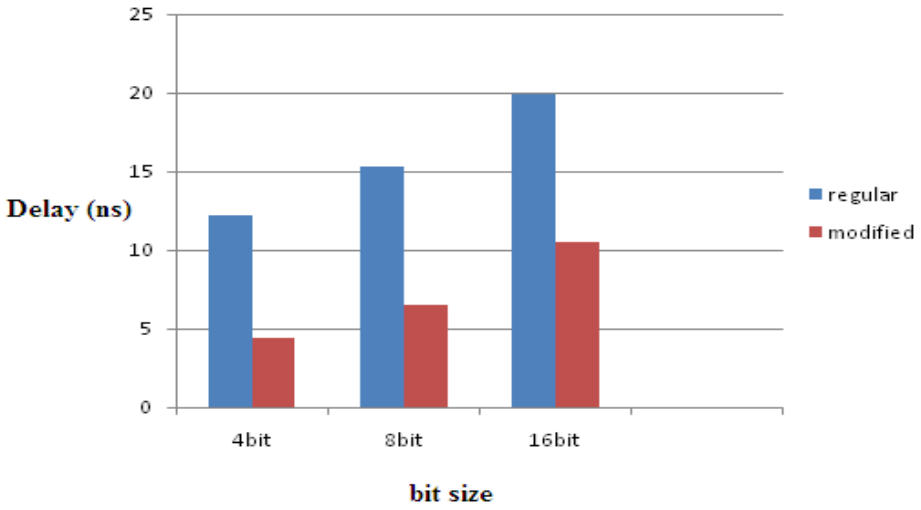

Fig. 5 Comparison of delay

It is clear from the comparison that the delay of 4-bit, 8-bit and 16-bit modified CSLA is decreased by 7.784ns, 8.734ns and 9.389ns respectively when compared to regular CSLA. Realization of less delay depicted that the modified CSLA consumes less power than regular CSLA. The modified CSLA overweigh than regular CSLA in term of delay and power.

VII.CONCLUSION

This paper presents an unique approach in increasing the performance of carry select adder by reducing delay and power. A regular CSLA uses two copies of the RCA, one with block carry input is one and other with block carry input is zero. Regular CSLA suffers from delay problem due to the cascading structure of RCA. Therefore, modified CSLA is proposes using D-Latch which perform two operation in one clock cycle without any delay.

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