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Designing of Low Power Dual Edge - Triggered Static D Flip-Flop with DETFF Logic

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ABSTRACT: The normal D flipflop consumes very high power. So in this paper we enumerates new architecture of low power dual-edge triggered Flip-Flop (DETFF) designed at 90nm CMOS technology. In DETFF same data throughput can be achieved with half of the clock frequency as compared to static output-controlled discharge Flip–Flop (SCDFF). SCDFF involves an explicit pulse generator and a latch that captures the pulse signal. The latch structure of SCDFF consists of two static stages. In the first stage, input D is used to drive the pre charge transistor so that node follows D during the sampling period. In this paper conventional and proposed DETFF are presented and compared at same simulation conditions. Therefore the proposed DETFF design is suitable for low power and small area applications.

KEYWORDS: Dual-Edge Triggered, Flip-Flop, High Speed, Low Power, Static D Flip-Flop

I. INTRODUCTION

The latest advancement in computing technology is to set a goal of high performance with low power consumption for VLSI designer . Flip-Flops are important timing elements in digital circuits which have a great effect on circuit power consumption and speed. The performance of the Flip-Flop is an important element to determine the performance of the whole circuit, particularly in deeper pipelined design . For improving the performance one innovating approach is to increase the clock frequency. However, using high clock frequency, there are many disadvantages. Power consumption of the clock system increases and clock uncertainties take significant part of the clock cycle at high frequencies. Moreover the non-ideal clock distribution results in degradation of the clock, and produce power supply noise and crosstalk About 30%-70% of the total power in the system is dissipated due to clocking network, and the Flip-Flops . An alternative clocking approach is based on the use of storage elements which are capable of capturing data on both rising and falling edges. Such storage elements are termed as Dual-Edge Triggered Flip-Flops (DETFFs). In this, same data throughput can be achieved at half of the clock frequency as compared to single edge triggered Flip-Flops. We can also say that double edge clocking can be used to save half of the power in the clock distribution network. The average power in a CMOS circuits is given by the following equation:

Pavg = pt(CLV*Vdd* fclk) + Isc*Vdd + I leakage*Vdd

The above equation represents the three major sources of power dissipation in CMOS VLSI circuits. The first term represents the dynamic power dissipation. The second term indicates the direct path short circuit power dissipation. The third term indicates leakage power**.** In most cases, the voltage swing V is the same as the supply voltage Vdd. Dynamic power is proportional to the square of the supply voltage, contributes highest power consumption among the three. Therefore reducing the supply is the most effective way to reduce power consumption of the design. However it decreases the speed of designed circuit. Reduction in clock frequency is another alternative to reduce the dynamic power dissipation. Double edge clocking approach is adapted in this paper, to reduce the clock frequency. In this approach same data throughput can be achieved with half of the clock frequency as compared to SEDNIFF.
The paper is organized as follows-
Section 2 explains the conventional DETFF circuits and a new proposed architecture of DETFF.

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Section 3 contains the nominal simulation conditions, along with analysis and optimization performed, during simulation. Section 4 contains performance results for proposed design. These results are compared with conventional designs in terms of delay, power, PDP and area and Section 5 ends with conclusion.

II. FLIP FLOP STRUCTURES

In some of the designs DETFF approach is preferred to reduce power dissipation . Unlike SCDFF, data is captured by both edges of the clock. Implementation of DETFF is shown in fig.1

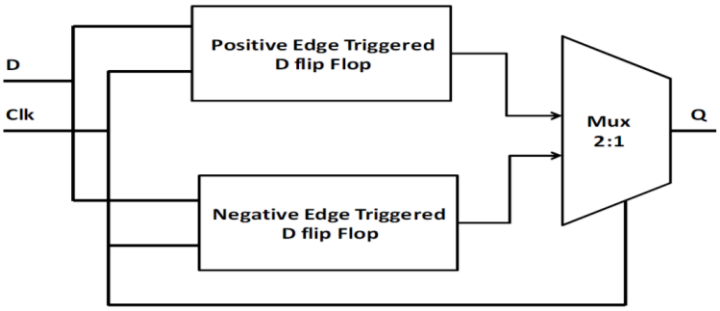

Fig 1 - Dual-edge-triggered Flip-Flops

Both positive and negative edges are used to sample the D input at alternate clock edges, and the appropriate sample is selected for the Q output by a clocked multiplexer (MUX).

A. Conventional Dual-Edge Triggered Flip-Flops

M.W.Phyu et.al, proposed a static output-controlled discharge Flip–Flop (SCDFF) . SCDFF is implemented by Cross-coupled inverters to keep the data at output Q. However, race problem is there in the cross-coupled inverters, which not only degrades the speed of charging and discharging, It also causes short-circuit power dissipation. The duration of the race current will be prolonged if the output load capacitance is large, which distort the desired output signal and also increases the dynamic power dissipation.

Xue-Xiang Wu et.al, proposed a static explicit-pulsed dual edge triggered Flip-Flop with latch node built-in (SEDNIFF) [8]. In SEDNIFF, a pulse generator circuit is used to generate narrow pulses at both rising and falling edges of the clock as shown in Fig 2.

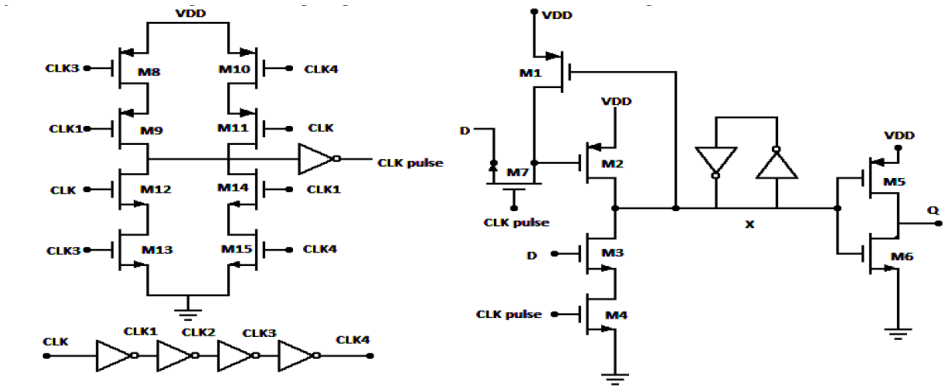

Fig 2- SEDNIFF circuit

In SEDNIFF the charge paths, from VDD to CLK-pulse are OFF when the discharge paths, from CLK-pulse to ground are ON and vice versa, which leads to reduction in short-circuit power dissipation. However because of large number of clocked transistors present in the clock generator circuit the overall power dissipation of the design is more.

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B. Proposed Dual-Edge Triggered Flip-Flop

In the proposed DETFF, positive latch and negative latch are connected in parallel as shown in Fig 3. These latches are designed using one transmission gates and two inverters connected back to back and the output of both the latches are connected to 2 to 1Mux as input. Mux is designed using 2T pass transistor logic, one PMOS and one NMOS connected in series and gates are connected together and derived by the inverted CLK. Output of Mux is connected to the inverter for strengthening the output. Back to back connected inverters hold the data when transmission gate is *OFF* and at the same time Mux sends the latched data to the inverter to get the correct D at the output.

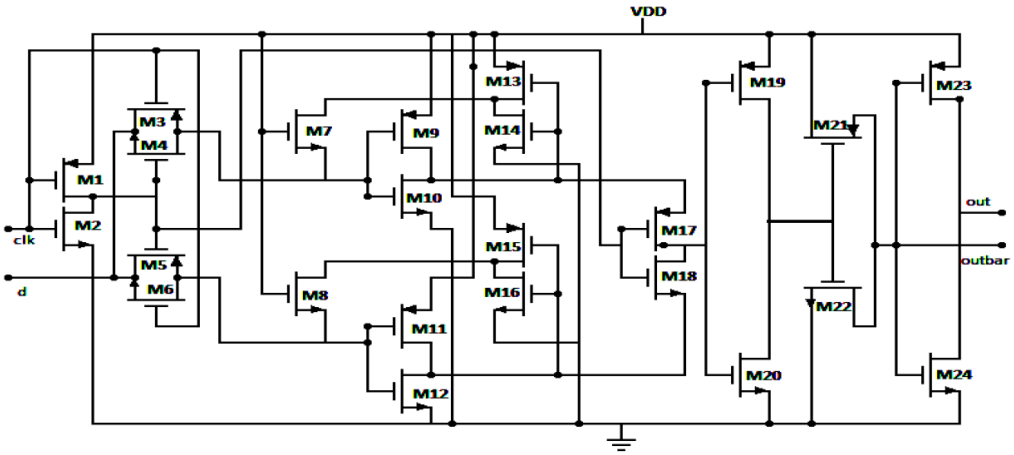

Fig 3 - Proposed DETFF Circuit

The proposed DETFF works as follows. When the CLK is low M3, M4 and M18 are ON and M5, M6 and M17 are OFF. Hence data hold by negative latch is transparent to Q. When CLK is high M5, M6 and M17 are ON and M3, M4 and M18 are OFF. If input D remains the same, Q also remains unchanged. On the other hand, if D is changed before the CLK then D will be hold by positive latch and the same value will be send to the output when CLK changes from Low to high and similarly for the transition of CLK from high to low.

III. SIMULATIONS

For a fair comparison each circuit is simulated at the layout level on same simulation parameters.
The layout of proposed DETFF shown in Fig 4 is designed using microwind tool.

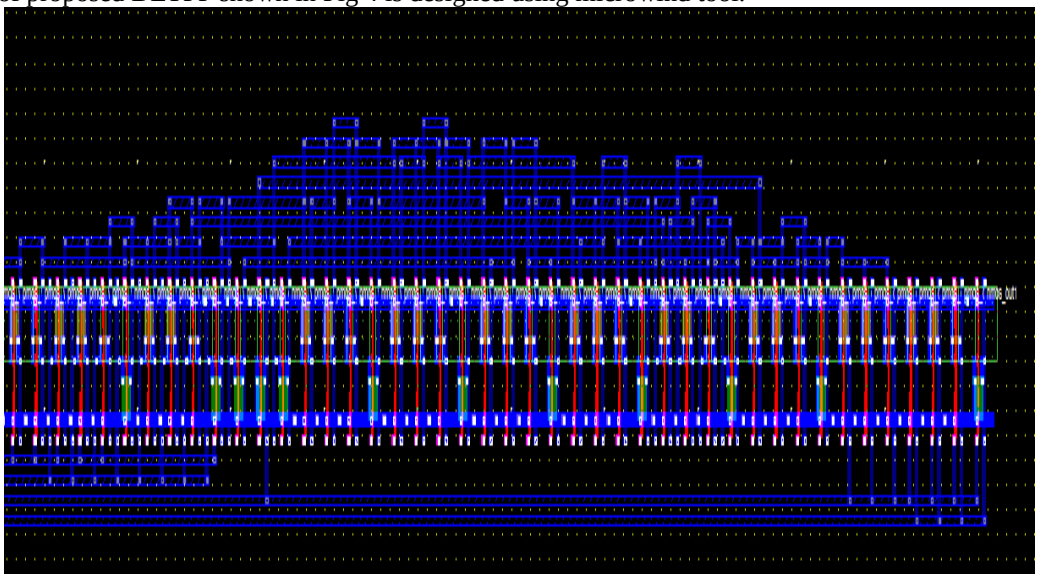

Fig.4 layout design of DETFF

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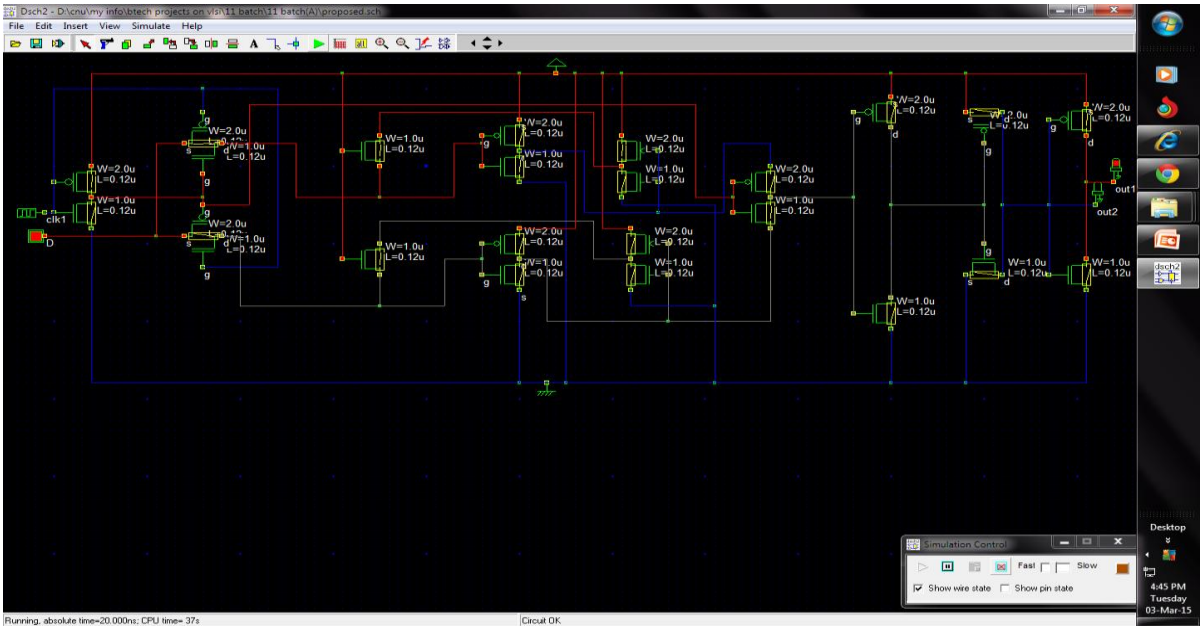

Fig. 5 Result verification

Fig .5 shows the simulated diagram of DETFF. After the execution the circuit transfers the value on D to Output. Fig. 6 shows the resultant waveforms, represent the working the D flip flop.

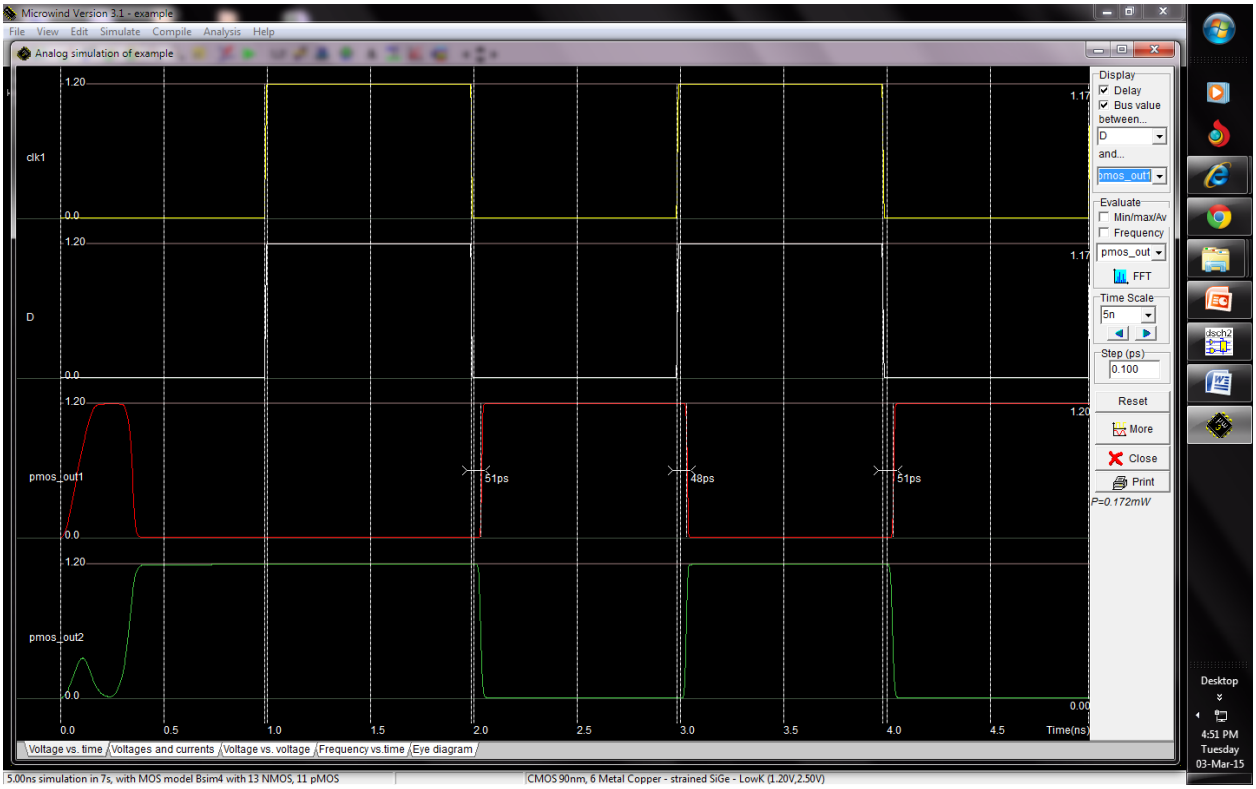

Fig. 6 Resultant Waveforms

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Simulation parameters used for comparison are shown in Table I.

Method	Area(in μm^2)	Power(in µw)	Delay(in ps)	Critical delay(in ns)
SEDNIFF	520	60.058	92	1.82
Proposed DETFF	765	34.739	44	2.45
CMOSDFF	860	57	119	3.5

Table I comparision of power dissipation and delay using three different techniques.

IV. EXPERIMENTAL RESULTS COMPARISON

The proposed DETFF is designed and compared with SEDNIFF and CMOS D flip flop.. Each Flip- Flop is optimized for power delay product. The proposed DETFF is having lesser number of clocked transistors than the other techniques. Simulation results for power, delay, critical delay and area at nominal conditions for the Flip-Flops are summarized in Table II.

V. CONCLUSION

In this paper, we proposed a low power, small area DETFF design which is static in nature. The proposed DETFF has lesser number of clocked transistors with respect to other techniques. The post layout experimental simulation results shows that proposed DETFF offers improvement in power dissipation, delay and area. Therefore the proposed DETFF is suited for low power and small area applications.

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