ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 3, March 2015

Design the 2X1 MUX with 2T Logic and Comparing the Power Dissipation and Area with Different Logics

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ABSTRACT: In decoders available multiplexer-based decoder requires less hardware, has more regular structure and shorter critical path. A 2-to-1 multiplexer is the leaf cell in the decoder. In this paper a 2-to-1 multiplexer circuit using complementary CMOS, dynamic and pass- ransistor logic styles have been analyzed. The power consumption, delay, area and power-delay product of various logic styles are compared. This paper shows that 2T multiplexer is an optimum device level design which has characteristics of high speed with minimum power compared with other realizations.

KEYWORDS: Thermometer code, Flash ADC, CPL, EEPL, LEAP.

I. INTRODUCTION

Among them multiplexer-based decoder has regular structure requires less hardware and has a shorter critical path than any other decoder and gives bubble error suppression. It consists entirely of 2-to-1 multiplexers. Multiplexing is the generic term used to describe the operation of sending one or more analogue or digital signals over a common transmission line at different times or speeds and as such, the device we use to do just that is called a **Multiplexer**. The *multiplexer*, shortened to "MUX" or "MPX", is a combinational logic circuit designed to switch one of several input lines through to a single common output line by the application of a control signal. In electronics, a multiplexer (or mux) is a device that selects one of several analog or digital input signals and forwards the selected input into a single line. A multiplexer of 2^n inputs has n select lines, which are used to select which input line to send to the output. Multiplexers are mainly used to increase the amount of data that can be sent over the network within a certain amount of time and bandwidth. A multiplexer is also called a data selector. An electronic multiplexer can be considered as a multiple-input, single-output switch. The schematic symbol for a multiplexer is an isosceles trapezoid with the longer parallel side containing the input pins and the short parallel side containing the output pin. Thus this paper analyzes 2-to-1 multiplexer using complementary CMOS, dynamic and pass-transistor logic styles. These implementations are compared based on transistor power dissipation and area. The rest of the paper is organized as follows: In section II, we present the architecture of multiplexer and basic idea of a 2-to-1 multiplexer. Section III gives the design of 2-to-1 multiplexer using complementary CMOS, dynamic and pass-transistor logic style. Results of quantitative comparisons based on simulations of different logic styles are given in section IV. Some conclusions are drawn in section V.

II.ARCHITECTURE OF MULTIPLEXERCIRCUIT

A circuit that generates an output that exactly reflects state of one of a number of data inputs, based on value of one or more control inputs is called as "multiplexer". A multiplexer with two data inputs and one control line is referred as "2-to-1 or 2:1" multiplexer. Commonly used circuit and graphical symbol for 2 to 1 multiplexer is shown in Fig.1 & Fig.2 respectively. Circuit and Graphical symbol of 2:1 Multiplexer Logic expression for multiplexer output is given below.

$$F = \hat{S}\, x1 + S\, x2 \quad (1)$$

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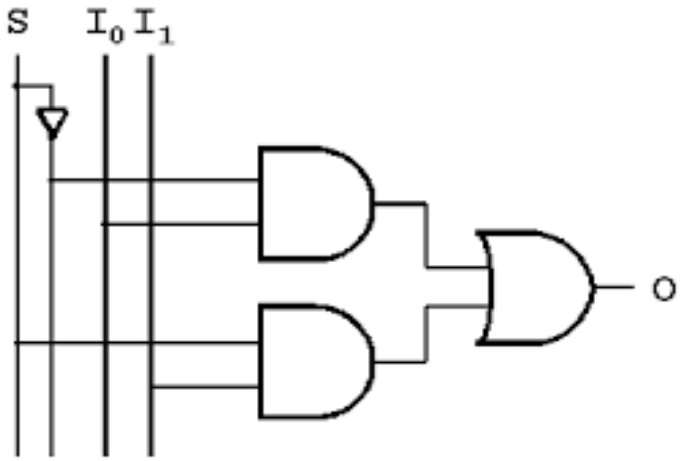

Fig 1 cicuit of 2:1 multiplexer

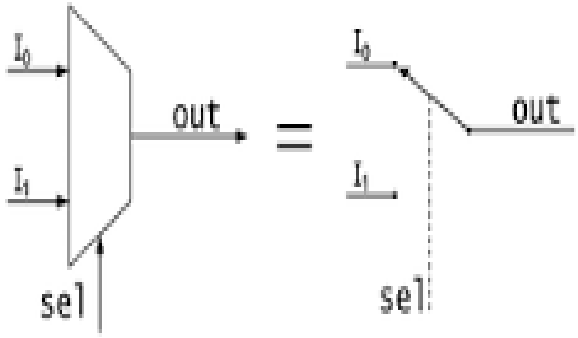

fig 2 symbol of 2:1 multiplexer

III. LOGIC STYLES

A logic style is the way how a logic function is constructed from the transistors. It influences the speed, area occupied, power dissipation and wiring complexity of a circuit. All these characteristics may vary considerably from one logic style to another style and thus make the proper choice of logic style crucial for circuit performance.

A. Complementary CMOS Logic style: Any logic function in complementary CMOS is realized by NMOS pull-down and PMOS pull-up networks connected between gate, output and power lines . Input signals are connected to transistor

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gates only. Pseudo nMOS and Cascade Voltage Switch Logic (CVSL) fall under CMOS rationed logic family.

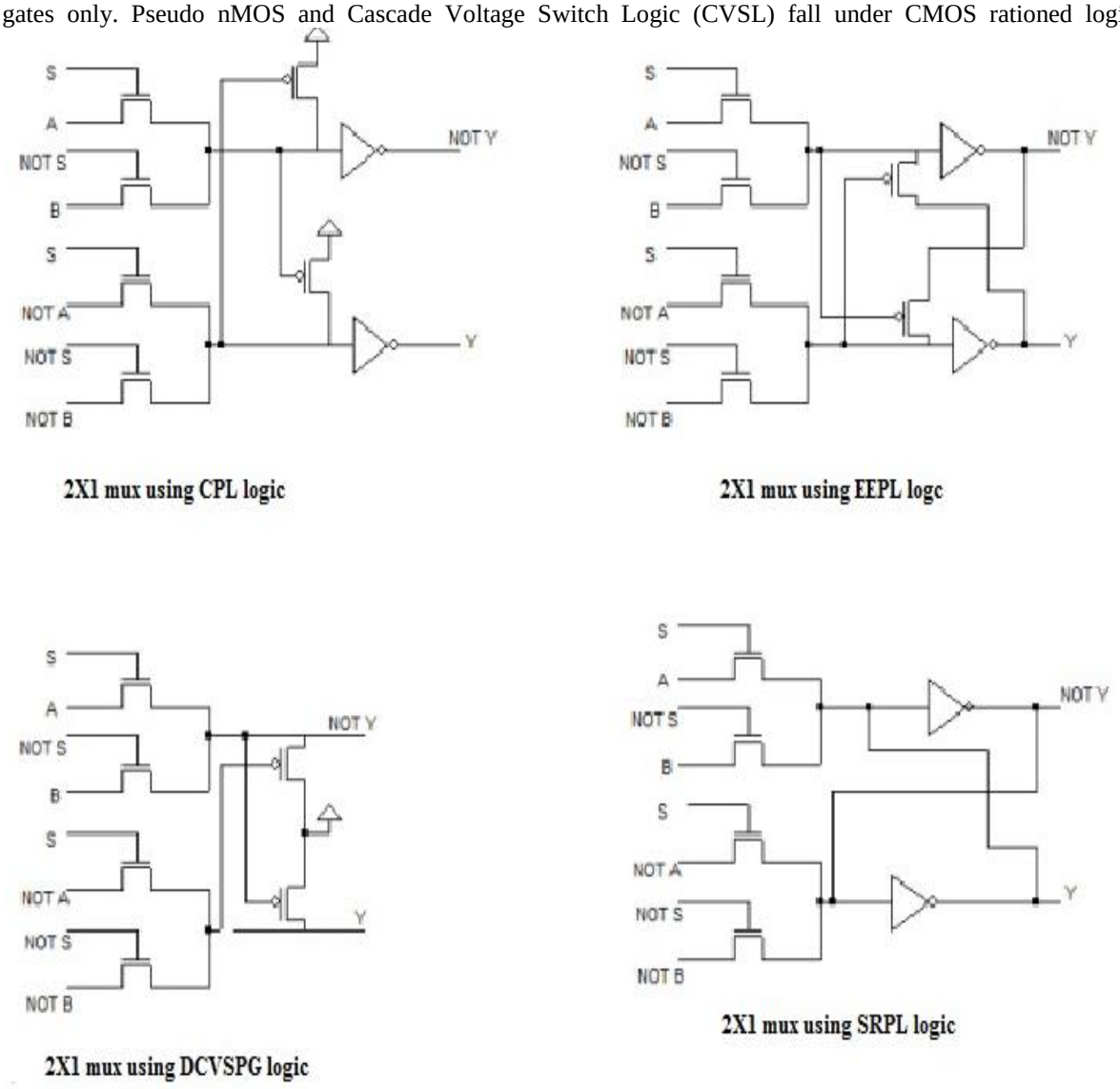

Fig 3 different techniques to construct the 2X1 mux

B. Dynamic Logic style: The operation of dynamic logic is based on storage of charge on capacitive node [6]. These are fastest, have zero static power dissipation and are sensitive to noise. Domino logic and Dual rail Domino fall under this category.

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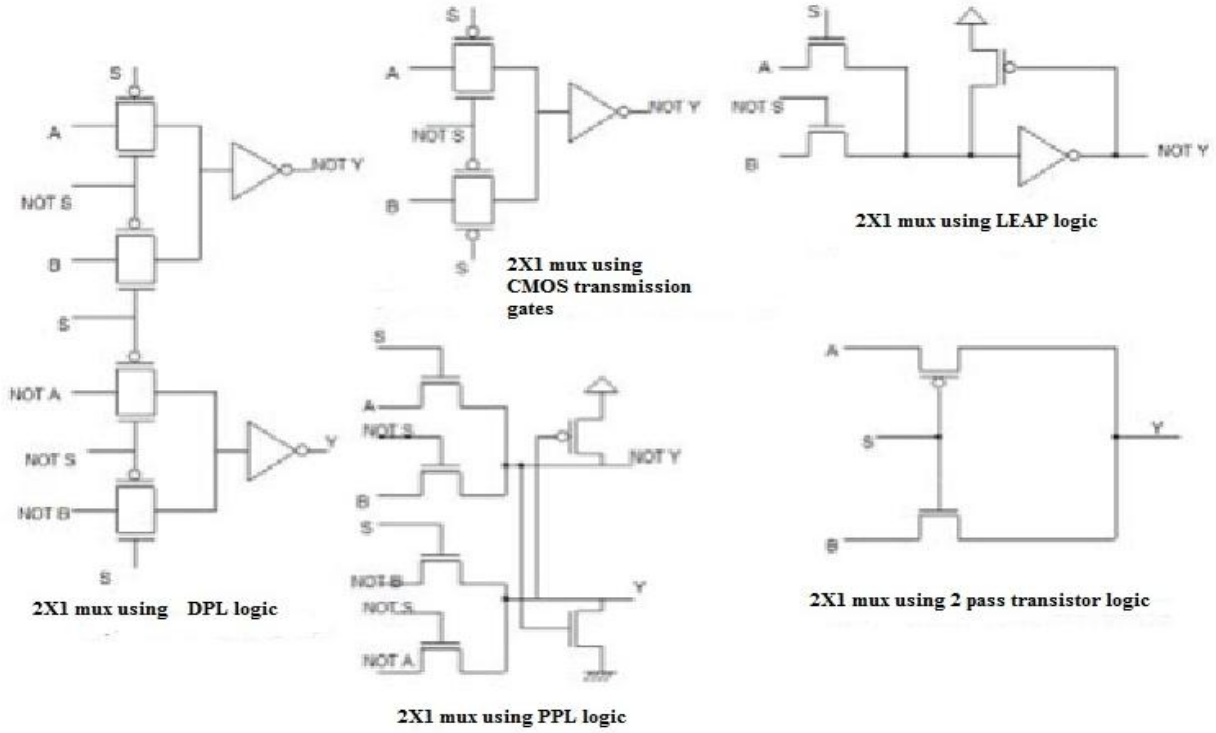

Fig 4 different techniques to construct the 2X1 mux

C. Pass-transistor Logic style: The pass-transistor logic reduces the number of transistors required, by allowing the primary inputs to drive gate terminals as well as source-drain terminals. The advantage is that one pass-transistor network (either NMOS or PMOS) is sufficient to perform the logic operation. Mostly we are choosing NMOS transistor for construction. Several pass-transistor logic styles Complementary Pass Transistor Logic (CPL)[6], Energy Economized Pass Transistor Logic (EEPL), Differential Cascode Voltage Switch logic with Pass gate (DCVSPG), Swing restored pass-transistor logic (SRPL)[6], Double pass-transistor logic (DPL), CMOS Transmission gate, Push-pull Pass Transistor Logic (PPL), LEAN Integrated pass gate logic (LEAP) and 2T Multiplexer are considered to implement 2-to-1 multiplexer. Among all these 2T Multiplexer is optimal. It uses one pMOS and one nMOS transistor and these two-pass transistors at the input select which signal to propagate. The logic levels will be deteriorated by the pass transistor. The threshold voltage of both pass-transistors should be identical for accurate operation.Fig.3 represents implementation of 2-to-1 multiplexer using several logic styles.

IV. SIMULATION & RESULT ANALYSIS

All the simulations have been done using Microwind tool. All the schematics are drawn using 0.9-µm technology with a 1.8V supply voltage. The calculation of power , delay and power-delay product are carried out for 2-to-1 multiplexer in Static CMOS , CVSL, 2TMux (pass transistors), CMOS transmission gate, CPL, DCVSPG, DPL, EEPL, PPL, SRPL and LEAP logic styles. To establish an impartial testing environment, simulations have been carried out using a comprehensive input signal pattern which covers every transition possible for a multiplexer. The simulation results of 2T mux is shown fig 5 & 6. Fig. 5 shows the simulation result of 2T mux. It shows the result that when s=0 & D=1 and o/p = 1. Thus we can verify the all 2^n possible conditions. Fig. 6 shows the waveforms of the result. Fig. 7 shows the layout diagram generated by tool. Fig. 8 shows the graph by which we can compare the power dissipation and area. For example 2T occupies the less are and consume less power. Next SRPL occupies the less area and consumes moderate power. But static CMOS occupies the more area. The CVSL and PPL logics consume more power when compared to other logics. Thus the 2T is the best with respect to area and power consumption. So in Dual edge triggered flip flops and other circuits, if mux is required and it can be implemented with 2T technique.

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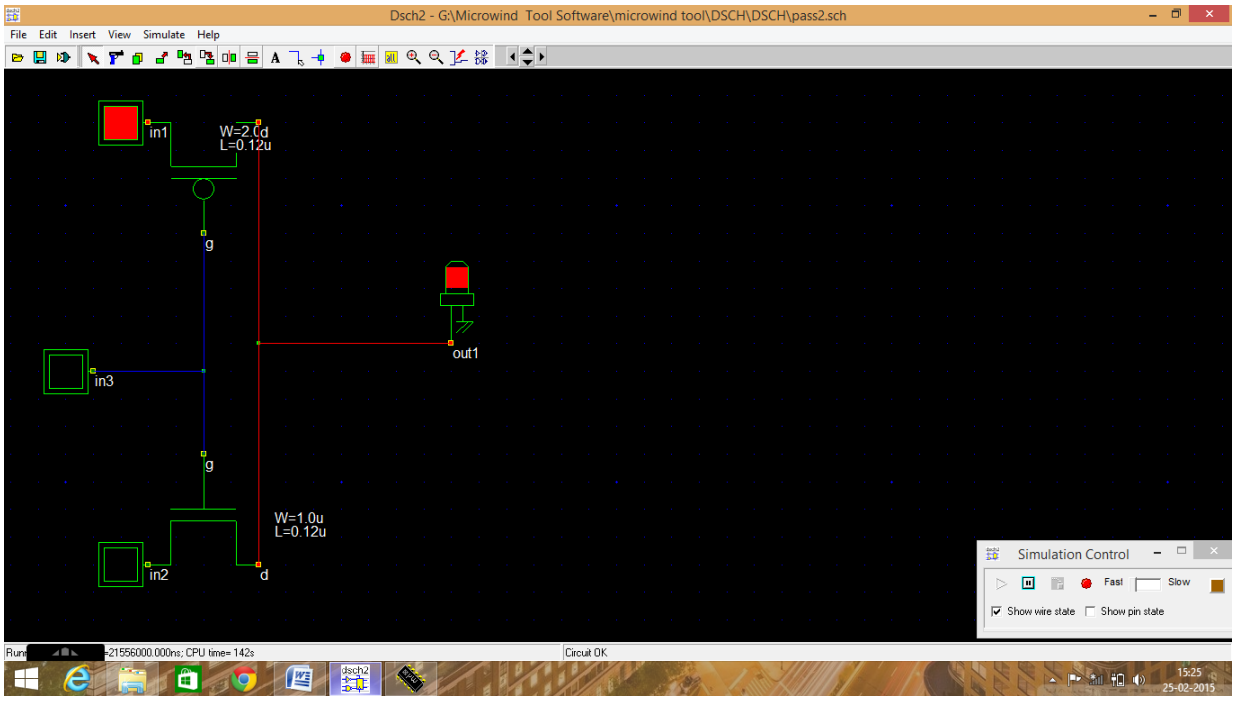

Fig.5 2T mux construction and verification of result

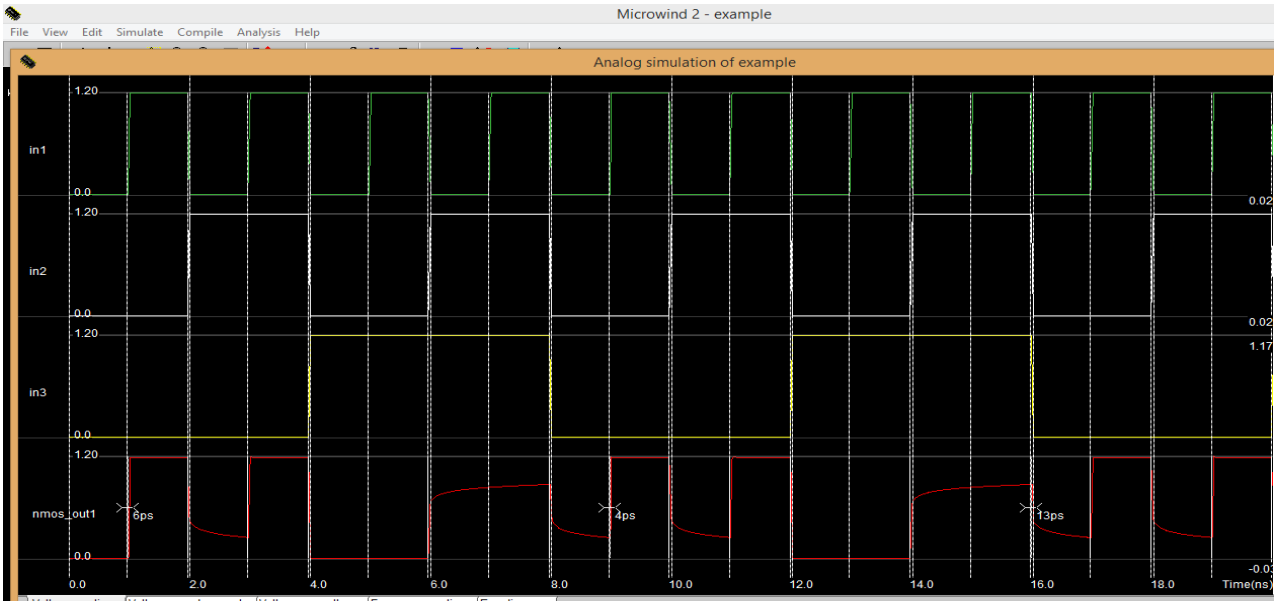

Fig. 6 Waveform of the result

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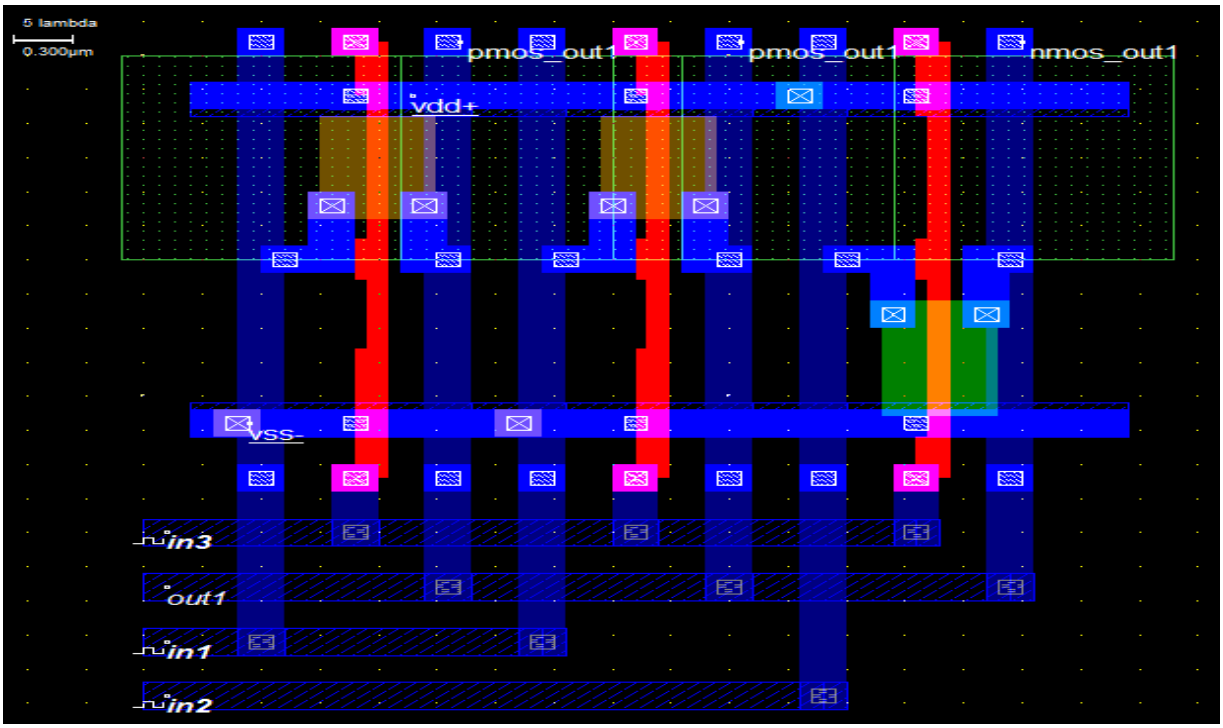

Fig. 7 layout of 2T mux

Logic Style	Area(in µm²)	Power Dissipation(in µw)
Static CMOS	147	4.298
CVSL	140	255
CPL	160	10.327
EEPL	136	8.442
DCVSPG	136	4.153
SRPL	77	9.020
DPL	120	4.439
CMOS TG	120	0.938
PPL	105	107
LEAP	105	431
2T MUX	24	0.159

Table 1 the comparison of different techniques w.r.t area and power dissipation

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Fig. 8 Comparison chart of different techniques

V.CONCLUSION

Static CMOS performs much better than pass-transistor logic styles if low power is of concerned. Pass-transistor logic has proved to be an attractive alternative to static CMOS design with respect to area, performance and power consumption. Among all pass-transistor logic styles considered 2T multiplexer is having few transistor counts. The advantage of having the same functionality with very few transistors and of small input capacitance in 2T pass-transistor logic will be beneficial in multiplexer realization for decoders. The pass transistor has loss of logic level but can be compensated by using buffers at intermediate places in decoder stages. Thus 2T multiplexer is suitable for multiplexer-based decoder implementation which is characterized by high speed with minimum power compared with all other realizations. As shown in table 1 , it occupies less area and consumes less power. The comparison chart is shown in fig. 8

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