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Power Flow Control of Photovoltaic Power Generation System Using Five-Level Inverter

Kondreddy Harshitha[1], T. Suneel Kumar[2]

PG Student [EPS], Dept. of EEE, Sree Vidyanikethan Engineering College, Tirupati, Andhra Pradesh, India[1]

Assistant Professor, Dept. of EEE, Sree Vidyanikethan Engineering College, Tirupati, Andhra Pradesh, India[2]

ABSTRACT: Generally, the output from the PV array is a DC power so, an inverter is necessary to inject that power into the grid. In this paper, a five-level inverter with dual-buck topology is used. The dual-buck converter converts the DC power into three DC voltage levels i.e., $0,V_{dc}/2,V_{dc}$. Due to this conversion, the number of switches used in five-level inverter is reduced. Further, the three level DC voltage is converted into five-level AC voltage with the help of full-bridge inverter. As a result, the switching losses and harmonic distortions are reduced. A Boost converter is used to boost the output voltage of solar array. The switching control of IGBT of boost converter is obtained by perturb and observe method. This entire module is developed in SIMULINK.

KEYWORDS: Inverter, Switching losses, harmonic distortions, Perturb and observe method.

I.INTRODUCTION

The renewable energy generation has been assuming increasing significance now-a-days because of the growing concern towards country's energy security. Day-by-day the energy scenario is changing. so, an intensified research on renewable energy generation has lead to the emergence of various methods involving energy resources like solar, wind etc., basically, all kinds of energy on earth originate in solar energy. so it is possible to use solar energy for various applications. the solar PV contributes 4.59% of the renewable energy installed capacity in India[1]

However, the renewable energy sources needs the power electronic interface to the utility grid because of various power conversions being involved between the sources and the grid. An inverter plays a major role for this power conversion. The multilevel inverters presents great advantage when compared to two-level inverters. These advantages are fundamentally focused for the improvement of output signal quality. As the number of levels increases, the THD of the inverter output remains less when compared to two-level inverters.

while considering all these advantages, the multilevel inverters also have some limitations. The converter control is complex when compared to conventional inverter topologies. Balancing of DC capacitor voltages, high switching losses etc., remains a serious issue[2].
The predominantly used multilevel inverter topologies are the neutral point clamped (NPC)type, flying capacitor (FC)type, cascaded H-bridge (CHB) type. these different types of inverters has been successfully commercialized for very high power and power quality demanding applications at various power ratings.
This paper reveals the working and simulation of a new five-level inverter topology which proves to overcome some of the limitations of conventional multilevel topologies.

II.PROPOSED TOPOLOGY

The proposed single phase five-level inverter is developed to transfer power that is obtained from solar PV to grid with the series connection of components like DC-DC Boost converter, two DC capacitors, dual-buck converter, full-bridge inverter and a filter. The PV arrays are connected to the inverter via a DC-DC Boost converter which performs the functions of maximum power point tracking(MPPT) and boosting the output voltage of the solar cell array. The five-level inverter is configured by two DC capacitors, a dual-buck converter and a full-bridge inverter. The two DC capacitors perform as energy buffers between the DC-DC converter and the five-level inverter. The dual-buck converter is configured by two buck converters through which the voltage balancing between the two DC capacitors is

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done and converts into a DC output voltage with three levels. Finally, the output of the dual-buck converter is connected to the full-bridge inverter to convert the three-level DC voltage into five-level AC voltage[3]. Fig. 1 shows the circuit configuration of the five-level inverter applied to a photovoltaic power generation system.

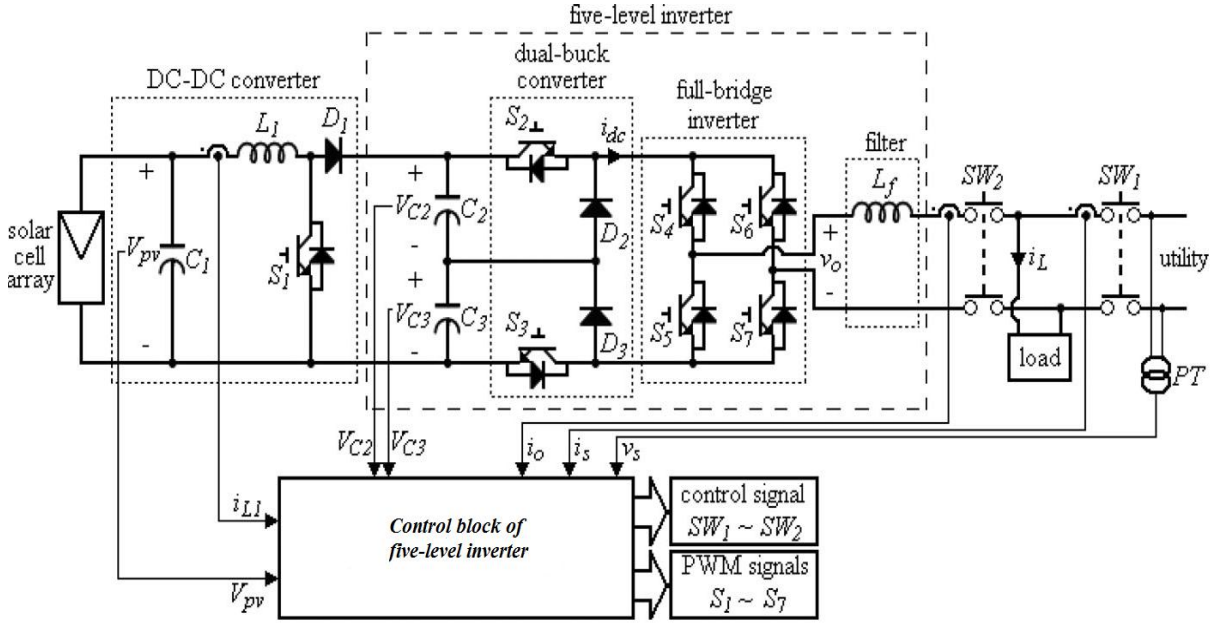

Fig. 1 circuit configuration of photo voltaic power generation system of five level inverter with dual-buck converter topology

III. OPERATING PRINCIPLE

The operation of the five-level inverter is categorized into eight modes. The modes 1-4 are for positive half cycle and the other modes 5-8 are for the negative half cycle. Fig. 2 shows the operating modes of five-level inverter. The power electronic switches i.e., IGBT's of the full-bridge inverter are switched in low frequency and is synchronous with the utility voltage to convert the DC power into AC power. As seen in Fig. 2(a)-(d), the power electronic switches S_4 and S_7 are in ON state, and the corresponding S_5 and S_6 are in OFF state. Similarly, the power electronic switches S_4 and S_7 are in OFF state and the necessary S_5 and S_6 are in ON state for negative half-cycle. The DC capacitor voltages V_{C2} and V_{C3} are balanced by controlling the five-level inverter as explained above. The DC capacitor voltages V_{C2} and V_{C3} can be represented as follows:

$$V_{c2} = V_{c3} = \frac{1}{2} V_{dc} \tag{1}$$

The modes of operation of the five-level inverter are stated follows.

Mode 1: Fig. 2(a) shows the circuit operation of mode 1. The power electronic switch of the dual-buck converter S_2 is turned ON and S_3 is turned OFF. The DC capacitor C_2 is discharged through S_2, S_4, the filter inductor, the utility, S_7 and D_3 to form a loop. The output voltage values of dual-buck converter and five-level inverter are $V_{dc}/2$.

Mode 2: Fig. 2(b) shows the circuit operation of mode 2. The power electronic switch of the dual-buck converter S_2 is turned OFF and S_3 is turned ON. The DC capacitor C_3 is discharged through D_2, S_4, the filter inductor, the utility, S_7 and S_3 to form a loop. The output voltage values of dual-buck converter and five-level inverter are $V_{dc}/2$.

Mode 3: Fig. 2(c) shows the circuit operation of mode 3. The power electronic switches S_2 and S_3 of the dual-buck converter are turned OFF. The stored current in the filter inductor flows through the utility, S_7, D_3, D_2 and S_4. The output voltage values of dual-buck converter and five-level inverter are zero.

Mode 4: Fig. 2(d) shows the circuit operation of mode 4. The power electronic switches S_2 and S_3 of the dual-buck converter are turned ON. The DC capacitors C_2 and C_3 are discharged together through S_2, S_4, the filter inductor, the utility, S_7 and S_3 to form a loop. The output voltage values of dual-buck converter and five-level inverter are V_{dc}.

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The same process repeats for negative half cycle with modes 5-8. Here, the power electronic switches S_4 and S_7 are in OFF state and corresponding S_5 and S_6 switches are in ON state.

By considering these operating modes 1-8, the full-bridge inverter converts the DC output voltage of the dual-buck converter with three levels to an AC output voltage with five levels which are V_{dc}, $V_{dc}/2$, 0, $-V_{dc}/2$ and $-V_{dc}$.

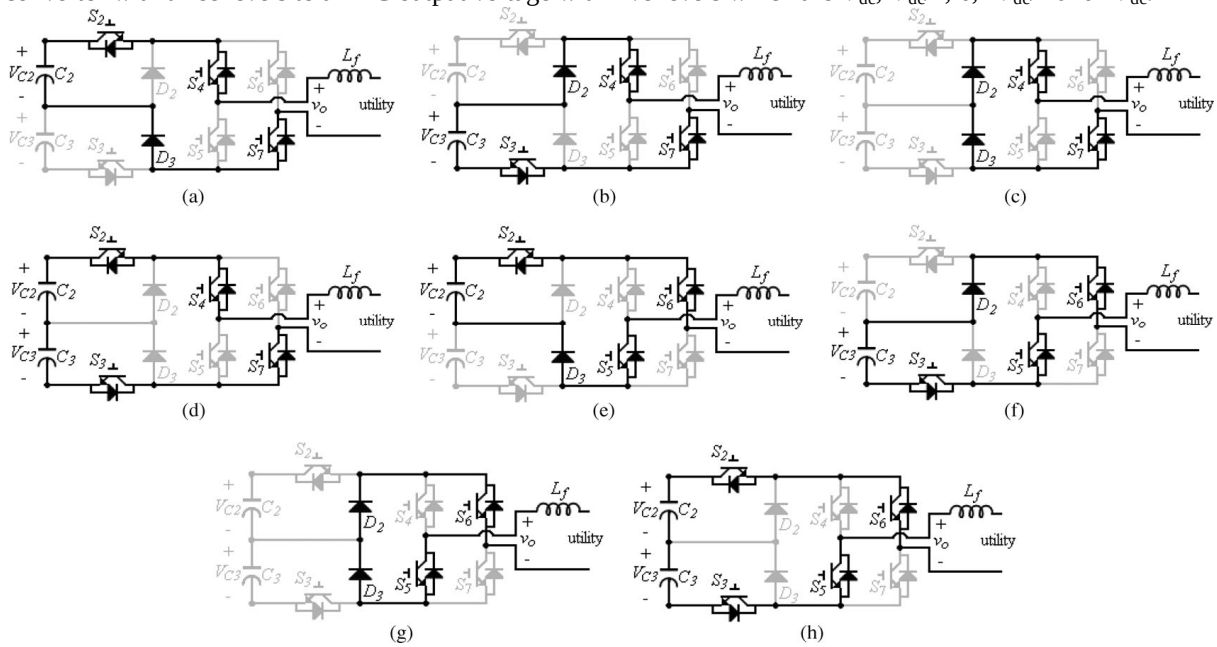

Fig. 2 Operation modes of the five-level inverter. (a) Mode 1 (b) Mode 2 (c) Mode 3 (d) Mode 4. (e) Mode 5. (f) Mode 6. (g) Mode 7. (h) Mode 8.

IV.VOLTAHE BALANCE OF FIVE-LEVEL INVERTER

The voltage balancing between two DC capacitors is very important in controlling the multi-level inverter. Here, voltage balance of DC capacitor voltages V_{C2} and V_{C3} can be controlled by the power electronic switches S_2 and S_3. When the absolute value of the utility voltage is smaller than $V_{dc}/2$, one power electronic switch either S_2 or S_3 is switched in high frequency and the other is still in OFF state. The voltage value of the DC capacitor V_{C2} or V_{C3} will decide the ON/OFF states of power electronic switches S_2 and S_3.

If V_{C2} is higher than V_{C3} the power electronic switch S_2 is switched in high frequency. In this condition, the voltage source V_{Cx} in Fig. 3(a) is equal to V_{C2}, and C_2 is discharged. Thus V_{C2} decreases and V_{C3} does not change. On the contrary, if V_{C3} is higher than V_{C2} the power electronic switched frequency. In this condition, the voltage source in Fig. 3(a) is equal to V_{C3}. Thus the DC capacitor voltage V_{C3} decreases and V_{C2} does not change. The voltage balance of C_2 and C_3 can be achieved in this way.

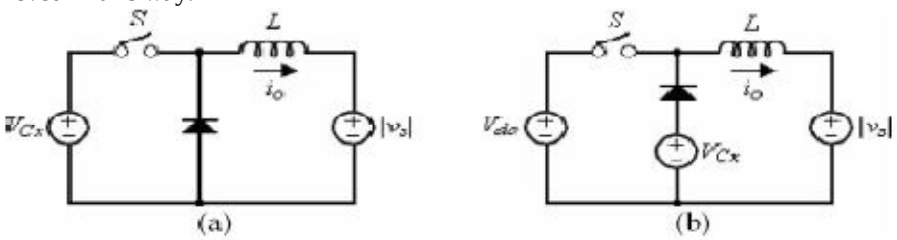

Fig. 3 Equivalent circuit. (a) $|vs| < Vdc/2$. (b) $|vs| > Vdc/2$

When the absolute value of utility voltage is higher than $V_{dc}/2$, one power electronic switch either S_2 or S_3 is switched in high frequency and other switch is still in ON state. Depending upon the voltage values of V_{C2} and V_{C3}, which power

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electronic switch (S_2 or S_3) is switched in high frequency can be found out. If V_{C2} is higher than V_{C3}, the power electronic switch S_3 is switched in high frequency and the voltage source V_{Cx} in Fig. 3(b) is equal to V_{C2}. when S_3 is turned ON, both C_2 and C_3 are discharged. However, when S_3 is turned OFF only C_2 supplies the power. In the same way, when V_{C3} is higher than V_{C2} the power electronic switch S_2 is switched in high frequency and the voltage source V_{Cx} in Fig. 3(b) is equal to V_{C3}. When S_2 is turned ON, both C_2 and C_3 are discharged. However, when S_2 is turned OFF only C_3 supplies the power. In this way, the voltage balance of C_2 and C_3 can be achieved. The logic for operation of power electronic switches S_2 and S_3 is represented in Table I.

Table I: ON/OFF states of S_2 and S_3

		$\|v_s\| < V_{dc}/2$	$\|v_s\| > V_{dc}/2$
$V_{C2}>V_{C3}$	S_2	PWM	ON
	S_3	OFF	PWM
$V_{C2}<V_{C3}$	S_2	OFF	PWM
	S_3	PWM	ON

V. CONTROL BLOCK DIAGRAM

The photovoltaic power generation system consists of a DC–DC power converter and the five-level inverter. The five-level inverter configured with dual-buck converter and full-bridge inverter performs the functions of converting the DC power into high-quality AC power and injecting it into the utility, balancing two dc capacitor voltages V_{C2} and V_{C3}, and detecting the islanding operation. The DC-DC Boost converter boosts the output voltage of the solar cell array and performs the MPPT to extract the maximum output power of the solar cell array. A control logic has been developed for the generation of PWM pulses in both five-level inverter and DC-DC Boost converter. The controllers of both the DC-DC Boost Converter and five-level inverter are explained as follows:

A. *Five-Level Inverter*

In the operation of the five-level inverter, the dc bus voltage must be regulated to be larger than the peak voltage of the utility and the dc capacitor voltages of C_2 and C_3 must be controlled to be equal. Besides, the five-level inverter must generate a sinusoidal current in phase with the utility voltage to be injected into the utility. As seen in Fig. 4, the voltages of dc capacitors C_2 and C_3 are detected and then added to obtain a dc bus voltage V_{dc}. The added result is subtracted from a dc bus setting voltage $V_{dc\ set}$. The dc bus setting voltage $V_{dc\ set}$ is larger than the peak voltage of the utility. The subtracted result is sent to a PI controller An islanding detection is also incorporated into the control of the five-level inverter.

As seen in Fig. 4, the utility current is detected and sent to an RMS detection circuit. The output of the RMS detection circuit is sent to a hysteresis comparator that contains a low threshold value and a high threshold value. If the RMS value of the utility current is smaller than the low threshold value, the output of the hysteresis comparator is high, meaning the condition of islanding operation or power balance occurs. On the contrary, the output of the hysteresis comparator is low when the RMS value of the utility current is larger than the high threshold value, meaning the utility is normal. The output of the hysteresis comparator is sent to a signal generator. The output signal of the signal generator is an islanding control signal S_a. The islanding control signal is a dc signal with unity amplitude if the output of the hysteresis comparator is low. On the contrary, the islanding control signal is a square wave with a frequency of 20 Hz (disturbance signal for islanding detection) when the output of the hysteresis comparator is high. The outputs of the PI controller and signal generator are sent to a multiplier, and the product of the multiplier is the amplitude of the reference signal. The utility voltage is detected and then sent to a phase-lock loop (PLL) circuit to generate an unity-amplitude sinusoidal signal whose phase is in phase with the utility voltage. The outputs of the multiplier and the PLL circuit are sent to the other multiplier. The product of this multiplier is the reference signal of the output current for the five-level inverter. The output current of the five-level inverter is detected by a current sensor. The reference signal and detected signal from the output current of the five-level inverter are sent to a sub tractor. The subtracted result is sent to a current-mode controller. The output of the current-mode controller is sent to a PWM circuit to generate a PWM signal. The detected dc capacitor voltages V_{C2} and V_{C3} are also sent to a comparator to obtain signal S_b . When dc

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capacitor voltage V_{C2} is higher than dc capacitor voltage V_{C3}, S_b is a high value. On the contrary, S_b is a low value when dc capacitor voltage V_{C2} is smaller than dc capacitor voltage V_{C3} . DC voltage V_{dc} is also sent to an amplifier with a gain of 0.5 to obtain voltage signal $V_{dc}/2$. The detected utility voltage is sent to an absolute circuit to obtain voltage signal $|v_s|$. Voltage signals $V_{dc}/2$ and $|v_s|$ are compared to obtain signal S_c . When $V_{dc}/2 > |v_s|$, S_c is a high value. On the contrary, S_c is a low value when $V_{dc}/2 < |v_s|$. The output signal of the PWM circuit and signals S_b and S_c are sent to the mode selection circuit. The output of the mode selection circuit will generate the control signals of power electronic switches S_2 and S_3 according to Table I. The detected utility voltage is also sent to a comparator to obtain complementary square signals that are synchronous with the detected utility voltage. The complementary square signals are the control signals of the power electronic switches of the full-bridge inverter. As mentioned earlier, only two power electronic switches S_2 or S_3 in the five-level inverter should be switched in high frequency, and only one of them is switched in high frequency at any time, and the voltage level of every switching is $V_{dc}/2$. Therefore, the five-level inverter can reduce the switching loss effectively.

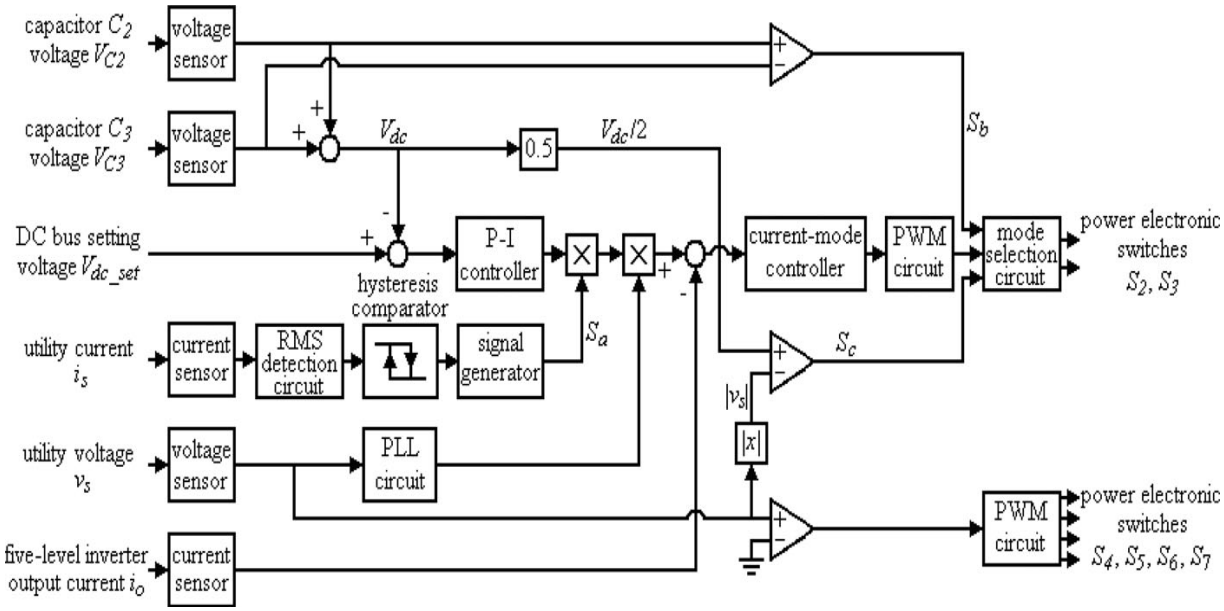

Fig. 4 Control block diagram of five-level inverter.

B. *DC-DC Boost converter*

The input of the DC-DC Boost converter is the output of the solar cell array. A ripple voltage with a frequency double that of the utility will appear in the dc bus voltage V_{dc}, while the five-level inverter injects real power into the utility. The function of MPPT will be degraded, while the output voltage of solar cell array contains a ripple voltage. Therefore, the ripple voltage super imposed on the DC bus voltage V_{dc} must be blocked by the DC–DC Boost converter for improving the function of MPPT. Accordingly, the dual control loops, an outer voltage control loop, and an inner current control loop are applied to control the DC–DC Boost converter as shown in Fig. 5. Since the output voltage of the DC–DC Boost converter is the DC bus voltage that is controlled to be a constant voltage by the five-level inverter, the outer voltage control loop is used to regulate the output voltage of the solar cell array. The inner current control loop is applied to control the inductor current to approach a constant current to block the ripple voltage of dc bus voltage V_{dc}. The perturbation and observation method is adopted to obtain the function of MPPT, and it is incorporated into the controller of the DC– DC Boost converter. The output of the MPPT controller is the desired output voltage of the solar cell array, and it is the reference voltage of the outer voltage control loop. The output voltage of the solar cell array is perturbed first, and then the output power variation of the solar cell array is observed to determine the next perturbation for the output voltage of the solar cell array.

The output power of the solar cell array is calculated from the product of the output voltage of the solar cell array and the inductor current. Therefore, the output voltage of the solar cell array and the inductor current are detected and sent

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to a MPPT controller to determine the desired output voltage of the solar cell array. The detected output voltage and desired output voltage of the solar cell array are sent to a sub tractor, and the subtracted result is sent to a PI controller. The output of the PI controller is the reference signal of the inner current control loop. The reference signal and the detected inductor current are sent to a sub tractor, and the subtracted result is sent to an amplifier to complete the inner current control loop. The output of the amplifier is sent to the PWM circuit. The output signal of the PWM circuit is the driving signal for the power electronic switch of the DC–DC Boost converter.

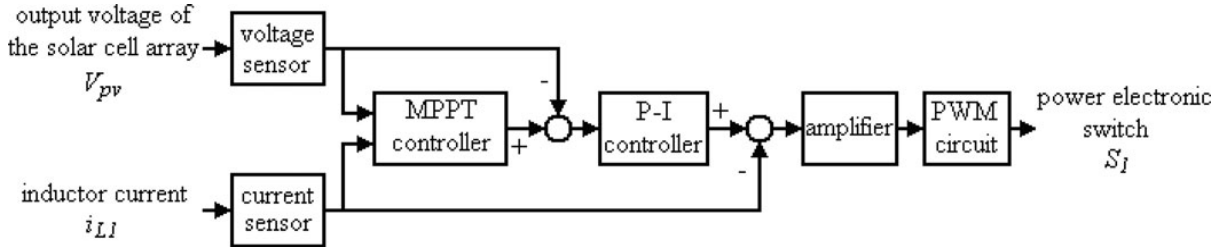

Fig. 5 Control block of DC-DC Boost converter

For protecting the renewable power generation system from the voltage rise, the MPPT function will be disabled and the power electronic switch S_1 will be turned OFF when the inverter stage is interrupted after detecting the islanding operation. Therefore, the output voltage of solar cell array is limited to the open-circuit voltage of solar cell array, and the dc bus voltage V_{dc} is also limited.

VI.CONCLUSION

The proposed five-level inverter is simulated using MATLAB/SIMULINK software to verify that the proposed inverter can be practically implemented in a PV system. The photovoltaic power generation system is developed for injecting the real power into the grid by using a five-level inverter to reduce losses and also to increase performance. The grid voltage was chosen to be 110V and the DC voltage was chosen as 170V since it must be greater than peak of grid voltage. Waveforms of grid voltage, inverter output current, inverter output voltage and capacitor voltages were obtained. Fig. 6 shows the grid voltage waveform, Fig. 7 shows inverter output voltage, Fig. 16 shows the current ripple of DC-DC Boost converter which is obtained with 1.6% current ripple by using a filter inductor of 5mH. The THD of inverter current was found to be 0.04%. THD% of inverter output was found to be 26.89%. The voltage of dc link capacitors shown in Fig. 9 and Fig. 10 were found to be balanced and each of the two capacitors stores 82.5V with a voltage ripple less than 5%.

Table II: Parameters used in Simulation

DC bus capacitor (C_2 and C_3)	2,200 μF
Filter inductor (L_f)	2mH
DC bus setting voltage	170V
Switching frequency (PWM)	20kHz
Utility voltage	110V
Utility frequency	60Hz
Load resistor	100 Ω
Open circuit voltage of solar panel	21.7V
Cell short circuit current	5.0A

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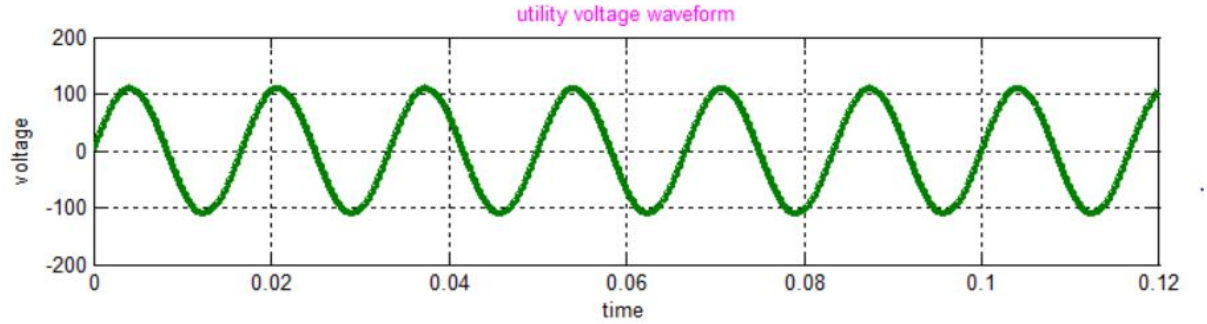

Fig. 6. Grid voltage waveform

Fig. 6 shows the experimental results of the utility voltage at the grid side i.e., 110V. This waveform is generated to match the obtained five-level output voltage with the peak voltage of the utility by converting the real power that is obtained for PV system so as to distribute the maximum output power in the form of AC to domestic loads.

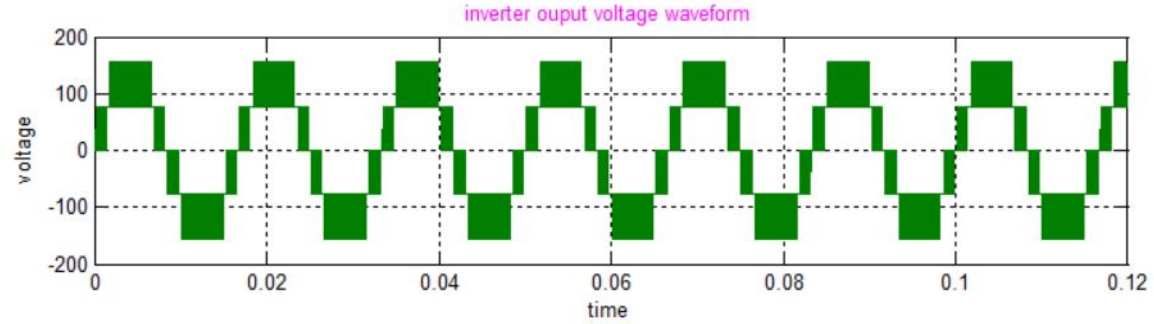

Fig. 7. Inverter output voltage waveform

Fig. 7 shows the experimental results for the five-level inverter used in the developed photovoltaic power generation system under steady state at five voltage levels V_{dc}, $V_{dc}/2$, 0, $-V_{dc}$, $-V_{dc}/2$ by the full-bridge inverter. The voltage variation of each level is $V_{dc}/2$. The output voltage waveform indicates the maximum voltage of 170V. This verifies that the five-level output AC voltage according to the utility voltage as explained above in the operating principle.

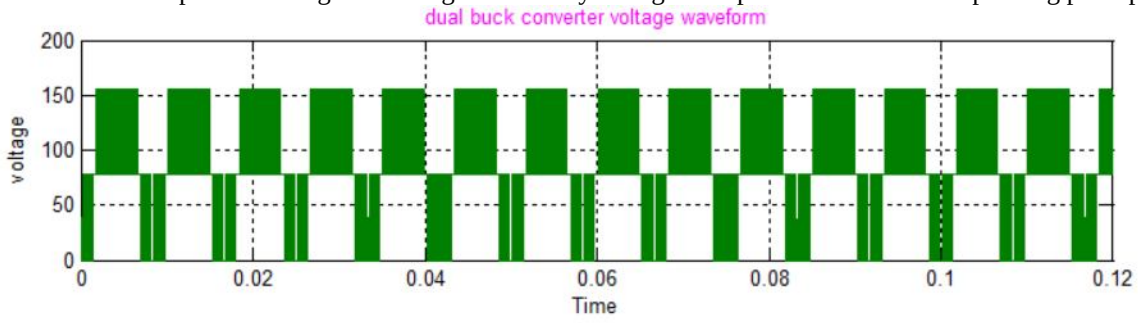

Fig. 8. dual-buck converter voltage waveform

Fig. 8 shows the experimental voltage of the dual-buck converter. The dual-buck converter outputs a DC voltage with three levels V_{dc}, $V_{dc}/2$ and 0. The output voltage of the dual-buck converter is further converted to an AC voltage with five voltage levels. The power electronic switches of the dual-buck converter is switched in high frequency.

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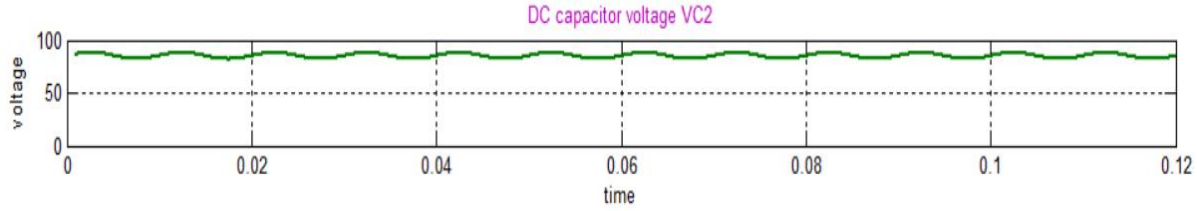

Fig. 9. DC capacitor voltage V_{C2}

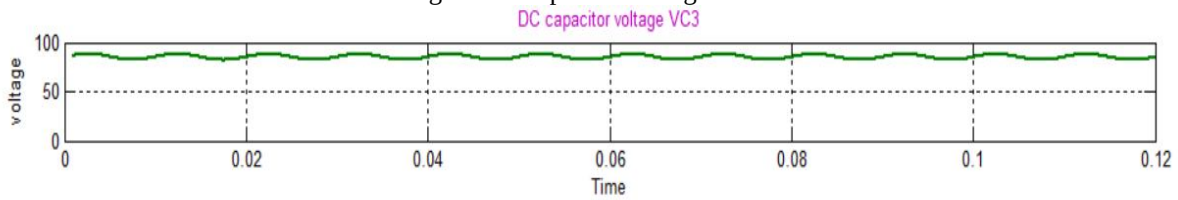

Fig. 10. DC capacitor voltage V_{C3}

Fig. 9 and Fig. 10 shows the DC capacitor voltages V_{C2} and V_{C3} remain in balance, and their voltage is about 85V, respectively.

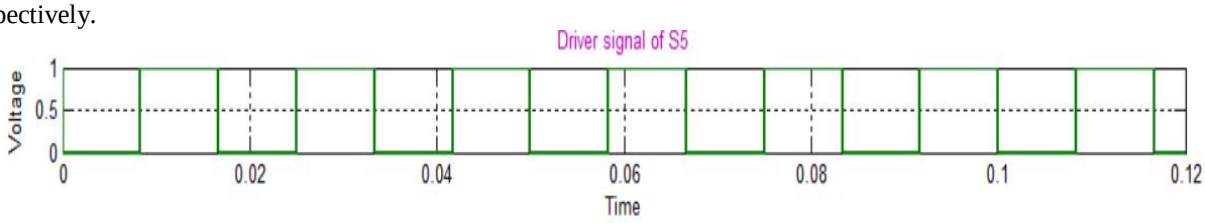

Fig. 11. Driver signal of S5

Fig. 12. Driver signal of S4(complementary square signal)

Fig. 11 and Fig. 12 shows the pulse generation of switches S_5 and S_4. The switching frequency of the switches is 60Hz.

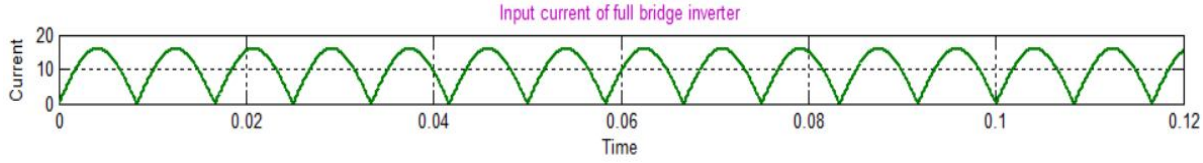

Fig. 13. Input current of full bridge inverter

Fig. 13 shows the absolute value of the output current of the full-bridge inverter. The power electronic switches of the full-bridge inverter are switched in low frequency, and the full bridge inverter can convert the DC power into AC power.

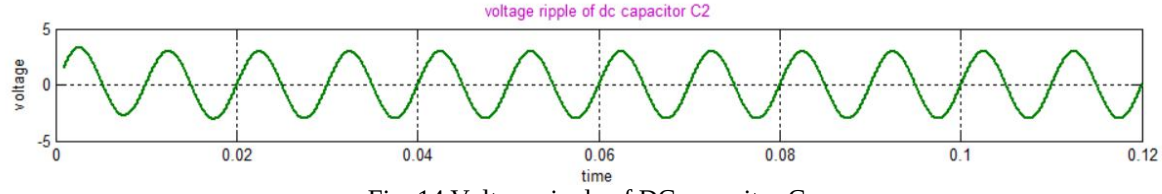

Fig. 14 Voltage ripple of DC capacitor C_2

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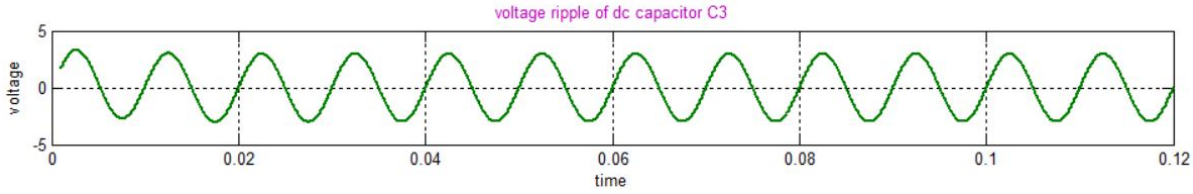

Fig. 15. Voltage ripple of DC capacitor C_3

Fig. 14 and Fig. 15 shows the peak-to-peak value of the voltage ripple at DC capacitors C_2 and C_3 is about 5V.

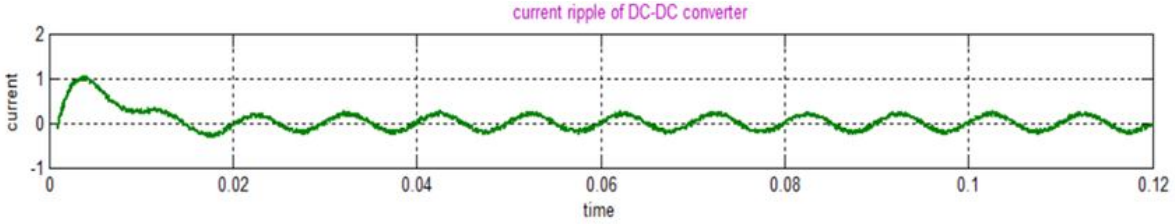

Fig. 16. Current ripple of DC-DC converter

Fig. 16 shows the ripple of inductor current is very small due to the use of the current mode control.

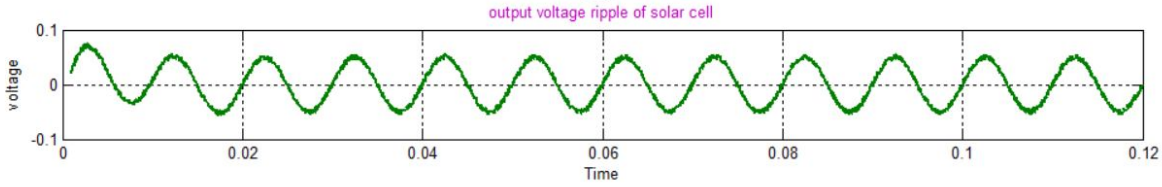

Fig. 17. Voltage ripple of solar cell

Fig. 17 shows the peak-to-peak value of the voltage ripple at the solar cell array is very small.

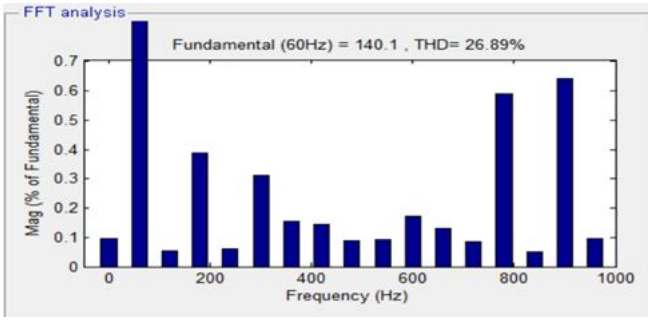

Fig. 18. FFT Analysis of output voltage of five-level inverter

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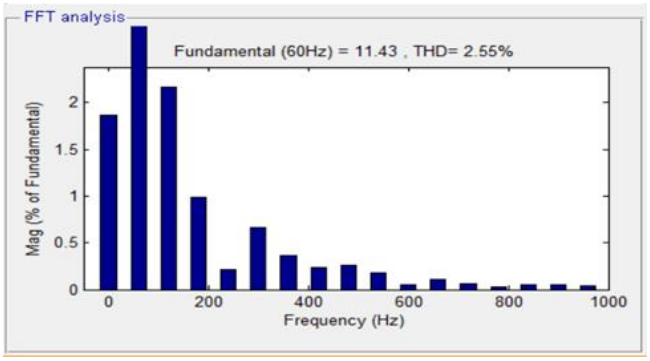

Fig. 19. FFT Analysis of utility voltage

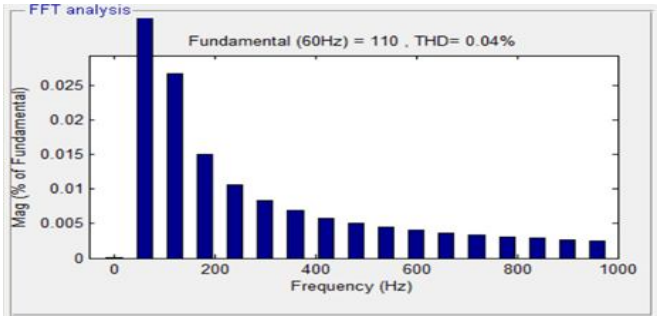

Fig. 20. FFT Analysis of output current of five-level inverter

From Fig. 19 and Fig. 20, it can be seen that the total harmonic distortion(THD%) of the utility voltage and the output current of the five-level inverter are 2.55% and 0.04% respectively.

Table III Comparison of different multi-level inverters

	Diode clamped	Flying capacitor	Cascaded H-bridge	Developed inverter
Power electronic switches	8	8	8	6
capacitors	2	4	2	2
Voltage balance of capacitors	Hard	Hard	Hard	Easy
High frequency switches	8	8	8	2

VI. CONCLUSIONS

The photovoltaic power generation system with a five-level inverter is developed. The proposed five-level inverter with dual-buck topology is simulated with the help of MATLAB/SIMULINK. The waveforms of grid voltage, inverter voltage, capacitor voltage etc., were obtained. By using the dual-buck converter the number of switches are reduced and it also effectively manages voltage balancing. The capacitor voltage was found to be almost balanced. Thus, the switching losses are comparatively less when compared to conventional topologies. Since, multi-level carrier based PWM technique is utilized to generate the switching pulses the reference and carrier signals are continuously compared and the switching pulses are generated according to the switching logic with a carrier frequency of 20kHz. The THD% of inverter current is found to be 26.89%. Thus as a whole the proposed five-level inverter with dual-buck topology is found to have good performance under grid connected application.

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