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Sleepy Stack Approach for Leakage Reduction of Low Power Flip Flop

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ABSTRACT: In today's world Leakage Power consumption of CMOS technology is of great challenge. According to the International Technology Roadmap for Semiconductors (ITRS) leakage power consumption may come to dominate total chip power consumption as the technology feature size shrinks. Leakage is a serious problem particularly for CMOS circuits in nanoscale technology below 20nm. In the proposed work sleepy stack method is used to reduce leakage power. Along with the leakage power consumption clock power is very serious issue. In the proposed work a low power flip flop with explicit clock and modified with signal feed through scheme is presented. The proposed design solves the issue of long discharging path which is problem in conventional explicit type pulse triggered flip flop. It also reduces power as well as delay than conventional P flip flop.

KEYWORDS: Leakage Power, explicit clock, Sleepy Stack, Signal feed through.

I.INTRODUCTION

Power consumption is one of the most important aspect of VLSI circuit design. The focus of designers is on low power design because of huge growing demands of portable battery operated applications. To solve the problem for power dissipation, many researchers have given different ideas from device to the architectural level. With the advance in the VLSI technology the channel length, oxide thickness and threshold voltage of transistor is reducing. This reduction in transistor parameters enhances the leakage current in nonlinear fashion. Power consumption in CMOS design is consists of dynamic and static components. Dynamic power consumption takes place when transistors are switching and static power is consumption takes place regardless of transistor switching. Dynamic power consumption was only concern previously for low power VLSI designs. One of the major reasons of causing the leakage power to increase is, increased in the sub threshold leakage current. When feature size is scales down, threshold voltage as well as supply voltage also scale down. The sub threshold leakage current increases exponentially as threshold voltage decreases [12].

Flip flops are the basic storage elements used in all kinds of digital designs. The digital designs nowadays adopt intensive pipelining techniques and employ many flip flop rich modules such as shift register, register file and counters. It is also estimated that the power consumption of the clock distribution networks and storage elements, is as high as 50% of the total chip power [2]. Pulse triggered FF because of its single-latch structure, is more popular than the conventional master slave and transmission gate based FFs in high speed applications. Besides the speed advantage the circuit simplicity lowers the power consumption of the clock distribution system.

A P-FF consists of a two parts a latch for data storage and pulse generator for enable strobe signals and. If the triggering pulses are narrow, then the latch acts like an edge-triggered flip flop. P flip flop allow time borrowing across clock cycle boundaries and feature a zero or even negative setup time [4]. Despite of these advantages, pulse generation circuitry requires delicate pulse width control to handle with possible variations in process technology and signal distribution network. The proposed work deals with a low-power P flip flop based on signal feed through technique. This mechanism is implemented by introducing a simple pass transistor to drive an extra signal.The combination of signal feed through scheme and sleepy stack technique not only reduces the active power as well leakage power of the design. As per the knowledge and survey of author none of the P flip flops designs are implemented by this scheme of leakage reduction. Results shows significant reduction in active power as well as delay when compared with conventional P flip flop designs ep-DCO, CDFF, MHLFF.

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II. LITEARTURE SURVEY

In many papers different flip flops are proposed overcoming the drawbacks of their presiding designs but problem of floating node has not been completely resolved. Along with this solution the complexity of designed circuit has been increased. Here are some designs which are revived in order to design flip flop having least floating node issue and for the reduction of the complexity.

CONVENTIONAL FLIP FLOP DESIGNES

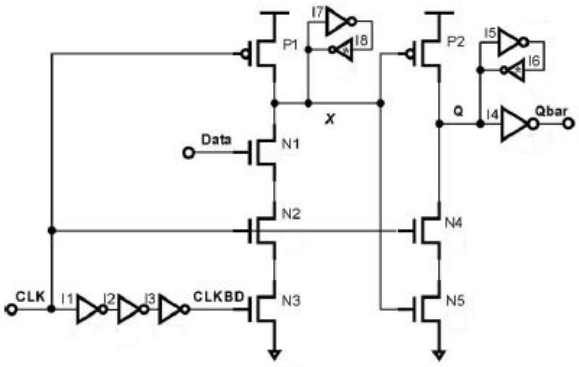

Fig. 1-(a)ip-DCO [6]

A low power flip flop designnamed ip-DCO, is given in fig. (a)[6]. It contains pulse generator based on AND logic semi dynamic latch design. Inverters I5 and I6 acts as buffer and are used to latch data andinverters I7 and I8 as buffer are used to hold logic of the internal node X. Two problems exist in this design, first is during the rising edge, NMOS transistors N2 and N3 getturned on. If data remains high i.e. at logic 1, node X will be discharged on every rising edge of the clock cycle. This leads to alarge switching power dissipation. Another problem is that node X controls two larger transistors P2 and N5. The large capacitive load to node X causes speed and power performance degradation.

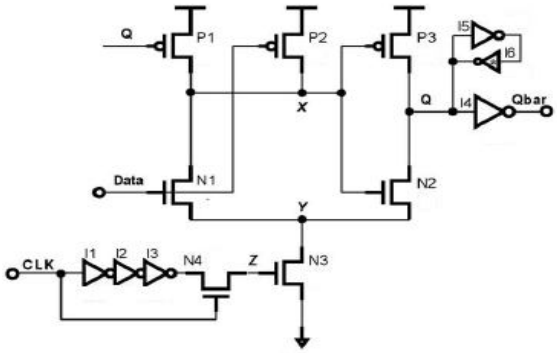

Fig. 1-(b) MHLFF [11]

Figure (b) shows an improved P-FF design, MHLFF i.e. modified hybrid latch flip flop by employinga static latch structure presented in [11]. In this design node X is no longerpre-charged periodically by the clock signal as that of in ip-DCO. A PMOS transistorP1 controlled by the FF output signal Q is used to maintain the logic of node X high when Q output is zero. This design gives solution to the unnecessarydischarging problem at node X. However, it has problem of a longer Data to Q delay during 0 to 1 transitions because node X is not pre-discharged. Large transistors N3 and N4 are required toenhance the discharging capability. One more drawback of this design is that node X becomes floating when output Q and input Data both equal to 1. It needs extra power if node X is drifted from an intact 1.

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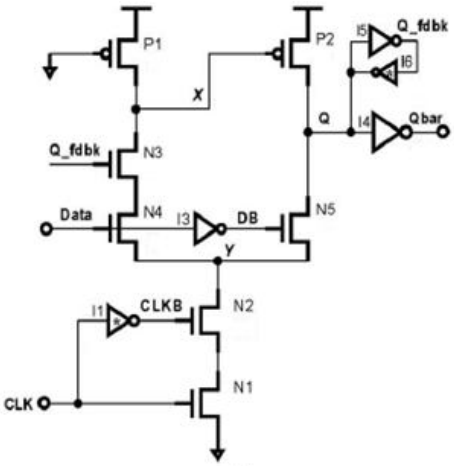

Fig.1- (c) SCCER [12]

Figure (c) shows a refined low power P flip flop design named as SCCERusing a conditional discharged technique. [9], [12]. In this design back to back inverters I7 and I8 in Figure (a) is replaced by PMOS transistor P1 in with an inverter I2 to reducethe load capacitance of node X [12].Since N3 is controlled by Q_fdbk no discharge occurs if inputdata remains high. The worst case timing of this design occurs when input data is 1 and node X is discharged through four transistors in series i.e. N1 through N4, while combating with the PMOS P1. A powerful pull down circuitry is thus required so that node X can be properly discharged. This implies bigger N1 and N2 transistorsand a longer delay from the delay inverter I1 to increase dischargepulse width.

III.PROPOSED LOW POWER P FLIP FLOP DESIGN

All reviewed designs encounter the same worst case timing occurring at 0 to 1 datatransitions. Referring to Figure 2(a), the proposed work adopts a signal feed through technique to improve this delay and improve the performance. Similar to the SCCER design, the proposed design also employs a static latch structure anda conditional discharge scheme to avoid switching at X which is an internal node.

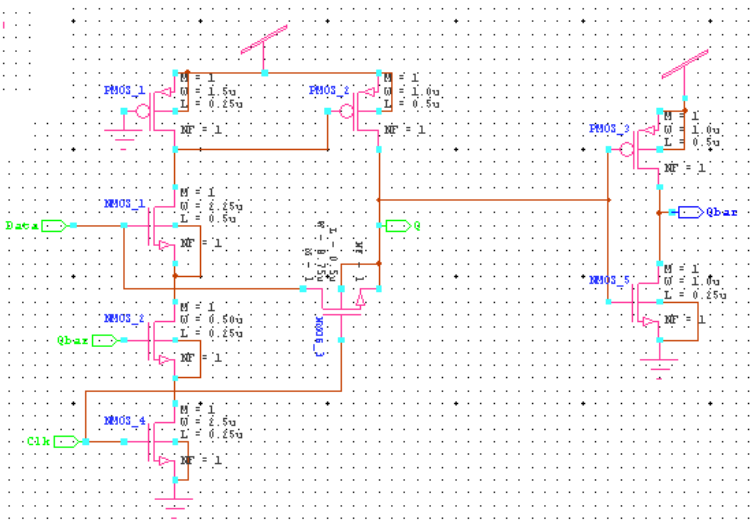

Fig.2-(a) Proposed Low Power Flip Flop

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The working of the proposed design is as follows. When a clock pulse arrives, if no data transition occurs, i.e. the input data and output Q are at the same logic level, the currentpasses through the pass transistor MNx. At the same time, the input data andthe output feedback Q_fdbk assume complementary signal levels and path of node X is off. So no signal change occurs at internal nodes. On the other hand if a '0' to '1' datatransition occurs, node X is discharged to turn on transistor MP2, which then change node Q high. The signal feedthroughscheme, a boost can be obtained from the input source via thepass transistor MNx and the delay can be greatly shortened. Although this seems to be a overheadto input source with direct charging and dischargingresponsibility, which is a common problem with the all pass transistor logic,the scenario is different in this case because MNx conducts only fora very short duration of time. When '1' to '0' datatransition occurs, transistor MNx is likewise turned on by the clockpulse and node Q is discharged by the input stage through this route. Unlike the case of '0' to '1' data transition, the input source bearsthe sole discharging responsibility. Since MNx is turned on for only a short duration of time the loading effect to the input source is not that much significant. To say in nutshell discharging does not correspond to the critical pathdelay and calls for no transistor size tweaking to enhance the speed.

SLEEPY STACK STRUCTURE

The proposed work introduces leakage power reduction technique 'sleepy stack'. The sleepy stack technique has a combinedstructure of the forced stack and the sleep transistor. Unlike the sleep transistor technique, thesleepy stack technique retains exact logic state when in sleep mode furthermore, unlike the forced stack technique, the sleepystack technique can utilize high- transistors without delay penalties [2]. Therefore, far better than any prior approach the sleepy stack technique can achieve ultralow leakage power consumption whilesaving state.

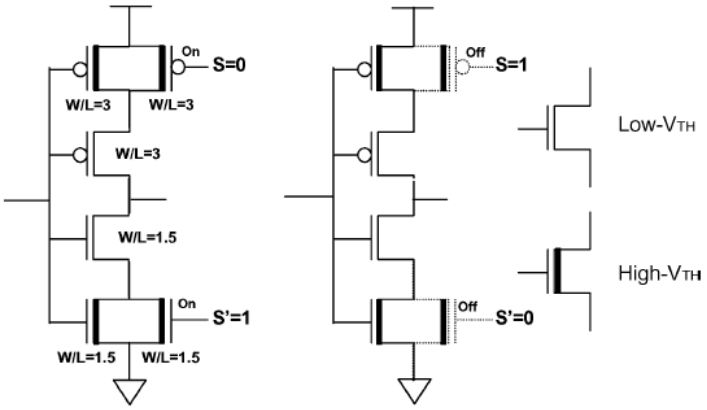

Fig. 4-Sleepy Stack Structure [2]

The sleepy stack structure hasa combined structure of the forced stack and the sleep transistortechniques. So we focus on implementation ofsleepy stack approach for leakage power reduction.The sleepy stack technique divides existing transistors into two transistors each typically with the same width W_1half the size of the original single transistor's widthW_0thus, maintaining equivalent input capacitance. The sleepy stack inverter in Fig. 4 uses$W/L = 3$ for the pull-up transistors and $W/L = 1.5$ for thepull-down transistors, while a conventional inverter with thesame input capacitance would use $W/L = 6$ for the pull-uptransistor and $W/L = 3$ for the pull-down transistor. Then sleep transistors are added in parallel toone of the transistors in each set of two stacked transistors. Proposed work uses a transistor sized as half the width of the original transistorfor the sleep transistor width of thesleepy stack. Although we exclusively use for the widthof the sleep transistor, changing the sleep transistor width invarious ways may provide additional tradeoffs between delay,power, and area. However, in this paper, we mainly focus onapplying the sleepy stack structure with sleep transistorwidths to generic logic circuits while varying technology featuresize, threshold voltage, and temperature. Please note thathalving transistor width is not possible for a circuit that usesminimum size transistors. However, many circuits use nonminimumsize to gain driving strength. In any case, if we cannothalve transistor width, then we simply use minimum width.

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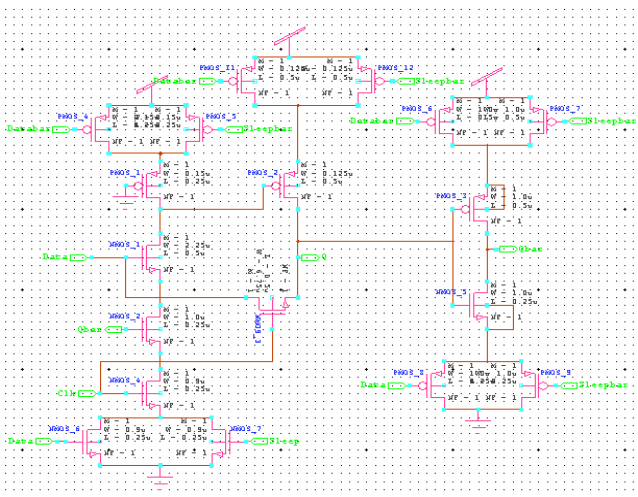

Fig. 5-Propose Sleepy Stack Low Power Flip Flop

Figure 5 shows the schematic of proposed sleepy stack low power flip flop simulated in S- edit of tanner EDA tool.The sleepy stack structure is connected at footer and header i.e. at Vdd and Gnd. In active mode these structures allows normal flip flop logic but in inactive mode (C=0,D=0 of C=D=0) it offers high resistance in the path of leakage current from Vdd to Gnd , as in these cases the transistors get off.

The performance of the proposed low power P flip flop is evaluated against existing designs. The compareddesigns include three low power P flip flop designs shown in Fig. a, b and c.(ip-DCO [6], MHLLF [11], SCCER [12]). The comparison is done on the basis of power delay and number of transistors.The target technology is the TSMC 18-nm CMOS process and supply voltage is 1V.All designs are further optimizedto balance the tradeoff between power and D to Q delay, i.e. minimizing the product of the two terms.

IV. RESULT AND DISCUSSION

The simulation has been done in Tanner EDA v-13 tool with VDD 1V in 18 nm technology .

Table1- Analysis of Power, Delay and Area

Flip Flop	ep-DCO	SCCER	MHLFF	Proposed Design	Proposed Stack	Proposed Sleepy Stack
No. of Transistors	23	17	18	8	10	11
Delay(D to Q)	$4.4X10^{-10}$	$6.5X10^{-10}$	$4\ X10^{-9}$	$4.41\ X10^{-11}$	$5.83X10^{-10}$	$4.26X10^{-10}$
Average Power	$4.35X10^{-7}$	$7.44X10^{-6}$	$6.2X10^{-6}$	$1.52X10^{-8}$	$4.31X10^{-8}$	$3.32X10^{-8}$
100% Data Activity	$4.43X10^{-7}$	$4.0X10^{-6}$	$2.46X10^{-7}$	$8.4X10^{-7}$	$7.46X10^{-8}$	$1.18X10^{-6}$
50% Data Activity	$3.53X10^{-7}$	$6.5X10^{-6}$	$1.741X\ 10^{-7}$	$4.6X10^{-7}$	$1.78X10^{-7}$	$8.73X10^{-7}$
25% Data Activity	$4.34X10^{-7}$	$4.51X10^{-6}$	$3.79X10^{-7}$	$3.58X10^{-7}$	$1.00X10^{-7}$	$5.94X10^{-7}$
0% Data Activity All 0's	$3.1X10^{-7}$	$7.81X10^{-6}$	$5.21X10^{-7}$	$3.22X10^{-9}$	$4.47X10^{-9}$	$4.74X10^{-9}$

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0% Data Activity All 1's	$4.47X10^{-7}$	$1.18X10^{-7}$	$4.26X10^{-7}$	$1.38X10^{-8}$	$3.5X10^{-8}$	4.74X8
Power Delay Product (JS)	$1.914X\ 10^{-16}$	$4.836X10^{-15}$	$2.48X\ 10^{-14}$	$6.7X10^{-19}$	$2.51X10^{-17}$	$6.98X10^{-20}$

In table 1.the analysis of power, delay and area has been done on ep-DCO, SCCER, MHLFF, Proposed flip flop, Proposed flip flop with Stack, Proposed flip flop with Sleep, Proposed flip flop. The proposed structure significantly reduces the power as well as the delay as compared to the conventional structures. The stack and sleepy stack structures are used for reduction of the leakage power.

Table2- Analysis of Leakage Power

Flip Flop		ep-DCO	SCCER	MHLFF	Proposed Design	Proposed Stack	Proposed Sleepy Stack
Clk	Data						
0	0	$8.78X10^{-10}$	$7.48X10^{-6}$	$6.03X10^{-11}$	$3.23X10^{-11}$	$1.01X10^{-11}$	$7.0X10^{-12}$
0	1	$9.56X10^{-10}$	$2.54X10^{-9}$	$3.54X10^{-5}$	$6.6X10^{-11}$	$2.3X10^{-11}$	$7.16X10^{-12}$
1	0	$9.34X10^{-10}$	$1.03X10^{-5}$	$1.55X10^{-7}$	$4.62X10^{-11}$	$3.1X10^{-11}$	$8.2X10^{-12}$

Table 2 shows analysis of leakage power in all the conventional designs, proposed design and proposed flip flop design with sleep, stack and sleepy stack structure. The sleepy stack approach for flip flop design gives best reduction in power followed by the sleep and stack approach. In the stack transistor approach the pair of stack transistor in off state increases the resistance for leakage current these stack transistors has W/L ration halved and connected in series their by maintain the same output resistance. The sleepy stack method takes the advantage of both techniques and without loss of data gives 17 times reduction of leakage power than conventional approach.

V.CONCLUSION

In this brief, we presented a novel P-FF design by employing a modified TSPC latch structure incorporating a mixed design style consisting of a pass transistor and a pseudo-nMOS logic. The key idea was to provide a signal feedthrough from input source to the internal node of the latch, which would facilitate extra driving to shorten the transition time and enhance both power and speed performance. The design was intelligently achieved by employing a simple pass transistor. In Sleepy Stack approach the leakage power as well as average power has been reduced drastically. Extensive simulations were conducted, and the results did support the claims of the proposed design in various performance aspects.

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