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APWM Based Multiple Output ZVS DC/DC Converter

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ABSTRACT: This project presents a new soft-switching dc/dc converter with series-connected transformers to implement the features of ZVS, low voltage stress for MOSFETs. The converter includes two half-bridge circuits connected in series to limit the voltage stress of MOSFETs at one-half of the input voltage. The output sides of four circuits are connected in series and parallel to primary circuit. The proposed multi output converter shows excellent performance in terms of its output regulation from no-load to full-load conditions and its provide multi output capability .

KEYWORDS: DC–DC converter, Asymmetrical half-bridge, multi output converter, soft switching.

I. INTRODUCTION

POWER FACTOR corrections (PFCs) have been widely used in modern power converters to compensate the reactive power and eliminate the ac current harmonics at the utility side. For a three-phase 380-V PFC converter or a single-phase PFC converter with wide input voltage range in South Africa or India, the dc bus voltage may be greater than 600 V. Therefore, MOSFETs with 600-V voltage stress and low turn-on resistance cannot be used in the rear dc/dc stage. Although high-voltage MOSFETs such as those with 900-V voltage stress can be used in the rear dc/dc converter, the disadvantages of high voltage MOSFETs are high cost and large turn-on resistance By using more MOSFETs, split capacitors, the voltage stress of each MOSFET can be reduced to one-half of the dc bus voltage. Therefore, MOSFETs with 600-V voltage stress can be used in the rear dc/dc converter for high-input-voltage was normally adopted to generate four PWM signals for power switches with zero-voltage switching (ZVS) turn-on at the designed load range.[1-4] A isolation transformers are adopted in the secondary side for low or high-voltage applications. Soft-switching techniques [5], [8]–[14] have been developed and proposed for the past 20 years to reduce switching losses and increase circuit efficiency.

This paper presents a new soft-switching dc/dc converter for high-input-voltage applications. The main advantages of the proposed converter are low switching losses, ZVS turn-on, and low voltage stress on MOSFETs. Two capacitors and two half-bridge circuits are connected in series at the high-voltage side to clamp the voltage stress of MOSFETs at one-half of the dc bus voltage. Asymmetric PWM (APWM) is adopted to control four MOSFETs so that the general PWM IC with three isolated gate drives can be used in the proposed circuit. Based on the resonant behavior by the output capacitance of MOSFETs and the resonant inductance, MOSFETs can be turned on at ZVS. Experiments with a 1-kW prototype are presented to verify the effectiveness of the proposed converter.

II. CIRCUIT CONFIGURATION

Fig.1 shows the circuit configuration of the stacked half-bridge ZVS dc/dc converter with low voltage stress on MOSFETs and with fewer circuit components to achieve load current sharing. The input dc bus voltage is obtained from a three-phase 380-V ac utility voltage with a diode rectifier. The normal dc input voltage Vin = 480–600 V. Two input voltage supplies and two half-bridge circuits are connected in series at the high-voltage side to limit the voltage stress of MOSFETs at one-half of the dc bus voltage. Therefore, MOSFETs with 500-V voltage rating can be used in this circuit. The components of circuit 1 include Vin /2, S1 , S2 , Cr1 , Cr2 , C1 , Lr1 , T1 , S5 , S6 , and Lo1 . Circuit 2 includes the components of Vin /2, S3 , S4 , Cr3 , Cr4 , C3 , Lr3 , T4 , S7 , S8 , and Lo2 . However, the components of

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the third circuit include Vin , S1 –S4 , Cr1 –Cr4 , C2 , Lr2 , T3 , T4 , S5 –S8 , Lo1 , and Lo2 . Co and Ro denote the output capacitance and load resistance, respectively. C1 –C3 are the dc blocking capacitances.

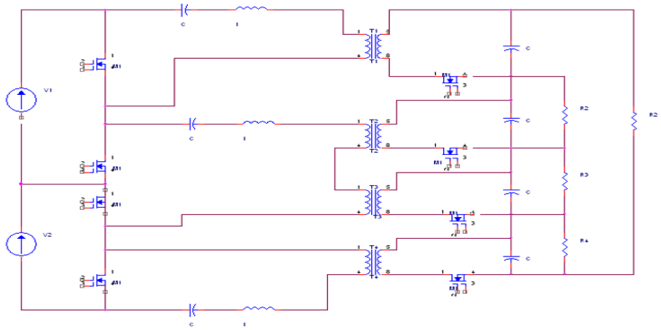

Fig. 1.Proposed converter .

The dc blocking voltages VC1 –VC3 are related to the duty ratio of MOSFETs. Cr1 –Cr4 are the output capacitances of MOSFETs S1 –S8 , respectively. Lr1 –Lr3 are the resonant inductances. Lm1 –Lm4 are the magnetizing inductances of transformers T1 –T4. The APWM scheme is used to control MOSFETs S1 –S4 . S5 - S8 have the same pwm signal.S1 and S4 have the same PWM signals, and S2 and S3 have the same PWM waveforms. However, S1 and S2 are complementary to each other with a dead time to allow ZVS operation. Therefore, the PWM signals of S1 –S4 can be easily generated by an analog PWM IC and three isolated gate drivers. The voltage stress of S1 –S4 is clamped to Vin /2. Since the secondary windings of four circuits are connected in series, four output capacitors currents are automatically balanced for high-output-current applications.[5-8]

III .CIRCUIT OPERATING PRINCIPLE

The theoretical waveforms of the proposed converter in one switching cycle. The duty cycle of S1 and S4 is δ, and the duty cycle of S2 and S3 is 1 − δ. Before the system analysis, the following assumptions are made:
1) MOSFETs S1 –S4 and diodes S5 –S8 are ideal;
2) Lm1 = Lm2 = Lm3 =Lm , and Lo1 = Lo2 = Lo ;
Lm4 = Lm , Lr1 = Lr2 = Lr3
3) the turn ratio of transformers T1 –T4 is
n = np /ns1 =np /ns2 ;
4) Cr1 = Cr2 = Cr3 = Cr4 = Cr and C1 = C2 = Cr ; and
5) the energy stored in resonant inductorsC3 = Cc is greater than the energy stored in resonant capacitors such that the ZVS turn-on of all switches can be achieved. Based on the ON / OFF states of S1 –S8 , there are four operation modes in one switching cycle. [9-10]

Mode 1 [t0 ≤ t < t1] ; During this interval, all switches i.e. S1,S2,S3,S4,S5,S6,S7,S8 turned off.c1,c2,c3 are charged in this mode.Lr1,Lr2 ,Lr3 are almost constant.c4,c5,c6,c7 discharged in this time.

Mode 2 [t1 ≤ t < t2 ; Fig. 3(b)]: At t1 **]:** During this interval, the antiparallel switches of *S*1 and *S*4 are conducting at *t*2. Before *iS*1 and *iS*4 are positive, *S*1 and *S*4 must be turned on to achieve ZVS. S2,S3 and S5-S8 switches are also on condition capacitors can charge in this mode .at the same time Lr1, Lr3 stores the energy . switches s2,s3 turned off.

Mode 3: [t2 ≤ t < t3] **]:** During this interval, the antiparallel switches of *S*1 and *S*4 are OFF. S2,S3 switches are On condition and S5-S8 switches are OFF condition, capacitors are discharge in this mode.

Mode 4[t3 ≤ t < t4] **:** During this interval, the antiparallel switches of *S*1 and *S*4 are ON. S2,S3 switches are OFF condition and S5-Sc8 switches are OFF condition, capacitors are discharge in this mode. . This mode ends at t0 **+** Ts when S2 and S3 are turned off. Then, the circuit operations of the proposed converter in one switching cycle are completed.

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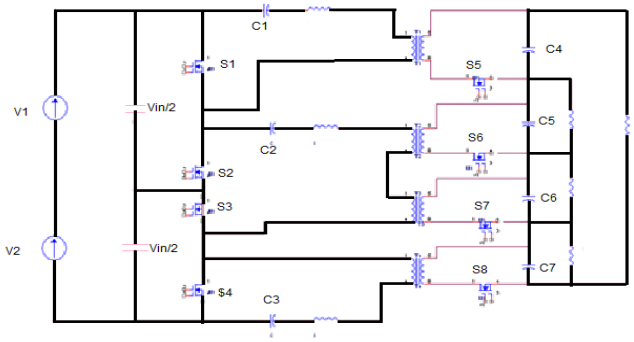


Fig.(2a)

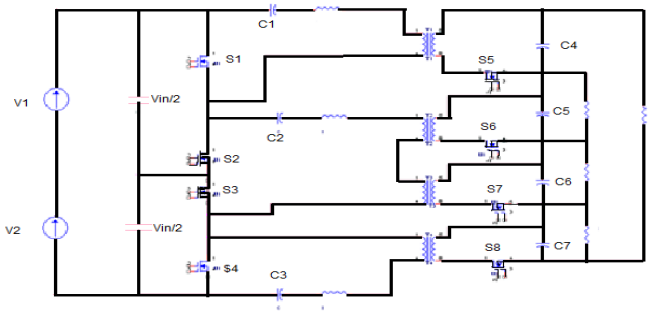
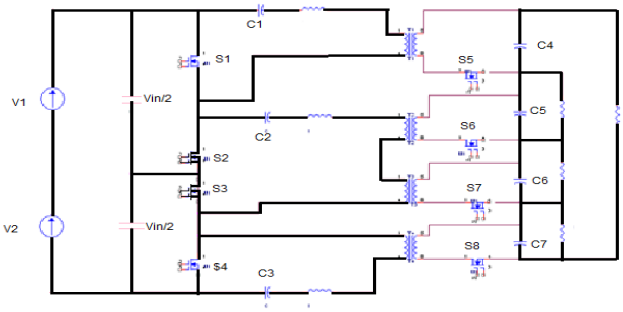
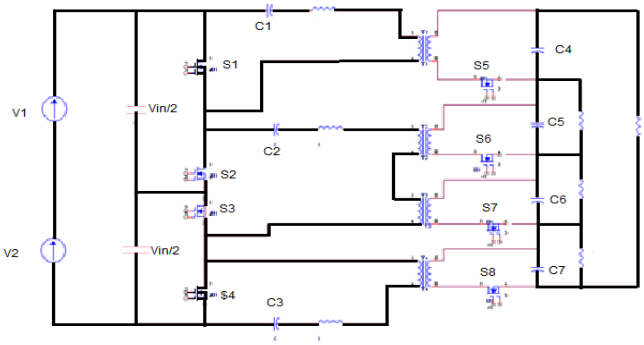


Fig.(2b)



Fig(2c)



Fig(2d)

IV. EXPERIMENTAL R ESULTS

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Experimental results are provided to demonstrate the effectiveness of the proposed converter. The circuit specifications of a laboratory prototype are Vin = 480–600 V, Vo1 = 45 V, Vo2 = 8.4, Vo3 = 7.8 V ,Vo4 = 13.5 V and Po = 1 kW. The switching frequency fs is 100kHz.The nominal input voltage Vin, nom is 540 V. The maximum duty cycle of S1 and S4 is selected as 0.45 for the case of Vin = 480 V and Po = 1 kW. MOSFETs IRFP460 are used for S1 –S4 . The dc blocking capacitances are C1 = C3 = 330 nF and C2 = 660 nF. The resonant inductances are Lr1 = Lr3 = 18 µH and Lr2 = 36 µH. The fast recovery diodes U30D20C are used for D1 –D6 . The turn ratio of transformers T1 – T4 is 34 : 5 : 5. The magnetizing inductance of T1 –T4 is 870 µH. The output capacitance is Co = 6200 µF. The output inductances are Lo1 = Lo2 = 46 µH. The measured PWM signals of S1 –S4 at full load and the different input voltages are shown in Fig. 4a. Fig. 4b shows the measured gate voltage, drain voltage, and switch current of switches S1 and S2 at the nominal input voltage Vin = 540 V and 25%- to 100%-load conditions. The drain voltages vS1,ds and vS2,ds have been decreased to zero voltage before switches S1 and S2 are turned on. Thus, S1 and S2 are turned on at ZVS from 25% to 100% load. Since the switches S1 and S4 have the same PWM waveforms and S2 and S3 have the same PWM waveforms, it is clear that S3 and S4 are also turned on at ZVS. shows the measured waveforms of the gate voltage vS1,gs and the inductor currents iLr1 –iLr4 at full load and the nominal input voltage. When switch S1 is in the ON state, the inductor currents iLr1 and iLr3 decrease, and iLr2 increases. On the other hand, inductor currents iLr1 and iLr3 increase and iLr2 decreases if switch S1 is in the OFF state. Fig. 7 shows the measured waveforms of vS1,gs , vC1 , vC2 , and vC3 at full-load condition. When switch S1 is on, the inductor currents iLr1 and iLr3 are negative so that capacitor voltages vC1 and vC3 decrease. However, inductor current iLr2 is positive so that capacitor voltage vC2 increases. Fig. 8 shows
the measured waveforms of vS1,gs , iS5 –iS8 , iLo1 , and iLo2 at full-load condition. The load current Io is equally supplied by output capacitors currents iCo1 and IC4 .[11-13]

V. SIMULATION RESULTS

A four-stage multiple output voltage of the APWM DC-DC converter for the simulation as shown in Fig.3.MATLAB/SIMULINK is used for simulation. The system is designed based on the the system specifications and the components as mentioned in experimental results .[14-17]

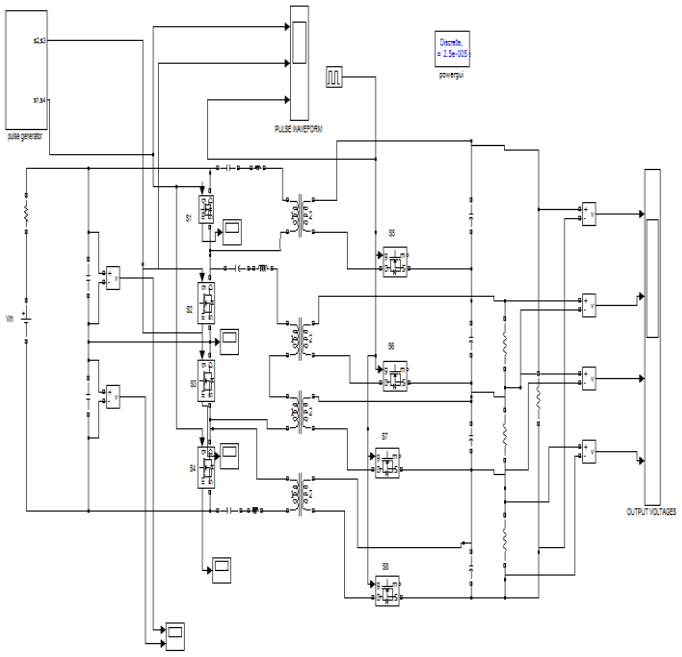

Fig.3. Simualtion of proposed converter

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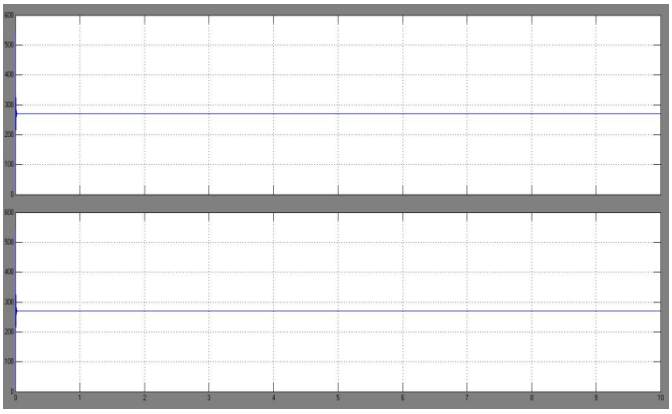

Fig(4a)

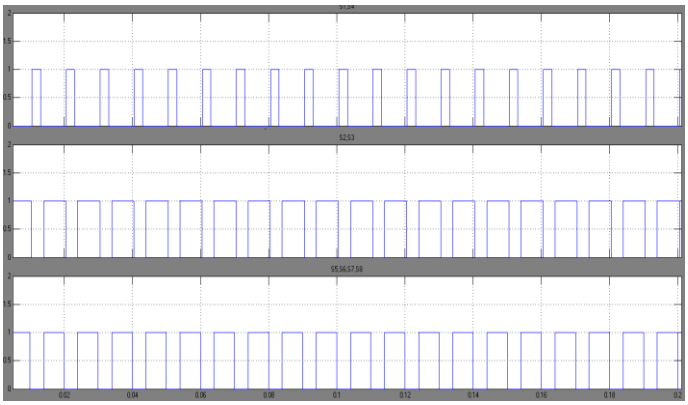

Fig.(4b)

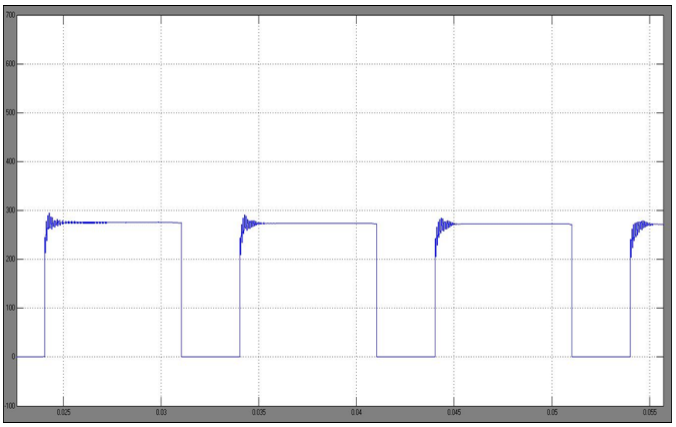

Fig.(4c)

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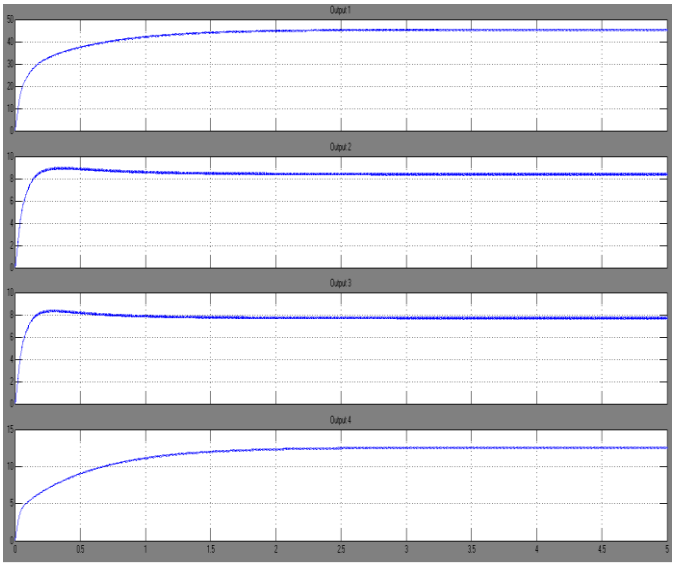

Fig.(4d)

Fig.4.(a)Input voltage (b)Switching Waveform.(c)Switch across the voltage for S1.(d) output voltage of the Dc-Dc converter and converter across load.

VI. CONCLUSION

This project has presented a new dc/dc converter with series connected transformers. The main functions of the proposed converter are as follows: 1) ZVS turn-on for all power switches; and 2) low voltage stress of power switches with a series half-bridge converter. Two split capacitors and two half-bridge converter circuits connected in series were used at the high-voltage side to limit the voltage stress of power switches at one-half of the input voltage. Thus, the MOSFETs can be used in high input voltage applications to achieve high switching frequency, low converter size, and high circuit efficiency.

Three APWM converters were used in the primary side, and the output sides of four circuits are connected in series and parallel to primary circuit. The proposed multi output converter shows excellent performance in terms of its output regulation conditions and its provide multi output capability .

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