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Mitigation of Power Quality Disturbances Using UPQC Based On HDE Optimization Technique

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ABSTRACT: This paper presents a new synchronous reference frame theory based control strategy to mitigate power quality disturbances through UPQC to enhance the power quality at distribution level. UPQC is an integration of STATCOM and DVR connected in back-to-back configuration with the help of DC-link capacitor. The proposed UPQC can compensate voltage sag and mitigate current harmonics. The simulations were performed on 33kv line with non-linear load and results were plotted .To obtain the optimal values of K_P, K_I, the PI controller in SRF theory is optimized with HDE technique. The simulations were performed in MATLAB 7.10.0.499(R2010a)/SIMULINK software.

KEYWORDS: Static Synchronous Compensator (STATCOM), Dynamic Voltage Restorer (DVR), Unified Power Quality Conditioner (UPQC), Synchronous Reference Frame (SRF) Theory, Total Harmonic Distortion (THD), Hybrid Differential Evolution (HDE).

I. INTRODUCTION

It has been always challenge for an electrical engineer to maintain good power quality within the desired tolerance. Poor power quality has several adverse effects. One of the main causes for the degradation of power quality is harmonic currents and voltage sags. Harmonic currents are mainly caused due to the operation of non-linear loads. These harmonic currents at load side are injected back into source side as a result source current becomes distorted. These harmonic currents are mitigated with the help of STATCOM by injecting reverse harmonics into the line. Voltage sags are mainly caused due to energization of heavy loads. These are compensated with the help of DVR [1]-[3]. UPQC is an integration of STATCOM and DVR connected in back-to-back configuration with the help of a DC-link capacitor. The proposed UPQC can mitigate current harmonics as well as compensate voltage sag simultaneously [4].

SRF theory is used to generate reference currents and compensating voltages. This theory was based on Parks transformation. The three phase ac components (a,b,c) from a stationary frame are transformed into (d,q,o)synchronously rotating frame[5]–[6] which are DC quantities. It is easier to analyze DC quantities rather than AC quantities. The phased locked loop (PLL) is used to generate sin (wt), cos (wt) which are needed for synchronizing purpose . To reduce the steady state error PI controller is used. Further simulations were performed based on knowledge from SRF theory.HDE technique is utilized as a tool for evaluating the optimal values of K_P and K_I to reduce the THD. HDE is a stochastic search and optimization method similar to DE method [7]–[9]. The main advantage of DE technique is fast convergence rate. However this descends the diversity of population. In order to overcome that drawback the migration operation like in genetic algorithm is used in HDE technique which makes it more robust than DE technique. This paper compares the simulation results with conventional PI controller and PI controller optimized with HDE (PI-HDE) which were performed in MATLAB 7.10.0.499(R2010a)/SIMULINK software.

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II.UPQC

It is a most versatile power quality conditioner that can mitigate power quality disturbances like voltage sag, voltage swell, and current harmonics. UPQC have two voltage source inverters connected in back to back configuration sharing a common dc link capacitance [1]–[5]. One inverter is connected in parallel with the load. It acts as STATCOM that injects reverse harmonics into the line and mitigates the harmonics in the source current and makes the source current harmonic free. The other inverter is connected in series with the line through series transformer. Whenever the supply voltage undergoes sag then DVR injects suitable voltage with supply and makes load voltage balanced.
The main objectives of UPQC in this paper are

A. It eliminates the harmonics in the supply current.
B. It maintains load end voltage at the rated value even at the time of voltage sag
C. To regulate the DC bus voltage.

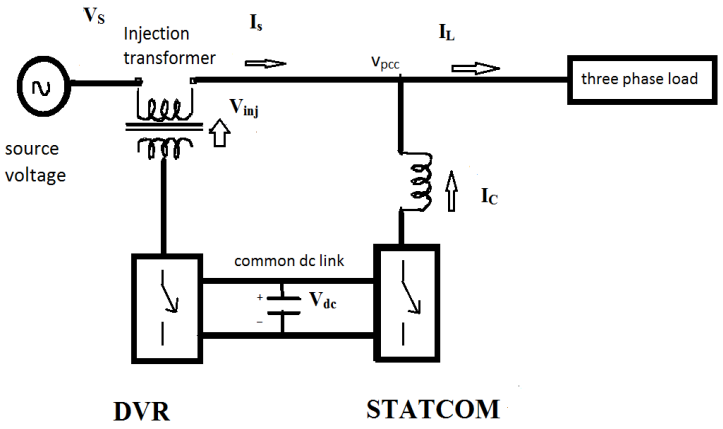

Fig. 1. Block diagram of UPQC.

III. SRF THEORY

A. STATCOM

This theory is used to generate reference currents. It is based on Park transformation. The load currents from a stationary reference frame (a-b-c) are transformed into synchronously rotating frame (d-q-o) as a result they are converted into DC quantities .It is easier to analyse in DC quantities rather than AC quantities. The phased locked loop (PLL) is used to synchronize the reference frame with supply voltage. The i_d and i_q components comprises both AC and DC components. The DC component corresponds to fundamental load currents and ac component corresponds to load current harmonics. The isolation of ac components can be achieved by filtering out the DC-offset. PI controller is used to control the DC link voltage. The (d-q-o) frame is again converted into (a-b-c) frame to get required reference currents (I_a^*, I_b^*, I_c^*). These are given to hysteresis band current controller to generate the gating pulses for inverter.

$$I_{ds} = \sqrt{2/3}\,(i_a \cos\theta + i_b \cos(\theta-120^0) + i_c \cos(\theta+120^0)) \rightarrow (1)$$

$$I_{qs} = \sqrt{2/3}(i_a \sin\theta + i_b \sin(\theta-120^0) + i_c \sin(\theta+120^0)) \rightarrow (2)$$

$$I_a^* = I_{ds}\cos\theta + I_{qs}\sin\theta \rightarrow (3)$$

$$I_b^* = I_{ds}\cos(\theta-120^0) + I_{qs}\sin(\theta-120^0) \rightarrow (4)$$

$$I_c^* = I_{ds}\cos(\theta+120^0) + I_{qs}\sin(\theta+120^0) \rightarrow (5)$$

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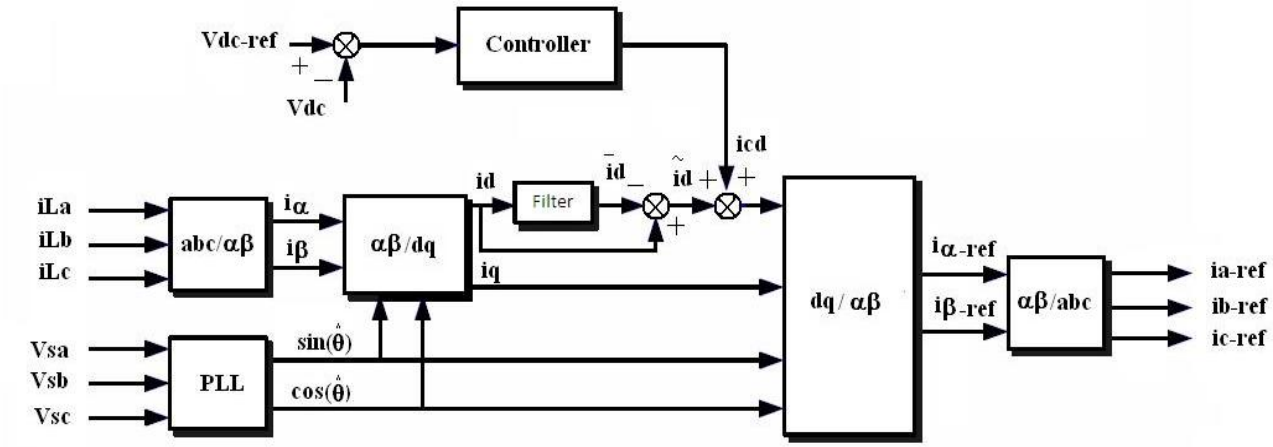

Fig. 2. Control block diagram of STATCOM

B.DVR

This theory is used to generate reference voltages. The three phase set of voltages are transformed into direct and quadrature components as a result it is possible to control active and reactive power independently. In order to inject the active power into the line the DC quantities are compared with 1 and 0. The active power is injected only when current and voltage are in same phase. The error is given to PI controller and again (d-q-o) frame is converted into (a-b-c) frame to get required voltages. These compensated voltages are given to SPWM to generate the required gating pulses for the inverter.

$$\begin{pmatrix} V_{qs} \\ V_{ds} \\ V_{os} \end{pmatrix} = 2/3 \begin{pmatrix} \cos\theta & \cos(\theta-2\pi/3) & \cos(\theta+2\pi/3) \\ \sin\theta & \sin(\theta-2\pi/3) & \sin(\theta+2\pi/3) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{pmatrix} \begin{matrix} Vas \\ Vbs \\ Vcs \end{matrix} \quad \rightarrow (6)$$

$$(V_{qdo}) = KV_{abc} \quad \rightarrow (7)$$

$$(V_{abc}) = K^{-1}(F_{qdo})^{T} \quad \rightarrow (8)$$

$$K^{-1} = \begin{pmatrix} \cos\theta & \sin\theta & 1 \\ \cos(\theta-2\pi/3) & \sin(\theta-2\pi/3) & 1 \\ \cos(\theta+2\pi/3) & \sin(\theta+2\pi/3) & 1 \end{pmatrix} \quad \rightarrow (9)$$

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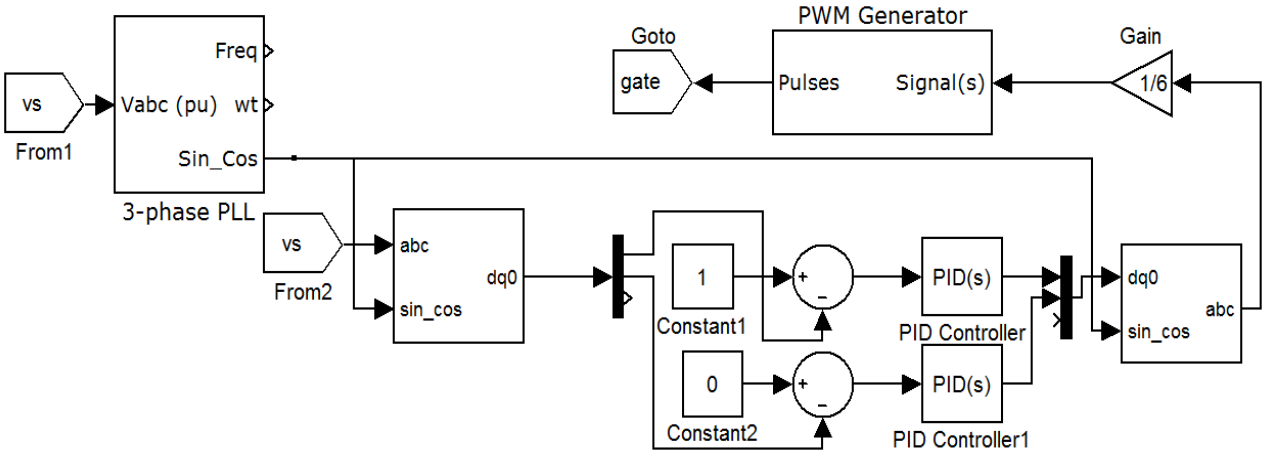

Fig. 3. Control block diagram of DVR

IV. GATING TECHNIQUES

A. HBCC

The gating signals to voltage source inverter (VSI) are given with the help of hysteresis band current controller (HBCC) because of its simplicity and fast response. In this the controlled current is forced to track the reference current within the hysteresis band. The inverter switches should change their states instantaneously when the controlled current touches the upper and lower bands. HBCC generates a sinusoidal reference current of desired magnitude and frequency that is compared with the actual line current

If (i_{act}) > (i_{ref} + HB) upper switch of a leg is ON and lower switch is OFF.

If (i_{act}) < (i_{ref} - HB) upper switch of a leg is OFF and lower switch is ON.

If the current exceeds the upper limit of hysteresis band then upper switch is turned off and lower switch is turned on similarly when it exceeds the lower limit of hysteresis band then lower switch is turned off and upper switch is turned on. As a result current raises and decays .Thus actual current is forced to track the reference current within the hysteresis band.

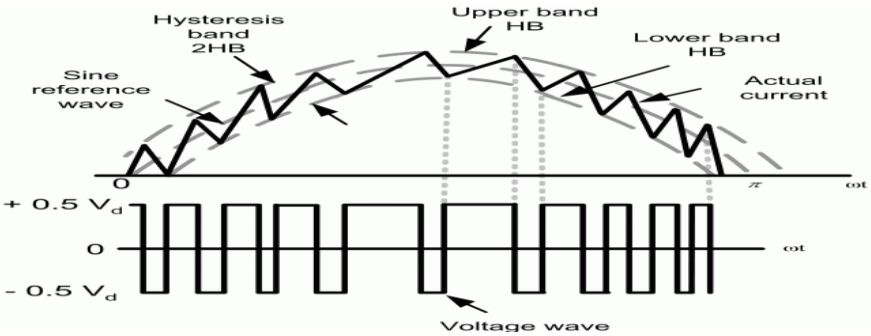

Fig. 4. Hysteresis Band Current Controller

B. SPWM

Variable switching frequency and high ripple content are disadvantages of HBCC. In order to overcome that we go for SPWM. In this the pulse are generated by comparing a triangular carrier waveform with reference modulating signal.

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The amplitude, phase and frequency of the reference signal are set to control the output voltage. The modulating signal is the compensating voltage. The triangular carrier signal is compared with the sinusoidal modulating signal. When the modulating signal is greater than carrier pulse then upper switch of VSI is on and lower switch is off .The range of switching frequency is (5 kHz-20 kHz).

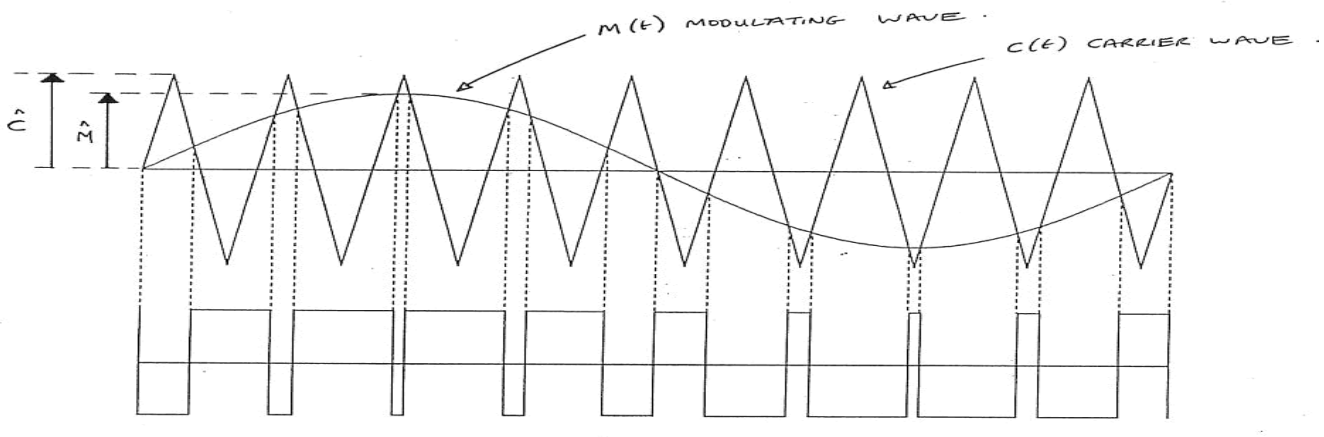

Fig. 5. Sinusoidal pulse width modulation

V. DESIGN SPECIFICATIONS

Design parameters of UPQC*:* DC bus voltage, DC bus capacitance, voltage rating of series active power filter, KVA rating of transformer and filter design.

A. DC capacitor voltage*:* The DC capacitor voltage is calculated based on following relation

$$V_{dc}=(2\sqrt{2}*V_{LL})/\sqrt{(3*m)} \quad \rightarrow (10)$$

Where m is modulation index (m=1)

B .DC bus capacitance of the VSC: The DC bus capacitance is calculated based on the energy required during the Change in load, it is calculated as

$$E=1/2*C_{dc}(V_{dc1}^2-V_{dc}^2) \quad \rightarrow (11)$$

Where V_{dc} is DC bus voltage and V_{dc1} is the minimum voltage level of DC bus

$$V_{dc1}=(2*V_s) \quad \rightarrow (12)$$

$$P*\Delta t=1/2*C_{dc}(V_{dc1}^2-V_{dc}^2) \qquad \text{Where } P=3*V_s*I_s \quad \rightarrow (13)$$

C. Voltage rating of series active power filter: The voltage rating of VSC depends on maximum voltage to be injected if there are any voltage variations in the load. .The injected voltage is calculated as a

$$V_{inj}=\sqrt{(V_s^2-V_L^2)}=V_{DVR} \quad \rightarrow (14)$$

D. KVA rating of transformer: The KVA rating of transformer is calculated as

$$S=(3V_s*I_s)/1000 \quad \rightarrow (15)$$

E. Ripple Filter: In order to eliminate the switching frequency ripples from injected voltage the ripple filter is designed.

Ripple filter consists a series connected R_r and C_r.

$$F_r=1/(2\pi*R_r*C_r) \quad \rightarrow (16)$$

Where f_r is taken as half of the Switching frequency. The range of switching frequency is from 5KHz – 20KHz.

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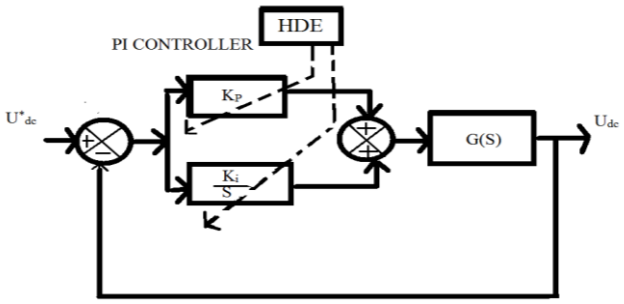
VI. HDE

The one-to-one competition of DE provides a faster convergence speed; this faster convergence yields a premature convergence. This drawback could be overcome by employing a larger population. However, by doing so, much more computation time is required to estimate the fitness function. In order to avoid employing a large population, Hybrid Differential Evolution (HDE) algorithms were developed. Warren Liao (2010) proposed hybrid differential algorithm. The fitness function is defined as

$$F = F(\text{THD of source current}) + F(\text{THD of load voltage}) + F(\text{sag}) \quad \rightarrow (17)$$

The optimization parameters are K_p and K_i values of PI controller. Where K_p and K_i are referred as proportional and integral gains respectively. The transfer function of PI controller is represented as follows.

$$K_C(S) = K_P + \frac{KI}{s} \quad \rightarrow (18)$$



The following is the procedure

A. Initialization : First initialize the population size, decision variables, fitness function

$$X_i^0 = X_{min} + \rho_i(X_{max} - X_{min}), \quad i=1,.....N_p \quad \rightarrow (19)$$

where $\rho i \in [0, 1]$ is a random number. The intial process produces N_P individuals of X_i^0 randomly

B. Mutation: The main aim of mutation process is to generate mutant vector. A mutant vector is generated based on the present individual X_i^G as fallows

$$Y_i^{G+1} = X_i^G + F((X_{r1}^G - X_{r2}^G) + (X_{r3}^G - X_{r4}^G)) \quad \rightarrow (20)$$

where $i = 1,2,3\ldots\ldots N_P$; r_1, r_2, r_3 and r_4 randomly selected and are distinct; $F \in [0,2]$ where F is the mutation rate and it is determined empirically.

C. Cross Over: The parent vector is mixed with the mutant vector to generate trial vector(offspring). The process of mixing parent vector with mutant vector is known as cross over.

$$Y_i^{G+1} = \begin{cases} X_{hi}^G, & \text{if a random number} > C_r \\ Y_{hi}^{G+1}, & \text{otherwise} \end{cases} \quad \rightarrow (21)$$

where $i = 1,2,3\ldots\ldots N_P$; $h = 1,2\ldots\ldots n_c$; where n_C is the dimension of decision parameters; Y_i^{G+1}, X_i^G are mutant and parent vectors; K is the number of genes $C_r \in [0,1]$ where C_r is the cross over constant that controls diversity of population.

D. Estimation and Selection: The parent is replaced by its offspring if the fitness of the offspring is better than that of the parent else the parent is retained for the next generation.

$$X_{hi}^{G+1} = \arg\min\{F(X_i^G), F(Y_i^{G+1})\} \quad \rightarrow (22)$$

$$X_b^{G+1} = \arg\min\{F(X_i^{G+1})\} \quad \rightarrow (23)$$

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where arg min means the argument of the minimum , and X_b^{G+1} is the best individual.

E. Migration:To regenerate a new diverse population, to effectively enhance the investigation and reduce the pressure to a small population we go for migration operation**.** The new populations are produced based on the best individuals X_b^{G+1}. The h^{th} gene of the i^{th} individual as fallows.

$$X_{hi}^{G+1} = \begin{cases} X_{hb}^{G+1} + P_i(X_{kmin} - X_{hb}^{G+1}) & \text{,if } P_2 < \dfrac{X_{hi}^{G+1} - X_{hmin}}{X_{hmin} - X_{hb}^{G+1}} \\ X_{hb}^{G+1} + P_i(X_{kmax} - X_{hb}^{G+1}) & \text{,otherwise} \end{cases} \rightarrow (24)$$

where ρ , ρ_2 are randomly generated numbers uniformly distributed in the range of [0,1]; i =1,2,3……N_P; h= 1,2……n_c; The migration in DE is executed only if a measure fails to match the desired steadiness of population diversity. The measure is defined as fallows.

$$P = \sum_{\substack{i=1 \\ i=b}}^{N} \sum_{j=1}^{N} X_j / n_c(N_P - 1) < \varepsilon_{i\,i} \rightarrow (25)$$

$$X_{ji} = \begin{cases} 1, \text{ if } X_{ji}^{G+1} - X_{jb}^{G+1} \\ 0, \text{otherwise} \end{cases}$$

$\varepsilon_1 \in [0,1]$ $\varepsilon_2 \in [0,1]$ Respectively express the desired steadiness for the population diversity and the gene diversity with respect to the best individual.

F. Repeat from B to E until desired THD is reached

VII. SIMULATION RESULTS

This the basic Simulink diagram showing how the power quality disturbances are created. Voltage sag is created with the help of programmable source by decreasing the input of step during the interval (0.05-0.1). Similarly current harmonics are created with the help of non-linear load.

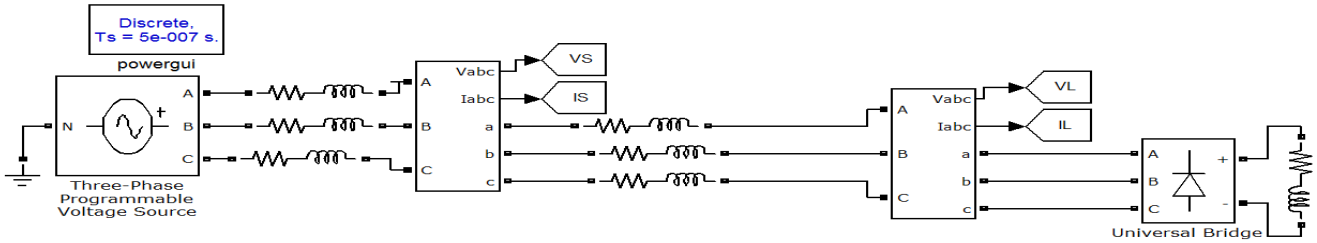

Fig. 6. Simulink diagram of basic distribution line

Since voltage sag is created with the help of programmable source there is a dip in voltage source. As impedance is constant, voltage is directly proportional to current so there is also a dip in the current waveform during that interval of time. Since non-linear load injects harmonics there is distortion in the current waveform.

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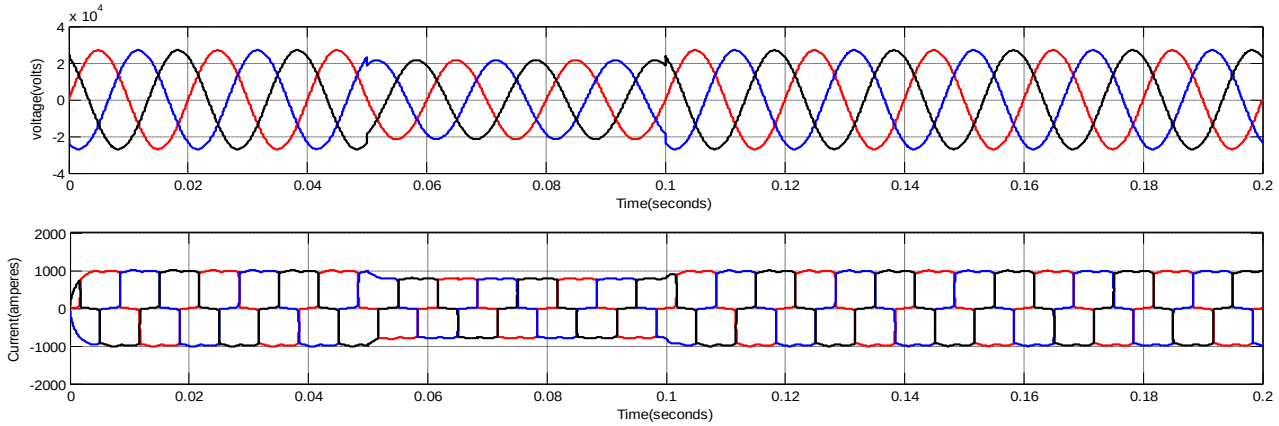

. Fig. 7. Source current and load voltage waveform before UPQC

UPQC is a most versatile device that can mitigate current harmonics and voltage sags. It comprises of DVR and STATCOM integrated with the help of a DC-link capacitor. The STATCOM is connected in shunt with the line and DVR is connected in series with the line with the help of series transformer.

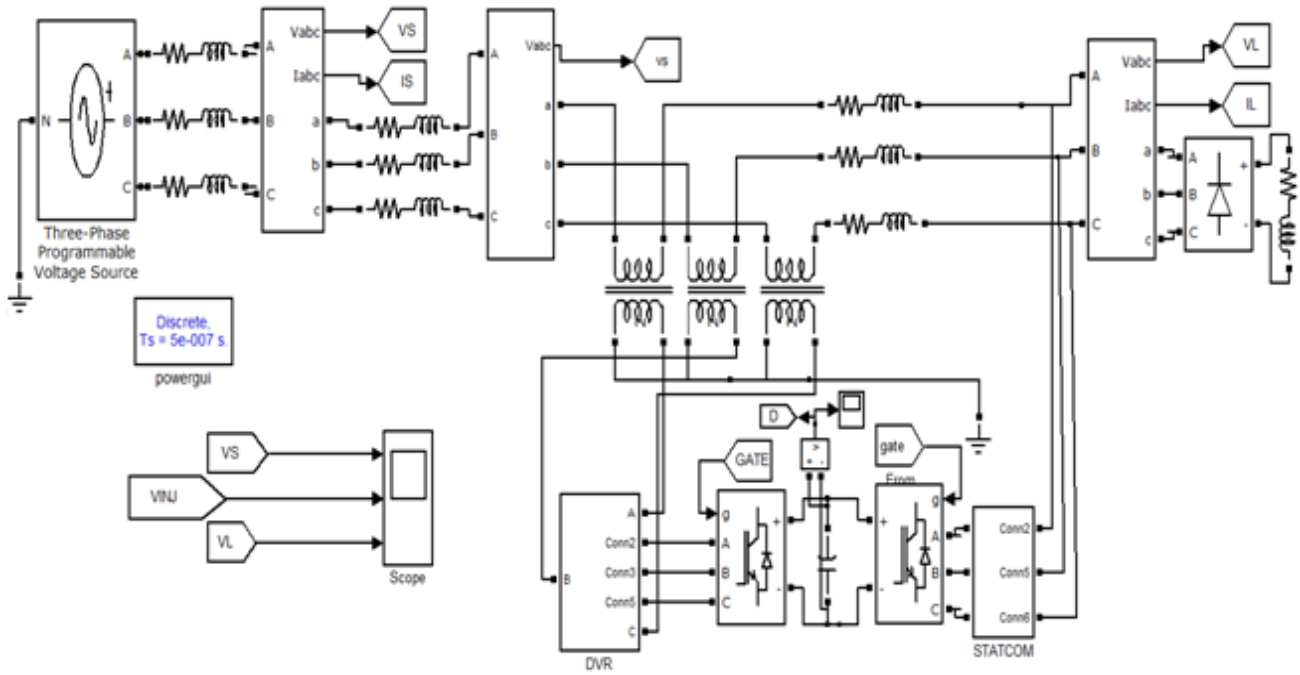

Fig. 8.Simulink diagram of UPQC

UPQC is applied to the basic distribution line the reference currents and voltages are generated using SRF theory. The gating pulses to the inverter are generated with the help of Hysteresis Band Current Controller.

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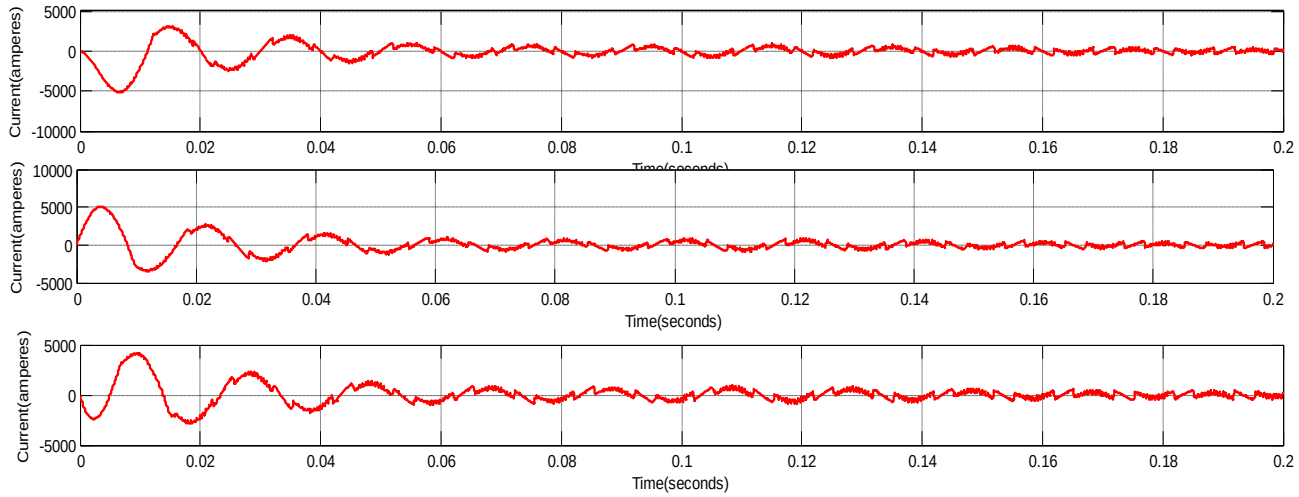

Fig. 9. Injected currents using UPQC

The UPQC injects opposite harmonics into the line and cancel out the harmonic currents present in the source current and helps it to maintain the source current harmonic free. These reverse harmonics are generated with the help of SRF control strategy using HBCC.

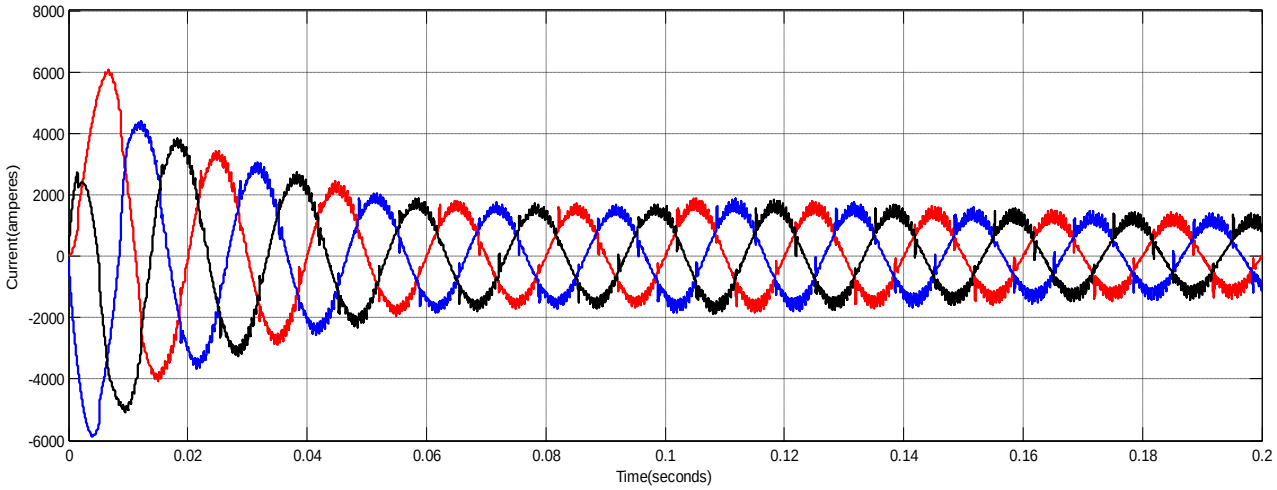

Fig. 10.Source current after the application of UPQC

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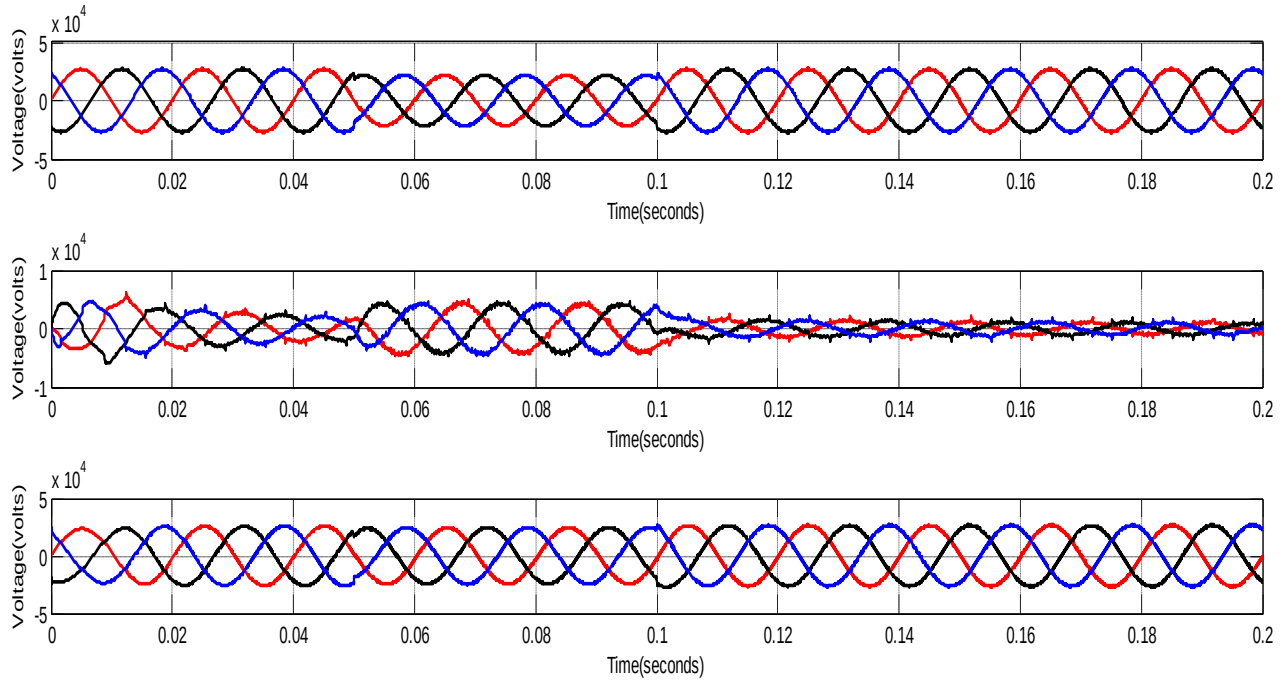

Fig. 11.Source injected and load voltages using UPQC

The UPQC compensates the voltage sag by injecting the voltage during sag interval of time. The compensated voltages are generated using SRF theory based on SPWM technique. Thus the UPQC mitigates current harmonics and compensate voltage sags.

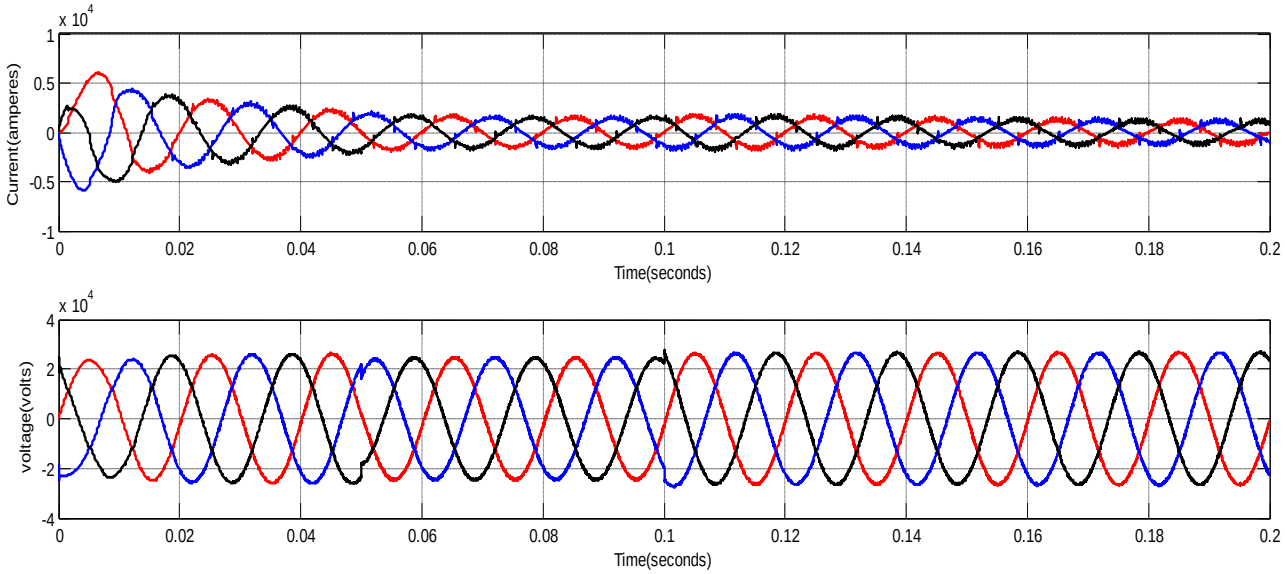

Fig. 12. Source current and load voltage after application of UPQC

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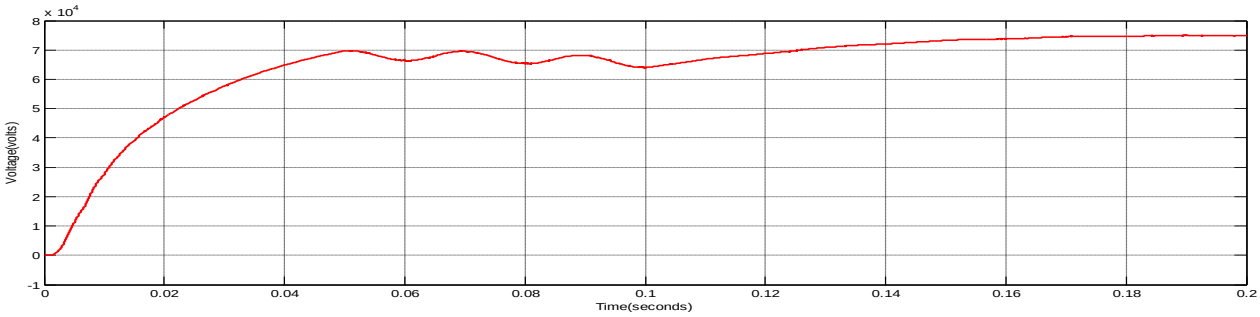

Fig. 13.DC link voltage

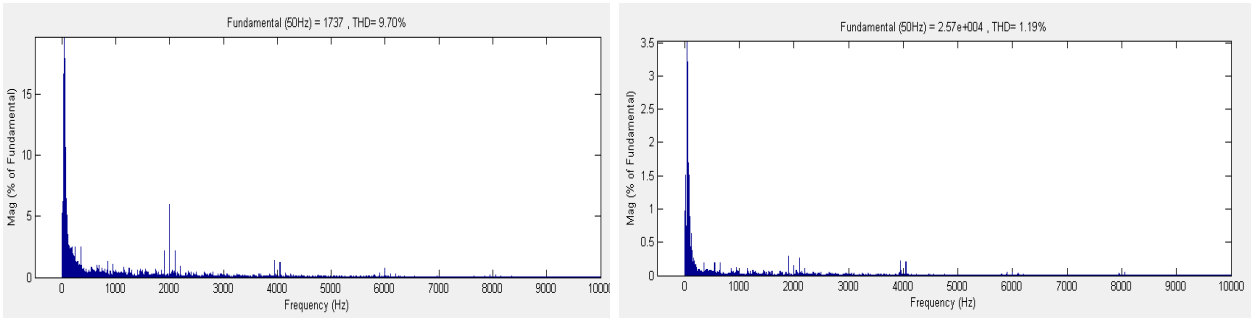

Fig. 15 T.H.D of source current and load voltage using PI controller from FFT analysis

It is difficult to change the PI parameters regularly and verify the T.H.D. In order to find the optimal values of K_p and K_I, the PI controller is optimized with HDE technique.

By taking objective function as F = F (THD of source current) ; For 20 iterations for C_R =0.6;F=0.9 The T.H.D has been reduced to 0.0564%

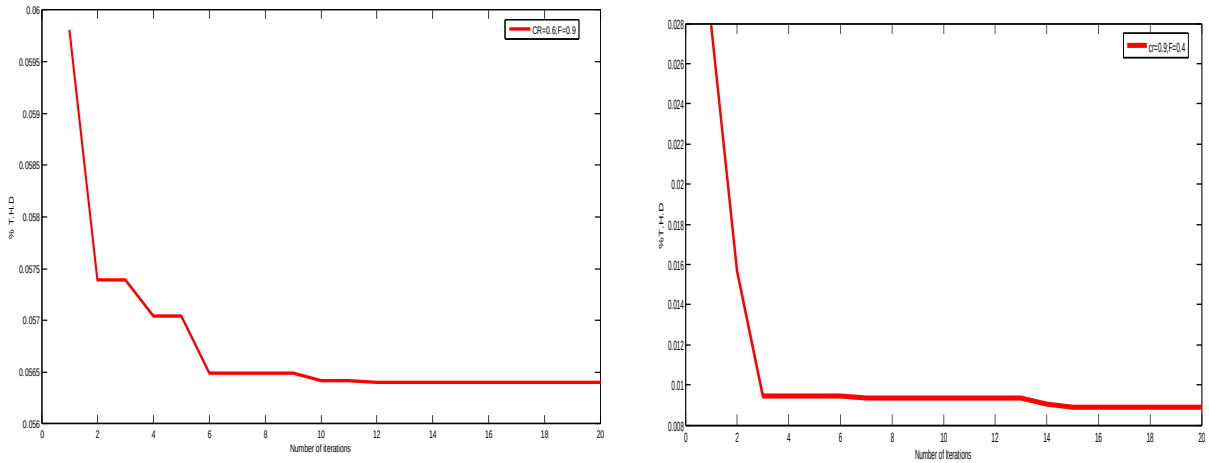

Fig. 15 T.H.D of source current and load voltage using PI-HDE from convergence graph

By taking objective function as F = F (THD of load voltage) ; For 20 iterations for C_R =0.9;F=0.4 The T.H.D has been reduced to 0.00890%

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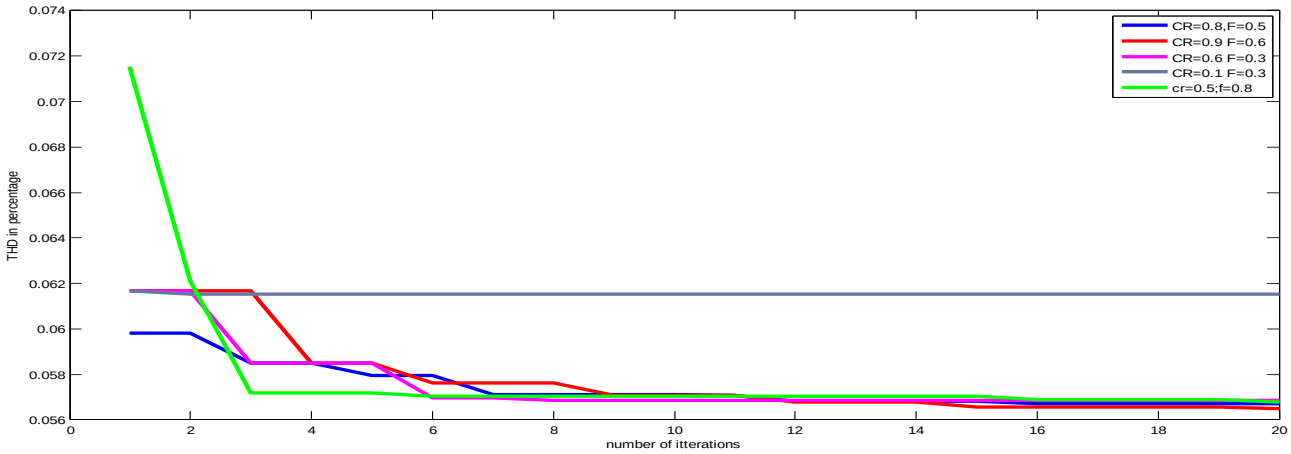

Fig. 16. Convergence graph for multi objective function

The multi objective function is F = F(THD of source current)+F(THD of load voltage)+F(sag)

Source Current	%T.H.D
PI Controller	9.70
PI-HDE(C_R =0.6;F=0.9)	0.0564

Load Voltage	%T.H.D
PI controller	1.28
PI-HDE(C_R =0.9;F=0.4)	0.0089

VIII. CONCLUSION

The Power Quality disturbances such as current harmonics and voltage sag are mitigated and compensated with the help of UPQC. Comparative analysis has been made on UPQC with conventional PI controller and PI controller optimized with HDE (PI-HDE) by taking different objective functions. It has been found that PI controller optimized with HDE gives better results than conventional PI controller when THD of source current and THD of load voltage are taken independently as objective function. By taking multi objective function as THD of source current, THD of load voltage and sag the overall THD reduces to a small value.

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