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A Study of Multilevel Inverter Topologies

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ABSTRACT: Inverter is a power electronic device which converts dc power into ac power at required voltage and frequency. Today need of inverter has been increased due to its industrial and home applications. In industries various range of motor drives and utility are available, some required medium voltage and megawatt power level. For simple two-level inverter topology it is difficult to fulfilled requirement of medium voltage in industries. To overcome this multilevel inverter have been introduced and attracting in favor of academia as well as industry in the recent decade for high-power and medium-voltage energy control. Multilevel inverter is also used to decrease the harmonic distortion in the output waveform without decreasing the inverter power output. This paper presents different topologies of multilevel inverter and Matlab Simulink model of cascaded H-Bridge inverter.

KEYWORDS: Multilevel inverter, topologies, cascaded H-bridge inverter, MATLAB/SIMULINK.

I.INTRODUCTION

Development in industrial revolution has been increased rapidly in all over the world. And suitable voltage, current and frequency are minimal requirement of any industrial utility for better power quality. Inverter is device which provide continues and quality power supply to utilities, from small supplies for a computer to large industrial application to transport bulk power. But some medium voltage motor drives and utility applications require medium voltage and megawatt power. Due to this multilevel inverter has been introduced as an alternative in high power and medium voltage situation. Also inverter output waveforms (either voltage or current) are usually rectilinear in nature and as such contain harmonics which may lead to reduced load efficiency and performances. So many researches had done on inverter until now. From these researches it is observe that multilevel inverter reduces the total harmonic distortion (THD) [2]. Multilevel inverter not only used for high power rating but also enables the use of renewable energy sources such as photovoltaic, wind and fuel cell[11]. Various modeling and simulation of multilevel inverter is carried out until now [2][3][4][6]. Multilevel inverters usually operate on pulse width modulation (PWM) technique. PWM is very advance and useful technique in which width of the Gate pulses are controlled by various mechanisms. This paper presents most important topologies like diode clamped (neutral point), capacitor clamped (flying capacitor) and cascaded H-bridge multilevel inverter. It also presents modeling of cascaded H-bridge multilevel inverter with output waveforms using soft tool MATLAB/SIMULINK.

II. MULTILEVEL INVERTER TOPOLOGIES

Multilevel inverter consists of three main topologies. First one is diode clamped multilevel inverter or neutral point clamped (NPC) inverter which was introduced in 1981, second one is capacitor-clamped or flying capacitor multilevel inverter which was introduced in 1992 and the third one is cascaded H-bridge multilevel inverter which was introduced in 1996. Although cascaded multilevel inverter was invented earlier when the concept of multilevel inverter has introduced in 1975, but its application was not powerful until the mid 1990s [2].

A. DIODE CLAMPED (NPC) INVERTER

The main concept of this inverter is to use diodes to limit the power devices voltage stress. In which the diode is used as the clamping device to clamp the dc bus voltage so as to achieve steps in the output voltage. The voltage over each capacitor and each switch is Vdc.

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An n level inverter required (n-1) voltage sources, 2(n-1) switching devices and (n-1) (n-2) diodes. By increasing the number of voltage levels the quality of the output voltage is improved and the voltage waveform becomes closer to sinusoidal waveform. Figure.1.a) shows a three-level diode-clamped converter in which the dc bus consists of two capacitors, C1, C2. For dc-bus voltage Vdc, the voltage across each capacitor is Vdc/2 and each device voltage stress will be limited to one capacitor voltage level Vdc/2 through clamping diodes. To explain how the staircase voltage is synthesized, the neutral point n is considered as the output phase voltage reference point. There are three switch combinations to synthesize three-level voltages across a and n.

1. Voltage level Van= Vdc/2, turn on the switches S1andS2
2. Voltage level Van= 0, turn on the switches S2 and S1′.
3. Voltage level Van= - Vdc/2 turn on the switches S1′,S2′.

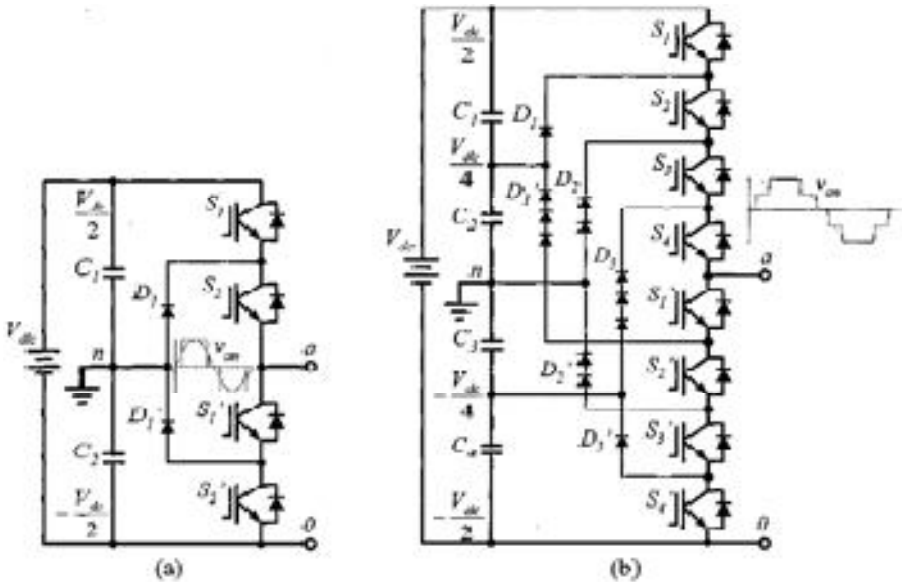

Figure: 1. Diode clamped multilevel inverter topologies (a) three level (b) five level

Figure.1 (b) shows a five-level diode-clamped converter in which the dc bus consists of four capacitors, C1, C2, C3, and C4. For dc-bus voltage Vdc, the voltage across each capacitor is Vdc/4 and each device voltage stress will be limited to one capacitor voltage level Vdc/4 through clamping diodes.

To synthesize 5-level output phase voltage, switching sequence as given in table 1. State condition 1 means switch ON and 0 means switch OFF.

Voltage V_{ao}	Switch State							
	S1	S2	S3	S4	S1’	S2’	S3’	S4’
Vdc	1	1	1	1	0	0	0	0
Vdc/2	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
-Vdc/2	0	0	0	1	1	1	1	0
-Vdc	0	0	0	0	1	1	1	1

Table1: Switching states in one leg of the five-level diode clamped inverter.

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Diode clamped multilevel inverters are used in conventional high power ac motor drive application like conveyers, pumps, fans and mills. They are also utilized in oil, gas, metals, power, mining, water, marine and chemical industries [4].

B. CAPACITOR CLAMPED INVERTER

Topology of capacitor clamped inverter is similar to that of diode clamped except that instead of diodes, uses capacitor in this topology. The flying capacitor involves series connection of capacitor clamped switching cells. An n level inverter will require a total (n-1) (n-2)/2 clamping capacitors per phase leg in addition to (n-1) main dc bus capacitors**.** The voltage synthesis in a five-level capacitor-clamped converter has more flexibility than a diode-clamped converter. For an n-level inverter, the voltage stress across each main device is same and is equal to Vdc / (n-1). Figure 2(b) synthesized the voltage of the five-level phase-leg "a" output with respect to the neutral point n (i.e. Van), following can be the switch combinations.

1. Voltage level Van= Vdc/2, turn on all upper switches S1 - S4 .
2. Voltage level Van=Vdc/4, there are three combinations.
    a. Turn on switches S1, S2, S3 and S1′.(Van= Vdc/2 of upper C4"s - Vdc/4 of C1"s).
    b. Turn on switches S2, S3, S4 and S4′.(Van= 3Vdc/4 of upper C3"s - Vdc/2 of C4"s).
    c. Turn on switches S1, S3, S4 and S3′. (Van= Vdc/2 of upper C4"s - 3Vdc/4 of C3"s + Vdc/2 of upper C„).
3. Voltage level Van= 0, turn on upper switches S3 , S4 , and lower switch S1′, S2′.
4. Voltage level Van= -Vdc/4, turn on upper switch S1 and lower switches S1′, S2′and S3′.
5. Voltage level Van= -Vdc/2, turn on all lower switches S1′, S2′, S3′ and S4′.

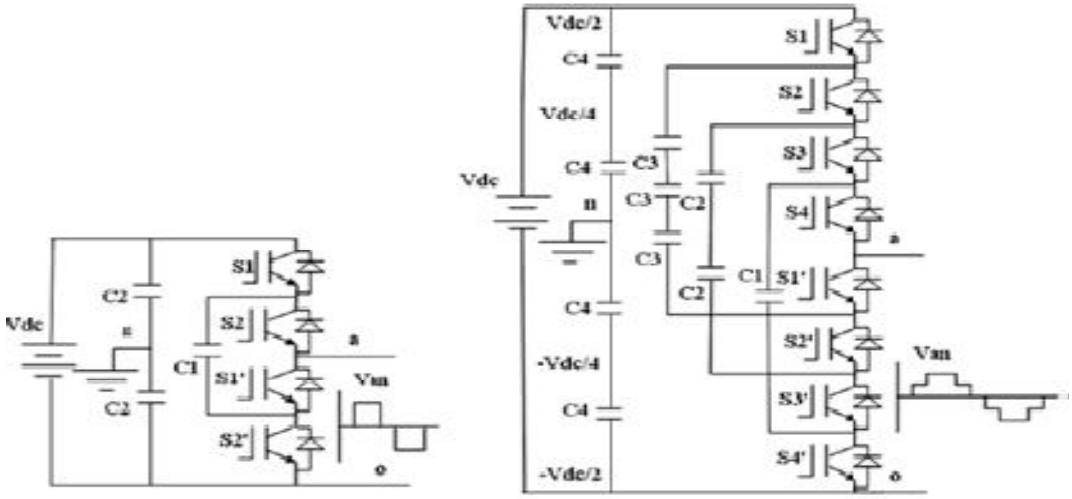

Figure.2: Capacitor-Clamped Multilevel Inverter Circuit Topologies, (a) 3-Level Inverter (b) 5- Level Inverter.

Capacitor clamped inverters have been used in high-bandwidth high-switching frequency applications such as medium-voltage traction devices [4]. Disadvantage of this is only that required large number of capacitors.

C.CASCADED H-BRIDGE MULTILEVEL INVERTER

The concept of this inverter is based on connecting H-bridge inverters in series to get a sinusoidal voltage output. The output voltage is the sum of the voltage that is generated by each cell. Each H-Bridge inverter circuit consists of four active switching elements that can make the output voltage either positive or negative polarity or simply zero which is depend on switching condition of switches in the circuit. The number of output voltage levels required are 2n+1, where *n* is the number of cells. The number of controlled switches required in this topology is 4n. The switching angles can be chosen in such a way that the total harmonic distortion is minimized.

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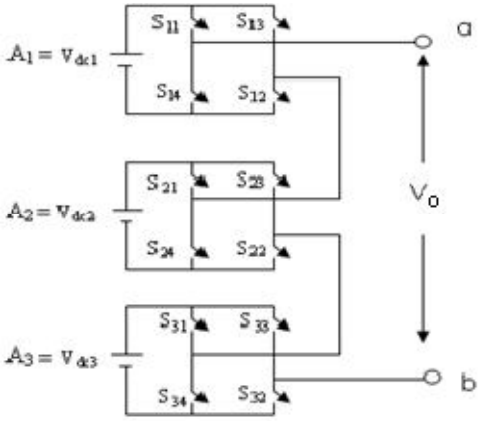

Figure.3. Topology for cascaded Multilevel Inverter.

One of the advantages of this type of multilevel inverter is that it needs less number of components comparative to the Diode clamped or the flying capacitor, so the price and the weight of the inverter is less than that of the two types.

Number of switches required in cascaded multilevel inverter can again reduced by adopting modified cascaded multilevel inverter in which number of switches are equal to number of level [4] [11]. For example seven-level inverter required only seven switches instead of twelve switches. This modified cascaded multilevel inverter reduces the complexity of control circuit; cost, lower order harmonics means reduces THD.

III. MATLAB SIMULINK MODEL

Modeling of five-level cascaded H-bridge inverter is carried out in MATLAB/SIMULINK software. In this modeling sinusoidal PWM technique is used for modulation. Here MOSFET based inverter simulation is carried out.

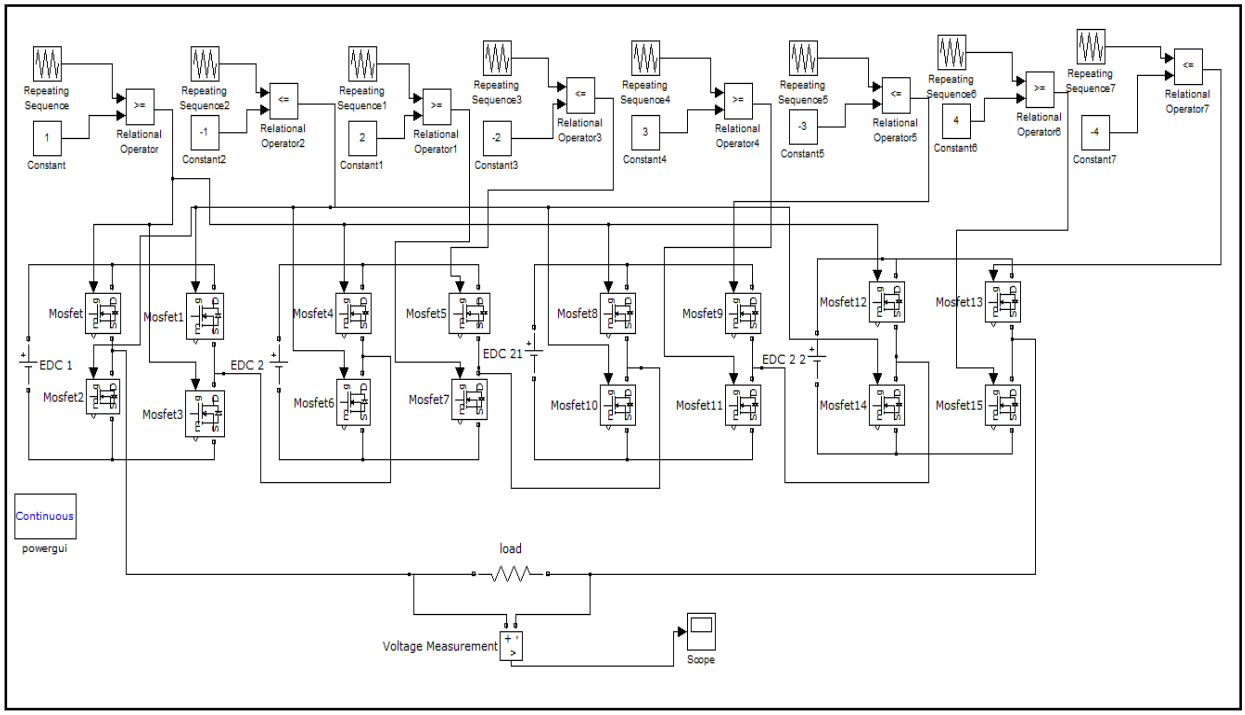

Fig.4. Simulation model of five-level MOSFET based inverter

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IV.SIMULATION RESULT

In this paper different multilevel inverter topologies has been studied. And along with that simulation of cascaded H-bridge five-level inverter is carried out in MATLAB/SIMULINK. Output waveform of load voltage is obtained from scope shown in simulation model (Fig. 4). Fig. 5 shows output waveform of load voltage obtained.

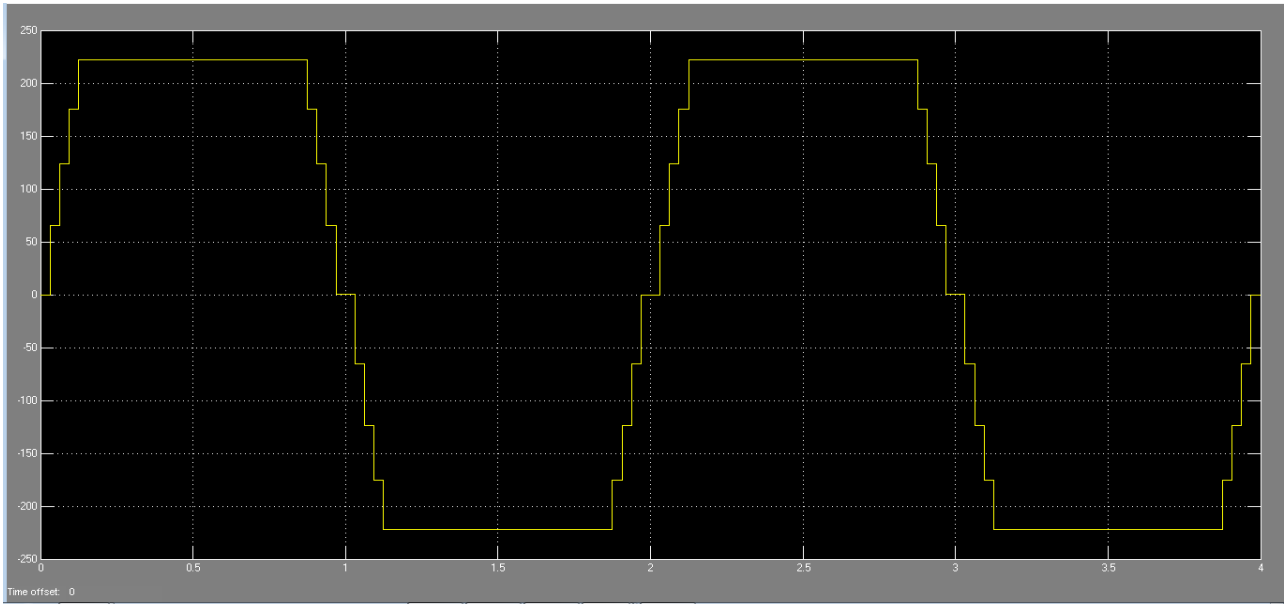

Fig.5. Waveform of output load voltage

VI.CONCLUSION

This paper gives overview of different multilevel inverter topologies. Simulation of five-level cascaded inverter is carried out in MATLAB/SIMULINK and waveform of output load voltage is shown in figure.5. In future modelling of multilevel inverter can be carried out using different semiconductor switches such as IGBT and GTO.

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