ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 6, June 2015

Convolution and Deconvolution Using Vedic Mathematics

N. R. Punwantwar[1], Dr. P. N. Chatur[2]

PG Student [ESC], Dept. of ECE, Government College of Engineering, Amravati, Maharashtra, India[1]

Head of Department, Dept. of ECE, Government College of Engineering, Amravati, Maharashtra, India[2]

ABSTRACT: Convolution and Deconvolution is having wide area of application in Digital Signal Processing. As in DSP Convolution and Deconvolution of long sequences is often required in many applications. Convolution helps to estimate the output of a system with arbitrary input, with knowledge of impulse response of the system. Linear systems characteristics are completely specified by the systems impulse response, as governed by the mathematics of convolution. Primary requirement of any application to work fast is that increase the speed of their basic building block. Multiplier and Divider is the heart of convolution and Deconvolution respectively. It is most important but, slowest unit of the system and consumes much time in the system. Many methods are invented to improve the speed of the Multiplier and Divider, amongst all vedic Multiplier and Divider is under focus. Because, of faster working and low power consumption. In this paper the speed of Convolution and Deconvolution module is increased using Vedic multiplier and Divider.

KEYWORDS: Linear Convolution, Deconvolution, Vedic Mathematics, Urdhva Tiryagbhyam sutra, Paravartya sutra, Nikhilam sutra.

I. INTRODUCTION

With continuous advancement in VLSI technology, Need of high speed convolution and Deconvolution is required. as many areas of Electrical and Electronics Engineering, Digital signal processing plays an important role, Discrete Convolution and Deconvolutionis having extreme importance in Digital signal processing. Convolution is having wide area of application like designing the digital filter, correlation etc.

However it is quite difficult for the new candidate to perform convolution as convolution method is so lengthy and time consuming. So many methods are proposed for performing Discrete Convolution, one of a tough approach is a Graphical method, it is quite sophisticated and systematic but, it is very lengthy and time consuming [1]. The main module for performing Convolution and Deconvolution is Multiplier and Divider. Pierre and John have implemented the fast method for performing linear convolution. This method is very easy, it is like to perform simple multiplication of Decimal numbers [2]. And because of this method in very little time it is possible to calculate Convolution of long sequences is very easily. Also a Novel method is used for performing Deconvolution. This method is similar to calculate long division and polynomial division. As Adder is also an important block for the proposed method, so all the possible adders is studied and synthesized using Altera Quartus II design suit. The Delay and Area of all adders is compared. Amongst all Adder which having highest speed and occupy less area is used for performing convolution. For the conventional multiplication, multipliers with Traditional shifts and add method is used. This method is difficult for VLSI implementation and also its Delay is too large. Vedic mathematics provides the unique solution for Multiplication and Division. Vedic Multiplier based on urdhava tiryagbhyam sutra (Vertically and Crosswise) is used to implement Convolution. For Deconvolution various Divider is Studied, by comparing the advantages and disadvantages of each method, Divider using Paravartya Sutra is used for implementation.

II. VEDIC MATHEMATICS

The word 'Vedic' is derived from the word 'veda' which means the store-house of all knowledge. We must be thankful to Jagadguru Swami Sri Bharati Krishna Tirthaji Maharaja to introduce Vedic Mathematics and acknowledge

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 6, June 2015

the work of various people regarding Vedic Mathematics. Vedic mathematics is mainly based on 16 Sutras. These sutras along with their brief meaning are enlisted below alphabetically [12].

1. Anurupye Shunyamanyat– If one is in ratio, the other is zero
2. Chalana-Kalanabyham– Differences and Similarities
3. Ekadhikina Purvena– By one more than the previous one
4. Ekanyunena Purvena– By one less than the previous one
5. Gunakasamuchyah- The Factor of the sum is equal to the sum of Factor
6. Gunitasamuchyah- The product of sum is equal sum of product
7. Nikhilam Navatashcaramam Dashatah– All from 9 and the last from 10
8. Paraavartya Yojayet– Transpose and adjust
9. Puranapuranabyham– By the completion or noncompletion.
10. Sankalana-vyavakalanabhyam– By addition and by subtraction
11. Shesanyankena Charamena– The remainders by the last digit
12. Shunyam Saamyasamuccaye– When the sum is the same that sum is zero
13. Sopaantyadvayamantyam– The ultimate and twice the penultimate
14. Urdhva Tiryagbyham– Vertically and crosswise
15. Vyashtisamanstih– Part and Whole
16. Yaavadunam– Whatever the extent to fits deficiency

III. CONVOLUTION METHOD

Convolution is considered to be heart of the digital signal processing. It is the mathematical way of combining two signals to obtain a third signal. Convolution helps to estimate the output of a system with arbitrary input, with knowledge of impulse response of the system. Linear systems characteristics are completely specified by the systems impulse response, as governed by the mathematics of convolution. Convolution is an operation which takes two functions as input, and produces a single function output (much like addition or multiplication of functions)
The Convolution of two Discrete Sequences is given by [3]

$$Y(n) = x(n) * h(n) \qquad (1)$$

$$Y(n) = \sum_{k=-\infty}^{\infty} x(k)h(n-k) \qquad (2)$$

Consider the example, let x(n) is finite length sequence (4,5,3,1) and h(n) equal to finite length sequence (2,7,9,3). The linear convolution of x(n) and h(n) can be solved by several method, resulting in the sequence

$$Y(n) = (\ 8,38,77,80,49,18,3)$$

Performing convolution using graphical method or formula based method is easy but it is quite lengthy and takes more time for calculation, again it is difficult to implement therefore among all the method given by john pierra easy to compute and implement, it is set up like conventional multiplication. Where the convolution of x(n) and h(n) is as shown in fig1.

As shown in the fig1 calculation of convolution sum is very easy using john perra method, it is like performing multiplication except the carry is not propagated out the column.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 6, June 2015

Example 1:

x(n):		4	5	3	1			
	*							
h(n):		2	7	9	3			
		8	10	6	2			
			28	35	21	7		
				36	45	27	9	
					12	15	9	3
Y(n):		8	38	77	80	49	18	3

Fig:1 Convolution by Proposed Method

IV. DECONVOLUTION METHOD

Deconvolution is an operation which takes two functions one input is convolved sequence y(n) where as other input is h(n) , and produces a single function output x(n).For Deconvolution a direct method is presented for performing Deconvolution of two finite length sequences. This method is similar to performing long division and polynomial division. The basic recursive Deconvoltion method is used for finding Deconvoltion of finite length sequences. The recursion method works similar to performing long division [10]. To illustrate the method further Consider the example 2, let Y(n) be the convolved sequence equal to (8,38,77,80,49,18,3) and h(n) be the finite length sequence equal to (2,7,9,3). Performing Deconvolution resulting

$$x(n)= (4,5,3,1)$$

The Deconvolution of finite length sequences Y(n) and h(n) using recursion method as shown below

Example2:

				4	5	3	1	⟶	x(n)
2	7	9	3	8	38	77	80	49	18	3
				8	28	36	12			
				0	10	41	68	49	18	3
					10	35	45	15		
					0	6	23	34	18	3
						6	21	27	9	3
						0	2	7	9	3
							2	7	9	3
							0	0	0	0

Fig.2. Deconvolution by Recursion Method

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 6, June 2015

V. VEDIC MULTIPLIER

In this paper a systematic Vedic multiplier using Urdhava Tiryagbhyam sutra is used for multiplication. Among all multiplier this Vedic multiplier performs faster multiplication and occupies less area. In the proposed convolution method the Multiplier is based on Urdhava Tiryagbhyam(vertically and crosswise).

Vedic mathematics provides easiest way to perform multiplication. It reduces the typical calculation which is difficult to compute using conventional multiplier. Urdhava Tiryagbhyam is general multiplication formula applicable for all types of multiplication. The parallelism in generation of partial product improves the speed of multiplication. For computing big multiplication of N X N, the number is divided in to small blocks and utilize for design. For higher number of bit some modification is required. Divide the number in to two equal parts. Let's analyse 4 x 4 multiplication, Say $X_3X_2X_1X_0$ and $Y_3\,Y_2\,Y_1\,Y_0$. The result of multiplication of these two numbers is given by $M_7\,M_6\,M_5\,M_4\,M_3\,M_2\,M_1\,M_0$. Let's divide the X and Y in to two parts say $X_3\ X_2$ and $X_1\ X_0$ for X and $Y_3\ Y_2$ and $Y_1\ Y_0$ for Y. using the Vedic multiplication method consider 2 bit at a time and perform the multiplication on using 2 bit multiplier. The following structure shows the multiplication of 4 x 4 numbers using Vedic multiplier.

$$\begin{array}{rr} & X_3\ X_2 \quad X_1X_0 \\ X & \\ & Y_3\ Y_2 \quad Y_1\ Y_0 \\ \hline \end{array}$$

$$\begin{array}{|c|c|c|} \hline X_3\ X_2 \\ X \\ Y_3\ Y_2 \\ \hline \end{array} \quad \begin{array}{|c|c|c|} \hline X_3\ X_2 \\ X \\ Y_1\ Y_0 \\ \hline \end{array} \quad \begin{array}{|c|c|c|} \hline X_1\ X_0 \\ X \\ Y_3\ Y_2 \\ \hline \end{array}$$

$$\begin{array}{|c|c|c|} \hline X_1\ X_0 \\ X \\ Y_1\ Y_0 \\ \hline \end{array}$$

Fig 3. Block Diagram presentation for 4 X 4 Multiplication

Each block as shown above is 2 x 2 multiplier. $X_3\ X_2$ and $Y_3\ Y_2$ are given as input to first 2 x 2 multiplier.$X_3\ X_2$ and $Y_1\ Y_0$ is given as input to second block. $X_1\ X_0$ and $Y_3\ Y_2$ is given as input to the third block of multiplier. $X_1\ X_0$ and $Y_1\ Y_0$ is given as input to last block. The final result of multiplication is of 8 bit say $M_7\ M_6\ M_5\ M_4\ M_3\ M_2\ M_1\ M_0$, calculated as given below.

$$\begin{array}{r} X_3\ X_2 \\ Y_3\ Y_2 \\ \hline M_{33}M_{32}M_{31}M_{30} \end{array} \qquad \begin{array}{r} X_3\ X_2 \\ Y_1\ Y_0 \\ \hline M_{23}M_{22}M_{21}M_{20} \end{array} \qquad \begin{array}{r} X_1\ X_0 \\ Y_3\ Y_2 \\ \hline M_{13}M_{12}M_{11}M_{10} \end{array} \qquad \begin{array}{r} X_1\ X_0 \\ Y_1\ Y_0 \\ \hline M_{03}M_{02}M_{01}M_{00} \end{array}$$

Assuming the output of each multiplication is as given above. For the final result, the multiplication result of each 2x 2 multiplier block is arranged in specific manner as shown below. Add the middle product term along with the term shown below.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 6, June 2015

$$M_{33}\,M_{32} \quad M_{31}\;M_{30}\;\;0\;\;0\;\;M_{01}M_{00}$$

$$M_{23}\;M_{22}\;M_{21}\,M_{20}$$

$$M_{13}\;M_{12}\;M_{11}\,M_{10}$$

$$0\;\;0\;\;M_{03}\;M_{02}$$

The first two outputs M_0 and M_1 are same as that of M_{00} and M_{01}.one 4bit full adder is used to add the ($M_{23}\,M_{22}\,M_{21}\,M_{20}$) and ($M_{13}\,M_{12}\,M_{11}\,M_{10}$). The result of addition of first adder is added with the ($M_{31}\;M_{32}\,M_{03}\,M_{02}$). The result of addition of second full adder gives $M_5\;M_4\,M_3\,M_2$ bit of final multiplication. The carry generated during first full adder operation is added using half adder with carry generated during second full adder operation. The final sum and carry of half adder is added with $M_{33}\,M_{32}$ gives $M_7\,M_6$ bit of final multiplication result. The same method can be extended for 8, 16, 32 input bits.

VI. VEDIC DIVIDER

In this paper a systematic method is used for division which based on Paravartya Sutra. Paravartya Sutra help to minimize computation and maintain accuracy even as the number of iteration is reduced. It provides easier and logically simple implementation [9].

According to paravartya sutra, all the digit of the divisor is complemented except the most significant digit. This complemented digit is initially multiplied with the most significant digit of the dividend and this multiplication result is added with columns of dividend. The result of addition is again multiplied with complemented digits of Divisor and added with the remaining column of the dividend, followed successive multiplication and addition of consecutive column. The summation of all columns results forms quotient and remainder.

Implementation of the algorithm is illustrated using an example. Assume the dividend is 14589 and divisor is 132. The division of this two numbers using paravartya sutra is shown in fig.4.

Divisor			Dividend				
1	3	2	1	4	5	8	9
	-3	-2		-3	-2		
					-3	-2	
						0	0
			1	1	0	6	9
			Quotient = 110			Reminder = 69	

Fig 4. Division using paravartya sutra

VII. SIMULATION AND RESULT

The Vedic Convolution algorithm proposed in this paper is synthesized using Altera Quartus II 9.1 design suit with the device family Cyclone II and Device EP2C35F672C6. The table shows the synthesis report of the proposed work for Convolution using Vedic mathematics with logic source utilization.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 6, June 2015

Table I. Device Summary Utilization for Convolution

Logic Utilization	Used	Available	Utilization
No. of Slices	712	7,168	9%
No. of LUTs	384	3,584	10%
No. of Bounded IOBs	88	221	39%

The simulated result of Convolution using Vedic Multiplier are shown below

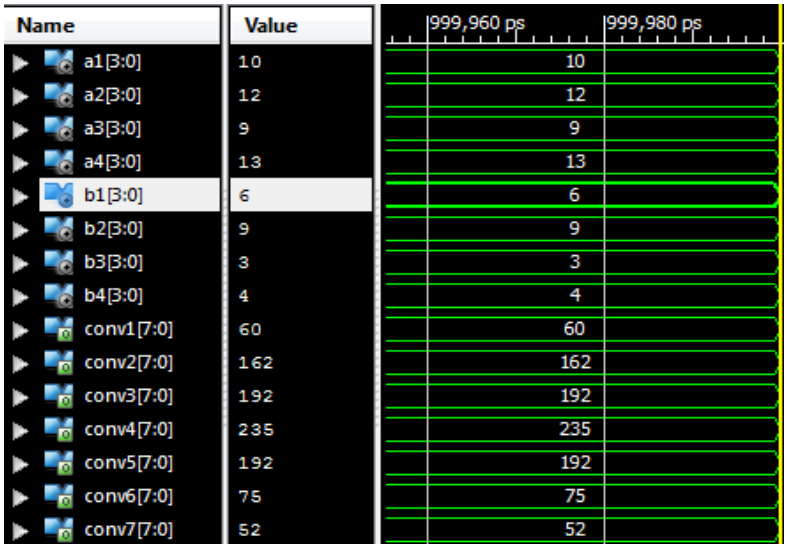

Fig.5. Simulation results of Convolution using Vedic mathematics

The Convolution module is simulated on Xilinx ISE simulator. The figure 5 shows the simulation result of Convolution module using Vedic Mathematics. A1, A2, A3, A4 and B1, B2, B3, B4 are the inputs of 4 bit each and conv1, conv2, conv3, conv4, conv5, conv6, conv7 are the outputs.

For Comparative Analysis of Conventional Method and Vedic method, the Convolution is implemented through Conventional multiplier and its delay is calculated and compare with the proposed Vedic Method as shown in table II.

Table II. comparison of Delay for Convolution using Vedic Mathematics versus conventinal method

Method	Delay
Conventinal method	27.784 ns
Proposed Vedic Method	20.433ns

Table II shows delay improvement of proposed circuit of convolution over the conventinal array multiplier.From the table it is clear that proposed method provides 28% improvement than conventinal method.

Simialar to convoltuion, Deconvolution using proposed method is also synthesize on Altera Quartus II 9.1 design suit with the device family Cyclone II and Device EP2C35F672C6. The table shows the synthesis report of the proposed work for Deconvolution using Vedic mathematics with logic source utilization.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 6, June 2015

Table III. Device Summary Utilization for Deconvolution

Logic Utilization	Used	Available	Utilization
No. of Slices	496	1,920	25%
No. of LUTs	265	960	27%
No. of Bounded IOBs	63	66	95%

The simulation result for Deconvolution using paravartya sutra is shown below

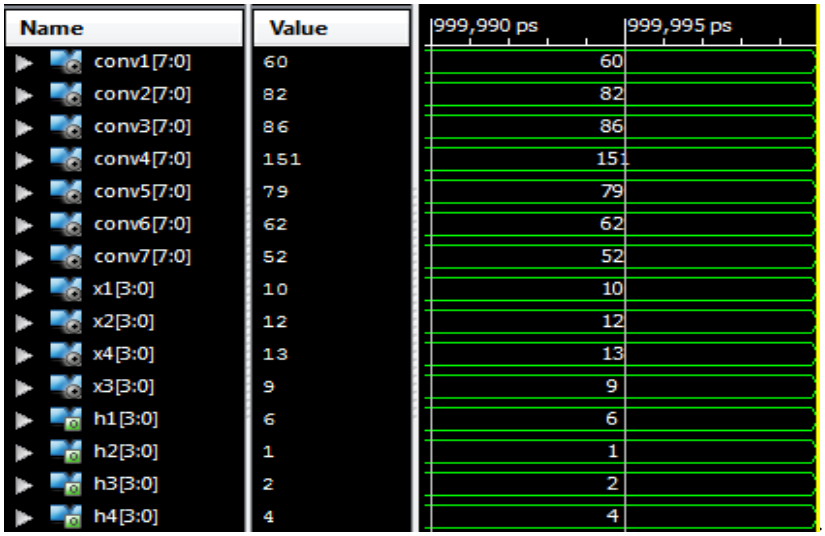

Fig.6. Simulation results of Deconvolution using Vedic mathematics

The Deonvolution module is simulated on Xilinx ISE simulator. The figure 6 shows the simulation result of Deonvolution module using Vedic Mathematics. are the inputs of 4 bit each and conv1, conv2, conv3, conv4, conv5, conv6, conv7 are the convolved inputs of 8 bit each and x1, x2, x3, x4 are the input of 4 bit each. h1, h2, h3, h4 are the outputs each is of 4 bit.

Table IV. comparison of Delay for Convolution using Vedic Mathematics versus conventinal method

Method	Delay
Deconvolution using Non Restoring Algorithm[10]	84.262 ns
Deconvolution using Proposed paravartya Algorithm	64.351 ns

Table IV shows delay improvement of proposed circuit of Deconvolution over Deconvolution using Non Restoring type of algorithm.from the table it is clear that proposed method provides 30% improvement than Non Restoring Algorithm.

VIII. CONCLUSION

The main focus of this paper is to introduce a method for calculating the linear Convolution and Deconvolution with the help of Vedic mathematics Sutrawhich easy to learn, perform and implement.the execution time of proposed method for Convolution is reduce by approximately 28% than the convolution using convolution using conventinal

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 6, June 2015

multiplier. Where as the execution time for Deconvolution is reduce by near about 30% than Non Restoring type of Algorithm.

REFERENCES

[1] J. G. Proakis and D. G. Manolakis, "Digital Signal rocessing: Principles, Algorithm, and Applications," 2nd Edition. New York Macmillan, 1992.
[2] Pierre, John W. "A novel method for calculating the convolution sum of two finite length sequences." Education, IEEE Transactions on 39.1 (1996): 77-80.
[3]Jain, S. ; Saini S. "High Speed Convolution and Deconvolution algorithm (Based on Ancient Indian Vedic Mathematics) electrical engineering/electronics, computer, telecommunications and information technology (ecti-con), 2014 11th international conference on doi: 10.1109/ecticon.2014.6839756 Publication Year: 2014 , Page(s): 1 – 5.IEEE 2014
[4] Lomte, Rashmi K., and P. C. Bhaskar. "High Speed Convolution and Deconvolution Using Urdhva Triyagbhyam." VLSI (ISVLSI), 2011 IEEE Computer Society Annual Symposium on. IEEE, 2011.
[5] Itawadiya, Akhalesh K., et al. "Design a DSP operations using vedic mathematics." Communications and Signal Processing (ICCSP), 2013 International Conference on. IEEE, 2013.
[6] L. Sriraman, T.N. Prabakar, "Design and Implementation of Two Variable Multiplier Using KCM and Vedic Mathematics," 1st Int. Conf. on Recent Advances in Information Technology, Dhanbad, India, 2012, IEEE Proc., pp. 782-787.
[7] Bansal, Y. ; Madhu, C. ; Kaur, P." High speed Vedic Multiplier Design A Review" Proceedings of 2014 RAECS UIET Panjab University Chandigarh, 06 – 08.IEEE March, 2014
[8]Huddar S., Kalpana M., Mohan S."Novel High SpeedVedic Mathematics Multiplier Using Compressors" Automation, Computing, Communication, Control and Compressed Sensing (iMac4s), 2013 International Multi-Conference pp: 465 - 469
[9] Senapati, Ratiranjan, Bandan Kumar Bhoi, and Manoranjan Pradhan "Novel binary divider architecture for high speed VLSI applications." Information & Communication Technologies (ICT), 2013 IEEE Conference on. IEEE, 2013.
[10]Jain S., Pancholi M, Garg Harsh, Saini S. "Binary Division algorithm and high speed Deconvolution algorithm (Based on ancient indian Mathematics)" Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTI-CON), 2014 11th International Conference Page(s): 1 – 5
[11] Lomte, Rashmi K., and P. C. Bhaskar. "Speedy Deconvolution using Vedic Mathematics." International Journal of Scientific and Engineering Research 2.5 (2011): 115-118
[12] Jagadguru Swami Sri Bharati Krisna Tirthaji Maharaja, "Vedic Mathematics: Sixteen Simple Mathematical Formulae from the Veda", Motilal Banarasidas Publishers,Delhi, 2009, pp. 5-45.