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Efficient FPGA Implementation of a Configurable Channel Estimation Algorithm for Wireless Communication Systems

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ABSTRACT: Wireless communication is intruding in every application realm. Cost effective solutions to design, development and testing of wireless systems is getting great interest among researchers. The efficient implementation of their components in terms of hardware cost and design time is of great importance. The major bottleneck in achieving higher throughput, data rate and lower BER in wireless communication is fading. MIMO uses multiple transmit antennas and receive antennas to improve both reliability and throughput of a receiver. Multiple antenna system requires the knowledge of channel state information (CSI) at the receiver for data recovery.Therefore highly accurate and fast estimation of wireless channel is of vital importance for error free data recovery.

KEYWORDS: Field Programmable Gate Array (FPGA),Multiple input multiple output systems (MIMO),Channel state information (CSI),Sphere decoder.

INTRODUCTION

Wireless communication is becoming a part of human life, its application extends to many area from simple communication to life giving medical treatments. Wireless communication is divided into mobile communications and fixed wireless communications. Each type of communication has huge demand according to customers need in the market. Wireless communications are a very popular application domain.

The major bottleneck in achieving higher throughput, data rate and lower BER in wireless communication is fading. Though the designed hardware components and system in wireless communication has great reliability, the probability of channel becoming unreliable is prominent. Multiple-input multiple-output (MIMO) is a key technique in combating fading .It is being used in latest wireless standards such as 3G LTE, WiMAX and 802.11n. By exploiting multipath propagation, MIMO uses multiple transmit antennas and receive antennas to improve both reliability and throughput of a receiver. Multiple antenna system requires the knowledge of channel state information (CSI) at the receiver for data recovery . Therefore highly accurate and fast estimation of wireless channel is of vital importance for error free data recovery. LS estimation is more frequently used due to its acceptable performance, but this estimation involves matrix inversion which results in high computational complexity and hence undesirable for hardware implementation. Sphere detection is a prominent method of simplifying the detection complexity while maintaining BER performance comparable with the optimum maximum-likelihood (ML) detection.

There are several alternative of implementing theoretical concepts of communication system on hardware, such as, DSP, ASIC, FPGA etc. FPGA combines the versatility of DSP and the performance of ASIC solutions. Moreover, FPGA solution is reconfigurable which result in reduced prototyping cost and offers parallel processing. This paper describes the FPGA realization of a configurable and flexible sort-free sphere detector, Flex-Sphere that supports 2;3 and 4 antenna/user configuration for uplink transmission. The following performance measures such as throughput of the wireless channel, BER, and implementation complexity are analyzed. The algorithmic optimizations applied to produce an FPGA friendly implementation are also discussed. Rest of the paper organized in the following manner, challenges in wireless communication and solutions to that discussed in. Section II, overcoming the challenges

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in III, overview of MIMO System in Section IV, Section V gives the importance of Channel estimation and Sphere decoding algorithm, design and implementation using FPGA and results in the subsequent sections.

CHALLENGES IN WIRELESS COMMUNICATION

One of the performance degrading effect arises from multipath that exists between wireless transmitter and receiver. Multipath refers to the presence of multiple copies of a transmitted signal at the receiver end due to the presence of multiple radio channel between them. These multiple copies arise due to reflections from various interacting objects present. Adverse effects of multipath and its level is manifested in several forms in communications receivers and it depends on the path difference relative to the wavelength of propagation, the of path difference relative to the signaling rate, and the relative speed between the transmitter and receiver. Multipath from interacting objects that are spaced very close together will cause a random change in the amplitude of the received signal. signals arriving at the receiver along different paths can result in increase in signal strength or reduce it. This gives rise to fading that depends on the wavelength of transmitted signal , known as frequency-selective fading. When there is relative change position n between the transmitter and receiver, this type of fading also depends on time, since the path length is a function of the radio geometry. This results in time-selective fading.

COMPATING FADING

The effects of fading can be combated by using diversity to transmit the signal over multiple channels that experience independent fading and coherently combining them at the receiver. The probability of experiencing a fade in this composite channel is then proportional to the probability that all the component channels simultaneously experience a fade, a much more unlikely event. Diversity can be achieved in time, frequency, or space. Common techniques used to overcome signal fading include:

- Diversity reception and transmission
- MIMO
- OFDM
- Rake receivers
- Space–time codes

Multiple-input multiple-output (MIMO) communication system, which plays an important role in improving wireless communications, is in the forefront of wireless research. The technique has recently emerged as one of the most significant technical breakthroughs in modern communication because of its ability to provide high efficiency and data rate. Numerous researches on antenna technology are ongoing to provide reliable communication systems. However, multiple antenna system relies upon the knowledge of channel state information (CSI) at the receiver for data detection and decoding.

Therefore, an accurate and robust estimation of wireless channel is of crucial importance for coherent data recovery. A considerable number of channel estimation methods have already been studied by different researchers for MIMO system . Least square is a training based estimation technique for which the channel coefficients are treated as deterministic but unknown constant. In practice, LS estimation is more frequently used due to its acceptable performance, but this estimation involves matrix inversion which results in high computational complexity and hence undesirable for hardware implementation.

I. MIMO SYSTEM

Multiple-input, multiple-output (MIMO) communications systems exploits spatial diversity to provide wireless communications channels of unprecedented capacity and throughput, prompting their adoption in wireless communications standards such as 802.11n . A generic MIMO system employing transmit and receive antennas is shown in Fig.1. The benefits of MIMO technology relies on the existence of accurate, high throughput receiver equipment—a very significant embedded architecture design problem. This difficulty is due to the following factors, the high computational complexity of accurate detector algorithms such as Sphere Decoders (SDs) is apparent in the

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current absence of reported real-time implementations for even moderate MIMO systems, such as the 4 X 4 16-QAM topologies employed in 802.11n

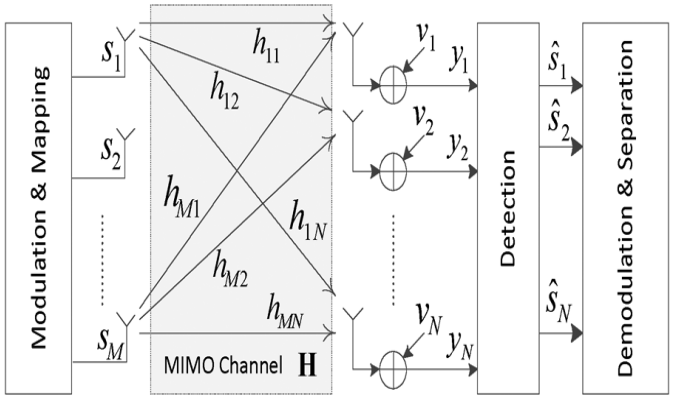

Fig.1.MIMO Communication system

V. SPHERE DECODING ALGORITHM

SD is a receiver baseband signal processing approach employed to estimate. It offers near-ideal detection performance with significantly reduced computational complexity relative to the ideal ML detector Considering an MIMO system with *M* transmit and receive antennas, the received signal *y* is given by

$$y = u H + n \qquad (1)$$

where u is a transmitted signal vector and n is an additive white Gaussian noise vector. H is the M x N channel matrix that can be assumed as known from perfect channel estimation and synchronization. For selected modulation scheme, each element of the transmit vector is a constellation point and the channel matrix generates a lattice. The ML decoding algorithm is to find the minimal distance between the received point and the examining lattice point that

$$u^{\wedge} = \arg \min \left\| y - uH \right\|^2 \qquad (2)$$

$$u \in \Omega^{M_T}$$

where is the $u^{\wedge}$ decoded vector. The entries of u are chosen from a complex constellation Ω The set of all possible transmitted vector symbols is denoted by Ω_M. Thus, the ML-based sphere decoding system can be summarized as follows.

Input: The channel lattice generation matrix H and the received signal vector Y.
Output: A 1 X M vector such that uH is a lattice point that is the closest to y .
A range of simplified SD variants have emerged in an attempt
to alleviate this complexity problem whilst maintaining quasi-ML detection accuracy. Amongst these, Fixed-Complexity SD (FSD) is exceptional since it uniquely combines relatively low complexity, deterministic behavior and quasi-ML accuracy. FSD has a two-phase behavior:
1) *Pre-Processing (PP)*: The symbols of are ordered for detection and the centre of the decoding sphere is initialized using Zero Forcing detection.
2) *Metric Calculation & Sorting (MCS)*: An -level decode tree performs a Euclidean distance based statistical estimation of s

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VI. FPGA IMPLEMENTATION

The hardware is designed in modular structure in order to simplify system design. This section illustrates the hardware design of a 2×2 antenna receiver. The main emphasis is led on the ability to extend the hardware in an easy way if the system requires hardware updates. The receiver combines the received signals and the channel matrix obtained from the channel estimation module. Hardware design and implementation of the receiver is based on (6) and (7). However the complex values and their operations of the equations cannot be simply implemented using hardware description language. These are expanded to real and imaginary parts to simplify implementation. The FPGA implementation process starting from system specification is outlined in Figure 3. The system is first examined with a high level simulation using MATLAB. Different sub-blocks of the system are then translated for hardware implementation.

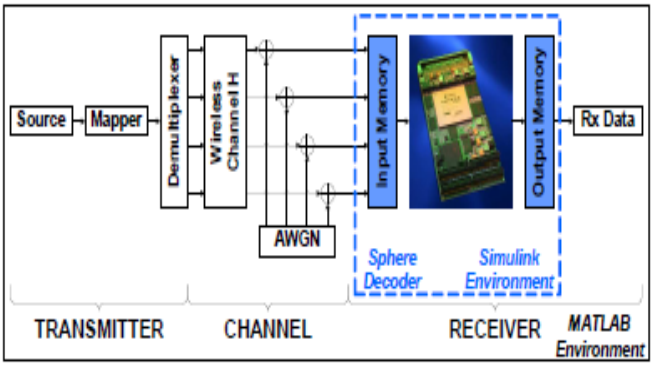

Fig.2 Hardware for MIMO system

The HDL used in this work is VERILOG for its flexibility of coding styles and suitability for handling very large and complex designs. Xilinx ISE 10.1 and XST engine are used for VERILOG synthesis and place-and-route, while Mentor ModelSim XE III 6.3c is used to run functional and post place-and-route simulations. After compilation, simulation and synthesis, configuration files are generated which are used to configure FPGA device. In every step the outputs are verified by comparing with MATLAB simulation result.

The MIMO receiver is implemented on a Xilinx Virtex™-4 LX MB Development Kit. The board includes a Xilinx XC4VLX60 FPGA device, 64MB of DDR SDRAM, 4MB of Flash, 16-bit LVDS Transmit and Receive ports, programmable LVDS clock source, USB-RS232 Bridge, a 10/100 Ethernet PHY, 100 MHz clock source, RS-232 port, and additional user support circuitry to develop a complete system. The board also supports the P240 expansion module standard, allowing application specific expansion modules to be easily added. The FPGA in the board has a total of 59,904 logic elements available for system development. With all these features the device can be configured to implement very complex systems.Figure 2 shows the picture of the experimental setup of the work.

The task of the decoder at MIMO receiver is to combine the signals simultaneously received in all antennas to construct an improved signal, from which the transmitted signal can be recovered. The decoder at the receiver takes the input of four 16 bit real and imaginary parts of the channel estimate and four 16 bit real and imaginary parts of the received signals. The design is a multicycle implementation; it takes multiple clock cycles to compute the results. The multipliers take one clock cycle to calculate a product and the add/subtract units also take one clock cycle.Therefore two symbol estimates (real and imaginary parts) are produced every 8 clock cycles.

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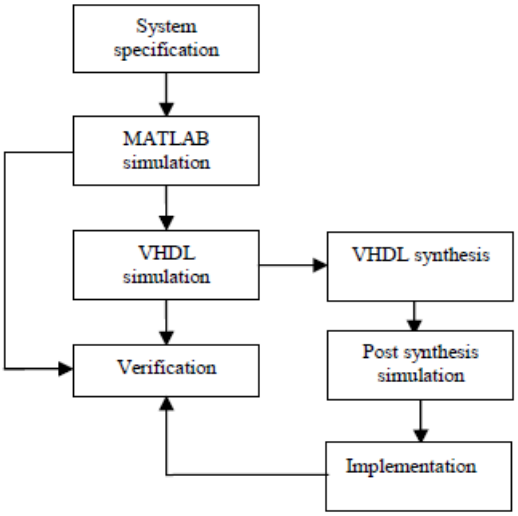

Fig.3 Implementation Design flow

VII. FPGA IMPLEMENTATION RESULTS

The SD and the FSD have been implemented for a $4x\ 4$ system using 16-quadrature amplitude modulation (QAM) modulation. In addition, the FSD has also been implemented for a 4X4 system using 64-QAM modulation. The resource use of the implementations of both 4 parallel SDs and the FSD on the Xilinx Virtex-II-Pro FPGA board are summarized in Table I for the case of 16-QAM. The input symbols to the algorithms have been quantized using 16 bits per real component with both algorithms achieving effectively the same bit error ratio (BER) performance.

TABLE I

FPGA RESOURCE USE OF 4-SDS AND THE FSD

Xilinx XC2VP70 FPGA	4-SDs	FSD
Number of slices	66%	39%
Number of flip-flops	27%	23%
Number of 4-input LUTs	46%	44%

VIII. CONCLUSION

It can be seen that the FSD uses significantly less resources than the 4-SDs with the exception of the flip-flops and the multipliers. The flip-flops are used in the design as delay nets to synchronize the different pipeline stages at the end of the detection process. Factors like the regular structure of the algorithm and the possibility of pipelining also determine the suitability of the algorithm for a hardware implementation.

The number of look-up tables (LUTs) has also been considerably reduced. The use of LUTs can be seen as an indicator of the control logic required for the algorithm. In the case of the FSD, the fixed number of operations and the possibility of pipelining greatly reduces the need for control blocks leaving the LUTs mainly to arithmetic operations. Finally, the number of memory blocks has been more than halved, where most of them are due to the input and output buffers defined on the FPGA to synchronize the FPGA board and the Simulink interface.

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