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A Modified Three Phase Four-Wire UPQC Topology with Reduced DC-Link Voltage Rating

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ABSTRACT: This circuit consists of capacitor in series with the interfacing inductor of the shunt active filter. The series capacitor enables reduction in dc-link voltage requirement of the shunt active filter and simultaneously compensating the reactive power required by the load, so as to maintain unity power factor, without compromising its performance. This allows us to match the dc-link voltage requirements of the series and shunt active filters with a common dc link capacitor. Further, in this topology, the system neutral is connected to the negative terminal of the dc bus.. This will avoid the requirement of the fourth leg in VSI of the shunt active filter and enables Independent control of each leg of the shunt VSI with single dc capacitor. The topology uses a capacitor in series with the interfacing inductor of the shunt active filter, and the system neutral is connected to the negative terminal of the dc-link voltage to avoid the requirement of the fourth leg in the voltage source inverter (VSI) of the shunt active filter. The average switching frequency of the switches in the VSI also reduces, consequently the switching losses in the inverters reduce. Detailed design aspects of the series capacitor and VSI parameters have been discussed in the paper. A simulation study of the proposed topology has been carried out using PSCAD simulator, and the results are presented. Experimental studies are carried out on three-phase UPQC prototype to verify the proposed topology.

I. EXISTING SYSTEM

In existing system the three phase three WIRE UPQC has used. Mainly Voltage rating of dc-link capacitor largely influences the compensation performance of an active filter.[1-3] So the dc-link voltage for the shunt active filter has much higher value than the peak value of the line-to-neutral voltage.

EXISTING SYSTEM METHODOLOGY

The three phase three wires UPQC system used for compensation of power quality issues.

DISADVANTAGES OF EXISTING SYSTEM:

In this method the UPQC which requires more rating of series and shunt active filters. Additionally to maintain the Low harmonics level by adding passive filters.

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BLOCK DIAGRAM OF PROPOSED SYSTEM:

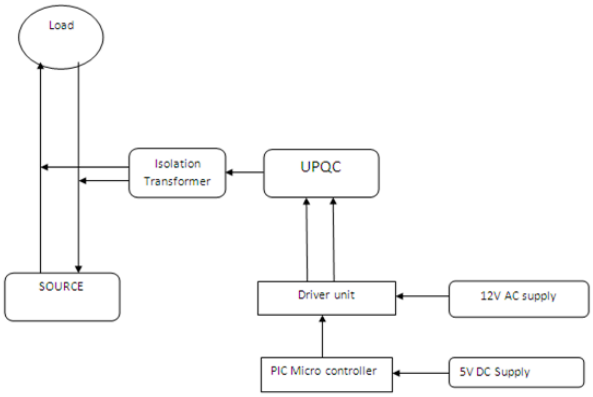

Figure.1. Proposed System Block Diagram

II. COMPONENTS IN THE PROPOSED SYSTEM

BASIC CONFIGURATION OF UPQC

UPQCs consist of combined series and shunt APFs for simultaneous compensation of voltage and current.[4]The series APF inserts a voltage, which is added at the point of common coupling (PCC) such that the load end voltage remains un affected by any voltage disturbance, whereas, the shunt APF is most suitable to compensate for load reactive power demand and unbalance, to eliminate the harmonics from supply current, and to regulate the common DC link voltage and to supply current.. The UPQC has two distinct parts:

Power circuit formed by series and shunt PWM Converters

UPQC controller

III. METHODOLOGY

Three phase four wire UPQC system for control the Power Quality issues.

PRINCIPLE:

The UPQC is a combination of series and shunt active filters connected in cascade via a common DC link capacitor.[5] The main purpose of a UPQC is to compensate for supply voltage power quality issues such as, sags, swells, unbalance, flicker, harmonics, and for load current power quality problems such as, harmonics, unbalance, reactive current and neutral current. A UPQC that combines the operations of a Distribution Static Compensator (DSTATCOM) and Dynamic Voltage Regulator (DVR) together.[6]

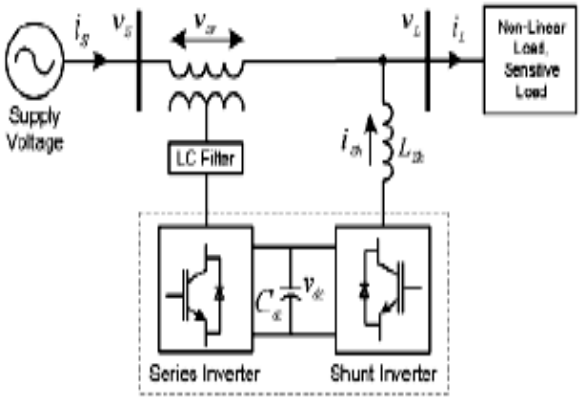

Fig.2. VSI based UPQC

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IV. CONSTRUCTION

Ultra capacitor consists of a porous electrode, electrolyte and a current collector (metal plates). There is a membrane, which separates, positive and negative plated is called separator. The following diagram shows the ultra capacitor module by arranging the individual cell.*[7]*

WORKING*:*

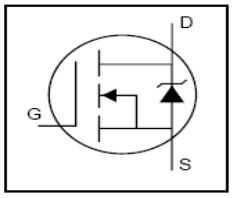
- Alternating current (AC) is used for power line transmission and for high power devices like appliances and lights.
- The characteristics of AC make it ideal for transmission over long lines and for delivering large amounts of power for relatively unregulated uses, such as generating heat and light.
- Lower power appliances and devices require the closely regulated control of direct current power (DC). As a normal house is supplied with AC, it must be converted to DC for many uses.
- Two high power AC networks can be connected via a DC link, as that does not require both networks to be synchronized in frequency and phase, which is often difficult or impossible. [8]
- DC link exists between a rectifier and an inverter, for example, in a phase converter. On one end, the utility connection is rectified into a high voltage DC. On the other end, that DC is switched to generate a new AC power waveform. [9]
- It's a link because it connects the input and output stages. The term "DC link" is also used to describe the decoupling capacitor in the DC link. I assume that this is what you're asking about.
- The switching network on the output side generates very large transients at the switching frequency.
- The DC link capacitor helps to keep these transients from radiating back to the input. This can also help prevent the switching network from oscillating or triggering inadvertently at an inappropriate moment and causing a short. [10]
- Additionally, if the input is not multiple-phase, the capacitor helps provide a source of energy when the input waveform is near zero.[11]

PERFORMANCE OF DRIVER UNIT

- The input to a TTL circuit is always through the emitter(s) of the input transistor, which exhibits a low input resistance.
- The base of the input transistor, on the other hand, is connected to the Vcc line, which causes the input transistor to pass a current of about 1.6 mA when the input voltage to the emitter(s) is logic '0', i.e.,near ground. [12]
- Letting a TTL input 'float' (left unconnected) will usually make it go to logic '1', but such a state is vulnerable to stray signals, which is why it is good practice to connect TTL inputs to Vcc using 1 kohm pull-up resistors.
- The most basic TTL circuit has a single output transistor configured as an inverter with its emitter grounded and its collector tied to Vcc with a pull-up resistor, and with the output taken from its collector.

POWER MOSFET:

The MOSFET, or Metal-Oxide-Semiconductor Field-Effect Transistor is far the most common field effect transistor in both digital and analog circuits. The MOSFET is composed of a channel of n-type or p-type semiconductor material, and is accordingly called an NMOSFET or a PMOSFET. Unfortunately, many semiconductors with better electrical properties than silicon, such as gallium arsenide, do not form good gate oxides and thus are not suitable for MOSFETs.



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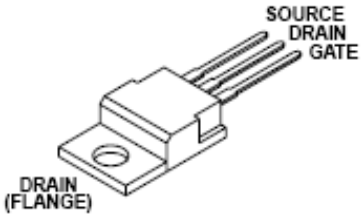

Fig 3. Power MOSFET

FEATURES OF POWER MOSFET:

- Power MOSFET has lower switching losses but its on-resistance and conduction losses are more.

BIDIRECTIONAL DC-DC CONVERTER:

The bidirectional dc to dc converter along with energy storage has become a promising option for many power related system including power related systems and hybrid electric vehicles. [13-14] It is not only reducing the cost and improving the efficiency. MOSFET is the switches used in the converter. In this T_1,T_2,T_3,T_4 are the switches used in the inverter bridge side and T_5,T_6,T_7,T_8 are the switches used in the rectifier side . Where L is the leakage inductance used for the soft switching and the values for the leakage inductance is 27 ⍰H, ,the capacitorsC_{dc1} ,C_{dc2}used for the filtering purpose

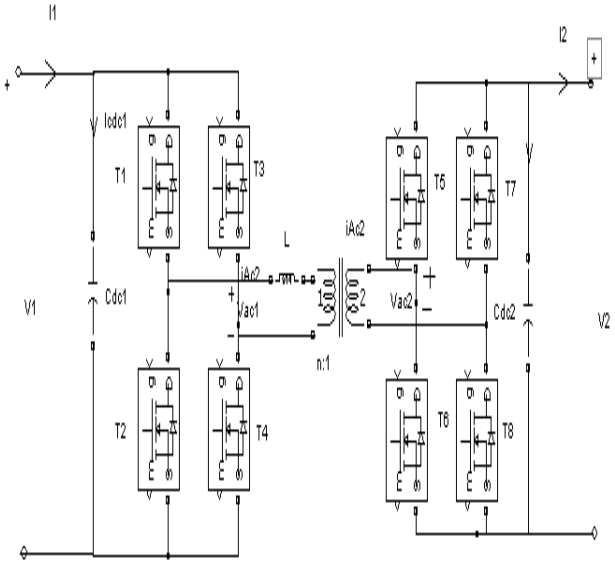

Fig 4. Bidirectional dc-dc converter circuit diagram

- In ,Dual active-bridge bi-directional dc-dc converter, the one full bridge serves as High Frequency (HF) inverter and the other full bridge serves as rectifier.

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V. OPERATING PRINCIPLE

The operating principle of the proposed system can be explained by the following modes of operation

MODES OF OPERATION
MODE1:

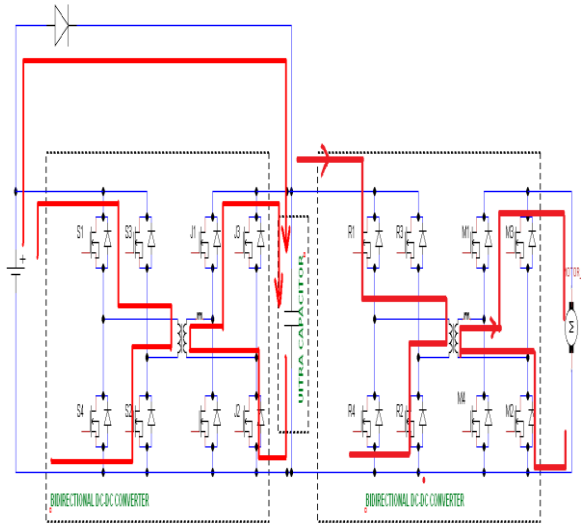

Fig 5. Energy flow of the Acceleration mode phase I

In Mode1 energy from the battery is directly supplied to Dual active bridge converter2(DAB2) and from DAB2 the energy is supplied to the motor and it starts running, meanwhile charging takes place in Ultra capacitor from battery through DAB1.'

MODE 2

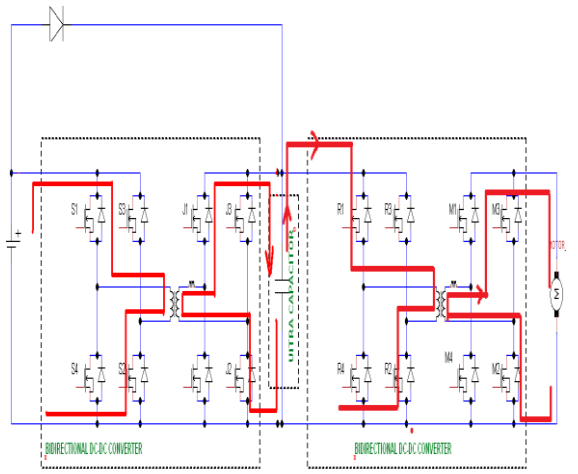

Fig 6. Energy flow of the Acceleration mode phase II

In Mode2 the motor draws energy from Ultra capacitor through Dual active birdge2. In this mode vehicle speed is increased.

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MODE 3

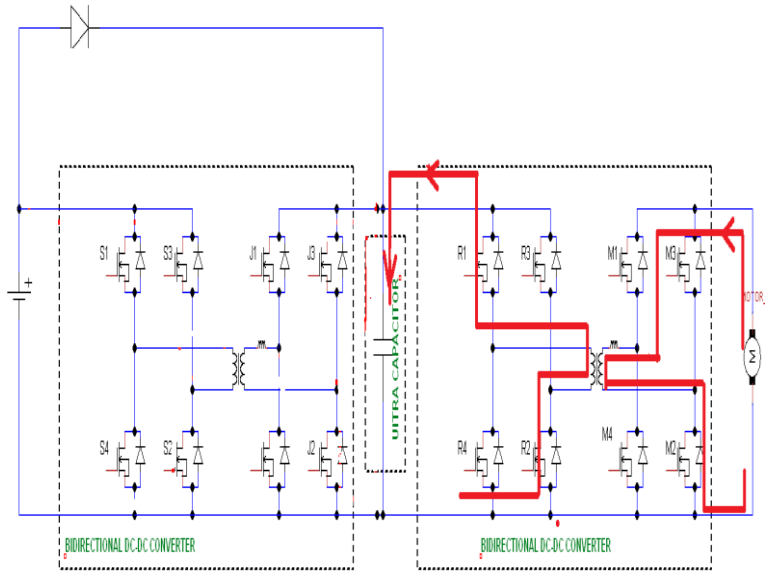

Fig 7. Energy flow of Regenerative braking phase I

InMode 3 theexcess energy from the motor is stored in ultra capacitor through Dual active bridge 2.

MODE 4

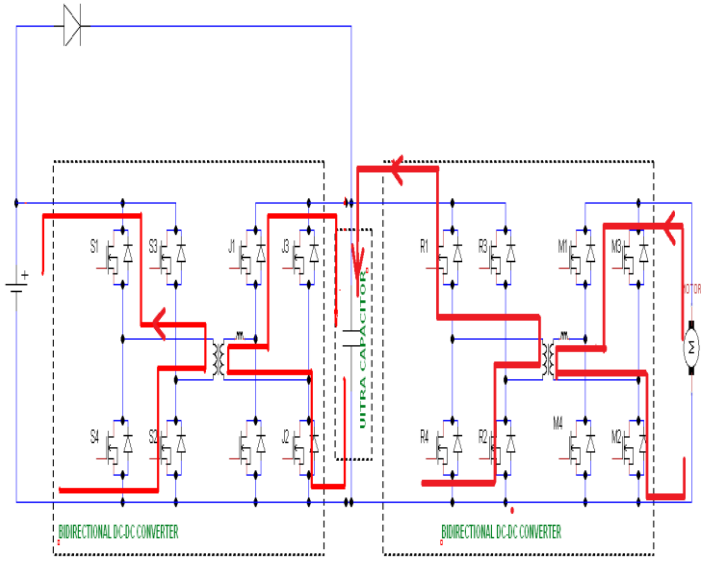

Fig 8. Energy flow of Regenerative braking phase II

In this mode when ultra capacitor is fully charged the energy from the motor is stored in battery through Dual active bridge1.

V_{in} is the input voltage

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$$V_0 = 6V$$

VI. SIMULINK RESULTS

SIMULINK MODEL

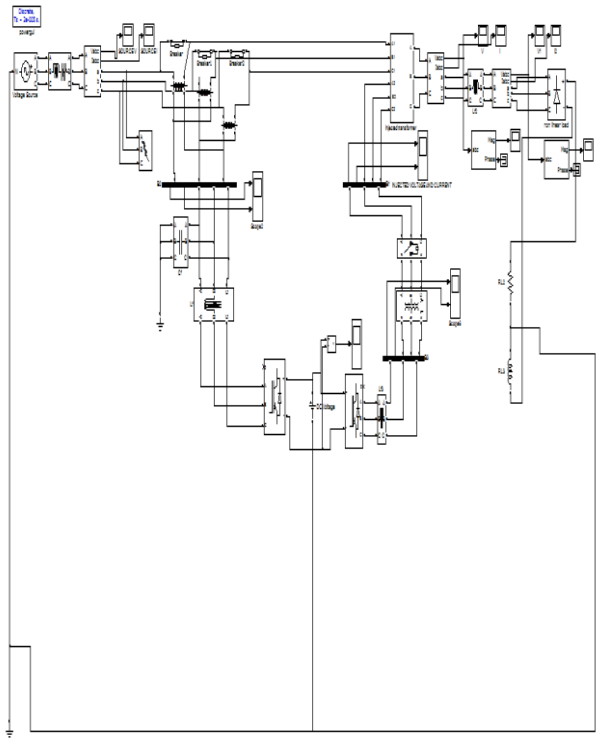

Fig 9. Simulink Diagram

OPTOCOUPLERS

The most important parameter for most Optocouplers is their transfer efficiency, usually measured in terms of their current transfer ratio or CTR. This is simply the ratio between a current change in the output transistor and the current change in the input LED which produced it. Typical values for CTR range from 10% to 50% for devices with an output phototransistor and up to 2000% or so for those with a Darlington transistor pair in the output. Note, however that in most devices CTR tends to vary with absolute current level. Typically it peaks at a LED current level of about 10mA, and falls away at both higher and lower current levels. Other optocoupler parameters include the output transistor's maximum collector-emitter voltage rating VCE (max), which limits the supply voltage in the output circuit; the input LED maximum current rating IF (max), which is used to calculate the minimum value for its series resistor; and the Optocouplers bandwidth, which determines the highest signal frequency that can be transferred through it ó determined mainly by internal device construction and the performance of the output Phototransistor.

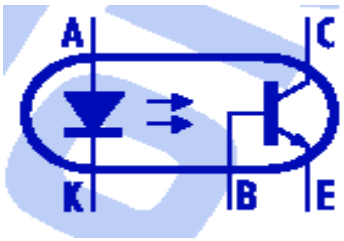

Fig 10. Optocoupler

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SIMULATION RESULT:

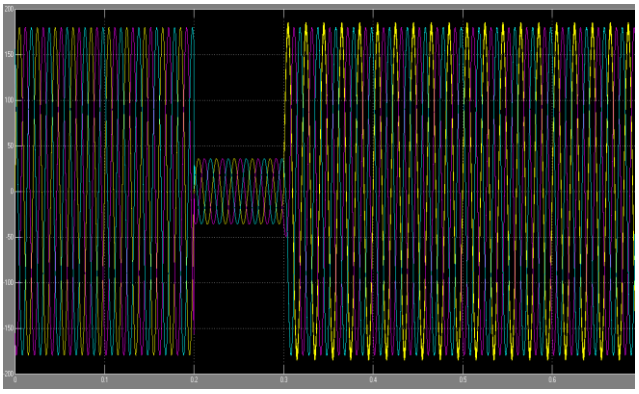

Fig 11.Output voltage with voltage sag

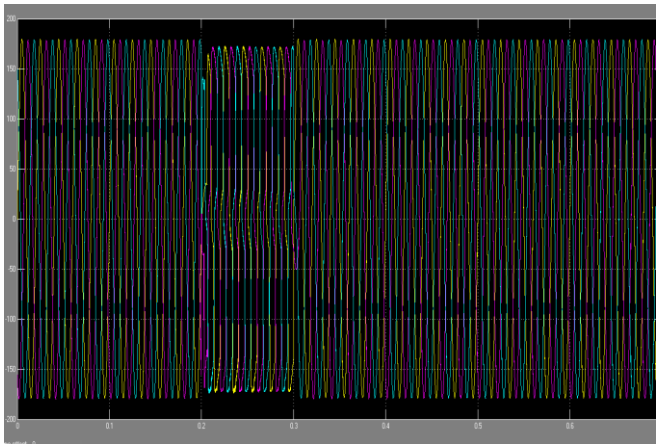

Fig 12.Output voltage after eliminating voltage sag

VII. CONCLUSION

A modified UPQC topology for three-phase four-wire system has been proposed in this paper, which has the capability to compensate the load at a lower dc-link voltage under non stiff source. Design of the filter parameters for the series and shunt active filters is explained in detail. The proposed method is validated through simulation and experimental studies in a three-phase distribution system with neutral-clamped UPQC topology (conventional). The proposed modified topology gives the advantages of both the conventional neutral-clamped topol ogy and the four-leg topology. Detailed comparative studies are made for the conventional and modified topologies. From the study, it is found that the modified topology has less average switching frequency, less THDs in the source currents, and load voltages with reduced dc-link voltage as compared to the conventional UPQC topology.

VIII. HARDWARE MODELLING

DRIVER CIRCUIT

The IR2110 are high voltage, high speed power MOSFET and IGBT drivers with HARD independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction.

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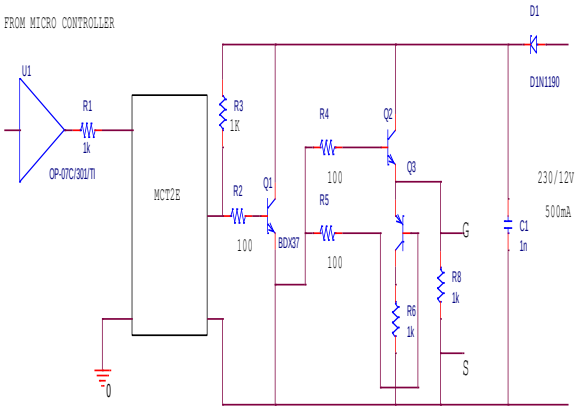
Circuit Diagram Of The Control Circuit



Fabrication Of Driver Circuit

ARCHITECTURE OF PIC16F877A

Make : FAIRCHILD
Vdc : 500V
Id :continuous : AT 25 ºC , 20A
Idm: Drain current- pulsed :80A
Vgss : +-30V
Iar avalanche current : 20 A
Tl : maximum lead temp: 300 ºc

Clock Management

- 2% internal oscillator
- Programmable PLL and oscillator clock sources
- Fail-Safe Clock Monitor (FSCM)
- Independent Watchdog Timer
- Low-power management modes
- Fast wake-up and start-up

Core Performance

- Up to 40 MIPS 16-bit dsPIC33F CPU
- Two 40 bit wide accumulators
- Single-cycle (MAC/MPY) with dual data fetch
- Single-cycle MUL plus hardware divide

Motor Control PWM

- Up to four PWM generators with eight outputs
- Dead Time for rising and falling edges
- 25 ns PWM resolution
- PWM support for Motor Control: BLDC, PMSM, ACIM, and SRM
- Programmable Fault inputs
- Flexible trigger for ADC conversions and configurations.

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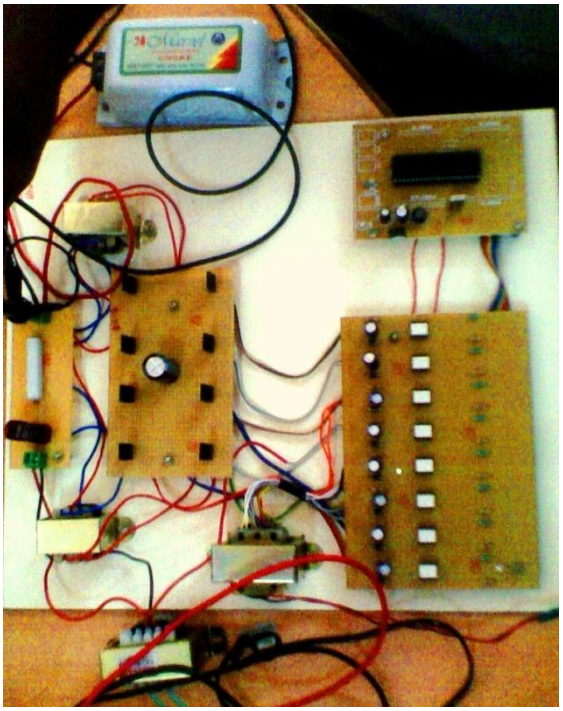
HARDWARE CIRCUIT



IX. CONCLUSION

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