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A Quadrupler Voltage Interleaved DC-DC Boost Converter with Fuzzy Logic Implementation

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ABSTRACT: The output voltage generated by the sources such as photovoltaic arrays, the fuel stacks, the super capacitors or the battery sources are very low, in the range of 12-48 V. Hence it must be boosted to a high voltage. Therefore a novel topology for a boost converter, which can achieve a higher voltage gain, is necessary. The proposed converter is derived from a two-phase interleaved boost converter. The advantages of interleaved boost converter compared to conventional topologies include high voltage gain, high efficiency, low input current ripple and better transient responses. Even though high voltage gain can be obtained, the closed loop control of transformer-less boost converter with PI controller results in reduction of the system responses and causes damage to the components used in the system. So, in order to overcome these drawbacks a quadrupler voltage boost converter with Fuzzy Logic Controller (FLC) is presented. Here simulation models of transformer-less interleaved boost converter with PI controller and Fuzzy Logic Controller in MATLAB was developed.The analytical model for the switching intervals has been validated with the simulation results using MATLAB simulation tool.

KEYWORDS:DC-DC converter, PI Controller, Fuzzy Logic Controller, Fuzzifier, Defuzzifier, Interleaved Boost Converter.

I.INTRODUCTION

The voltage provided by a number of small power generating sources such as renewables is usually low in amplitude. As a result of this, boost-type architecture with a large voltage gain is required to link this voltage to an inverter.A traditional boost converter can achieve an infinite voltage gain as the duty cycle approaches 100% in theory, but in practice, the leakage resistance in the inductor-charging loop limits the boost ratio.Because of this, a boost converter is not used when the required boost ratio is higher than four. Another important requirement is to drain a continuous current with minimum ripple.Therefore, converters combining these two features are expected to find many applications within the renewable-energy context. In the photovoltaic case, the current ripple impacts the power generation since it produces an oscillation around the MPP reducing the energy extracted from the photovoltaic generator. These characteristics make the boost converter a good candidate to interface the photovoltaic systems. Another possibility to reduce the converter's input current ripple is given by the interleaving structures. The interleaved structure can effectively increase the switching frequency and reduce the input and output ripples as well as the size of the energy storage inductors.

II.LITERATURE SURVEY

In the literature, converter topologies for obtaining high voltage gain have been mentioned. Papanikolaouet al. [1] proposes an isolated dc–dc flyback converter with a high step-up voltage gain and some energy regeneration techniques to clamp the voltage stress on the active switch and to recycle the leakage inductance energy. Li et al. [2] defines a family of interleaved high step-up boost converters with winding-cross-coupled inductors. In this converter the active clamp or passive lossless clamp circuits are adopted to achieve soft-switching operation. Here the coupled inductor section is covered.

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Ismail et al. [3] proposes a switched capacitor-based converter which provides solutions to improve the conversion efficiency and achieve large voltage conversion ratio. But In this proposed converter, the conventional switched capacitor technique makes the switch suffer high transient current and large conduction losses. Yang et al. [4] defines a high step-up ratio converter to achieve higher voltage conversion ratio and further reduce voltage stress on the switch and diode. This converter can provide large step-up voltage conversion ratios. But again, the voltage stress of diodes in those converters remains rather high.

In this paper, ref. [5,6 and 7] were taken into consideration while analysing the existing converter, whichdescribes about how the fuzzy logic can be applied to the converter and improve the system responses.

III. TRANSFORMER-LESS BOOST CONVERTER

The main objective of the topology is to obtain high voltage gain and such characteristic can only be achieved when the duty cycle is greater than 0.5 and in CCM. With duty cycle lower than 0.5 or in DCM, there is no enough energy transfer from the inductors to the blocking capacitors, output capacitors, and load side, and consequently it is not possible to get the high voltage gain as that for duty ratio greater than 0.5. In addition, only with duty cycle larger than 0.5, due to the charge balance of the blocking capacitor, the converter can feature the automatic current sharing characteristic that can obviate any extra current-sharing control circuit. On the other hand, when duty cycle is smaller than 0.5, the converter does not possess the automatic current sharing capability any more, and the current-sharing control between each phases should be taken into account in this condition.
Following assumptions are made in order to simplify the circuit analysis of the proposed converter,
1) All components are ideal components.
2) The capacitors are sufficiently large, such that the voltages across them can be considered as constant approximately.
3) The system is under steady state and is operating in CCM and with duty ratio being greater than 0.5 for high step-up voltage purpose.

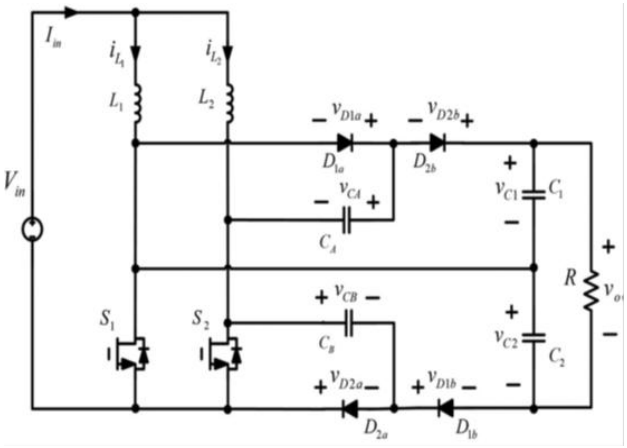

Fig. 1 Transformer-less Boost Converter

The converter topology is basically derived from a basic two-phase interleaved boost converter. Fig. 1 shows the circuit diagram of the topology. In this topology the boost inductors L1 and L2 connected parallel forms the interleaved structure. Active switches S1 and S2 are placed in the two phases. D1a, D1b, D2a, D2b forms the power diodes. CA and CB constitute the blocking capacitors and C1 and C2 the output capacitors.

IV. PROPOSED CONVERTER AND OPERATION PRINCIPLE

One switching period of the converter is divided into five intervals. The detailed theoretical analyses for each mode will be given as follows.

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Mode 1: Mode 1 corresponds to the time interval ($t_0 \leq t < t_1$). Before t_0, the converter works at a current free-wheeling stage, and both iL_1 and iL_2 are equal to zero. For mode 1, switches S_1 and S_2 are triggered to conduct and diodes D_{1a}, D_{1b}, D_{2a}, and D_{2b} are all OFF. The corresponding equivalent circuit is shown in Fig.5.3. In this case both iL_1 and iL_2 are increasing to store energy in L_1 and L_2, respectively. The voltages across diodes D_{1a} and D_{2a} are clamped to capacitor voltage V_{CA} and V_{CB}, respectively, and the voltage across the diodes D_{1b} and D_{2b} are clamped to V_{C2} minus V_{CB} and V_{C1} minus V_{CA}, respectively. Also, the load power is supplied from capacitors C_1 and C_2. The corresponding state equations are given as follows. Fig. 2 shows the equivalent circuit.

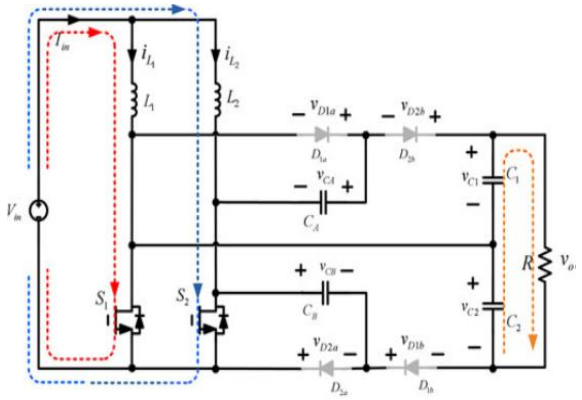

Fig. 2 Equivalent Circuit for Mode 1($t_0 \leq t < t_1$)

Mode 2: Mode 2 corresponds to the time interval ($t_1 \leq t < t_2$). For this operation mode, switch S_1 remains conducting and S_2 is turned OFF. Diodes D_{2a} and D_{2b} become conducting. The corresponding equivalent circuit is shown in Fig.3. It is seen from Fig.3 that part of stored energy in inductor L_2 as well as the stored energy of C_A is now released to output capacitor C_1 and load. Meanwhile, part of stored energy in inductor L_2 is stored in C_B. In this mode, capacitor voltage V_{C1} is equal to V_{CB} plus V_{CA}. Thus, iL_1 still increases continuously and iL_2 decreases linearly.

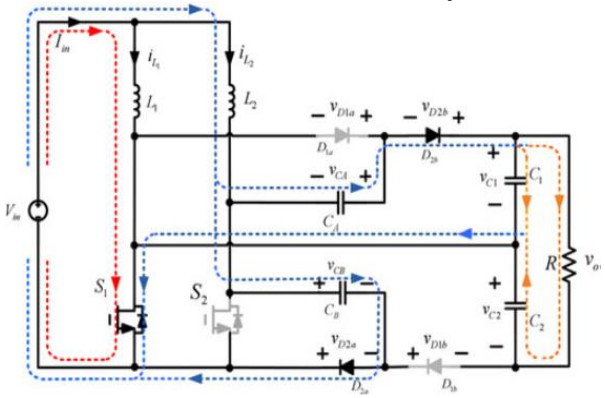

Fig.3 Equivalent Circuit for Mode 2 ($t_1 \leq t < t_2$)

Mode 3: Mode 3 corresponds to the time interval ($t_2 \leq t < t_3$). For this mode, operation is same as in the case of mode1. Both S_1 and S_2 are turned ON. The corresponding equivalent circuit turns out to be the same as Fig. 2.

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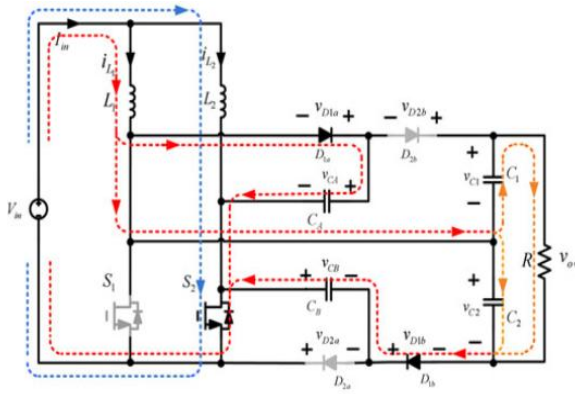

Fig.4 Equivalent Circuit for Mode 4 ($t_3 \leq t < t_4$)

Mode 4: Mode 4 corresponds to the time interval ($t_3 \leq t < t_4$). For this operation mode, switch S_2 remains conducting and S_1 is turned OFF. Diodes D_{1a} and D_{1b} become conducting. The corresponding equivalent circuit is shown in Fig. 4. It is seen from Fig.5.5 that the part of stored energy in inductor L_1 as well as the stored energy of C_B is now released to output capacitor C_2 and load. Meanwhile, part of stored energy in inductor L_1 is stored in C_A. In this mode, the output capacitor voltage V_{C2} is equal to V_{CB} plus V_{CA}. Thus, iL_2 still increases continuously and iL_1 decreases linearly.

V.STEADY STATE ANALYSIS

In order to simplify the circuit performance analysis of the proposed converter in CCM, the same assumptions made in the previous sections will be adopted.

A.Voltage Gain: Referring to Fig. 2 and 3, from the volt-second relationship of inductor L_1 (or L_2), the following relations can be obtained.

$$V_{in}D + (V_{in} - V_{CA})(1 - D) = 0 \quad (1)$$

$$V_{in}D + (V_{in} - V_{CB})(1 - D) = 0 \quad (2)$$

Also from the equivalent circuits in Fig. 5.4 and 5.5, the voltage V_{C1} and V_{C2} can be derived as follows,

$$V_{C1} = V_{CA} + V_{CB} = [2/(1 - D)]V_{in} \quad (3)$$

$$V_{C2} = V_{CA} + V_{CB} = [2/ (1 - D)]V_{in} \quad (4)$$

It follows from (3) and (4) that the output voltage can be obtained as follows:

$$V_o = V_{C1} + V_{C2} = [4/(1 - D)]V_{in} \quad (5)$$

Thus, the voltage conversion ratio M of the proposed converter can be obtained as follows:

$$M = V_o/Vin = 4/ (1 - D) \quad (6)$$

B. Voltage Stresses on Semiconductor Components

To simplify the voltage stress analyses of the components of the proposed converter, the voltage ripples on the capacitors are ignored. From Fig. 3 and 4, one can see that the voltage stresses on active power switches S_1 and S_2 can be obtained directly as shown in the following equation:

$$V_{S1,max} = V_{S2,max} = [1/ (1 - D)]V_{in} \quad (7)$$

Substituting (5) into (7), the voltage stresses on the active power switches can be expressed as

$$V_{S1,max} = V_{S2,max} = V_O/4 \quad (8)$$

From (8), it is clear that the voltage stress of active switches of the proposed converter is equal to one fourth of the output voltage. Hence, the proposed converter enables to adopt lower voltage rating devices to further reduce both switching and conduction losses.

As can be observed from the equivalent circuits in 2 and 4, the open circuit voltage stress of diodes D_{1a},D_{2a},D_{1b}, and D_{2b} can be obtained directly as shown in (9).

$$V_{D1a,max} = V_{D1b,max} = V_{D2b,max} = V_O/2 \ , \ V_{D2a,max} = V_O/4 \quad (9)$$

In fact, it is clear from (8) that the maximum resulting voltage stress of diodes is equal to $V_O/2$. Hence, the proposed converter enables one to adopt lower voltage rating diodes to further reduce conduction losses.

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VI.PI CONTROLLER

As the name suggests it is a combination of proportional and an integral controller. In a PI controller the output is directly proportional to the summation of the proportional of the error and integration of the error signal. The PI controller has the ability to reject disturbances and can stabilize the process. The output dc voltage is sensed and compared with a reference output voltage, which gives the error signal. This error signal is then processed by the controller to keep the output voltage constant.

VII. FUZZY LOGIC CONTROLLER

Fuzzy logic is a multivalued logic. It is an approach to computing based on "degrees of truth" rather than the usual "true or false" (1 or 0) Boolean logic on which the modern computer is based. The idea of fuzzy logic was first advanced by Dr, LotfiZadeh of the University of California at Berkeley in the 1960s. Fuzzy logic includes 0 and 1 as extreme cases of truth (or "the state of matters" or "facts") but also includes the various states of truth in between.The basic block diagram of fuzzy logic controller is shown in Fig. 5

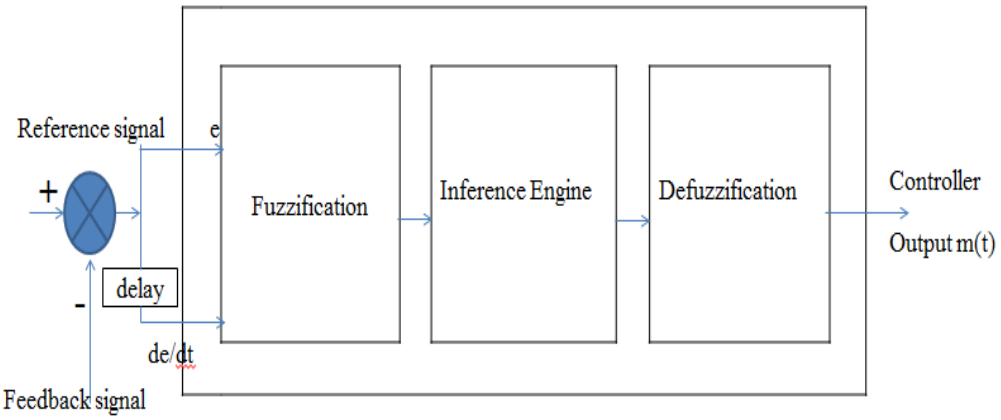

Fig. 5 Basic Block Diagram of FLC

The fuzzy logic controller is divided into five modules. They are fuzzifier, data base, rule base decision maker and defuzzifier. The function of fuzzifier is to convert crisp data into linguistic variables. For example, a car runs at a speed of 10 Kmph. Here 10 Kmph is the crisp or measured data. In terms of fuzzy, it is expressed as "speed of the car is too slow". Here slow is the linguistic variable. Rule base and data base are together known as the knowledge base in which the linguistic variable definitions are made. FLC consist of a control rule set which determines the behavior of the entire system. The function of defuzzifier is to convert back the linguistic variables into crisp values.

A.Fuzzy Inference System (FIS) Editor:Fuzzy Logic Toolbox software does not limit the number of inputs. However, the number of inputs may be limited by the available memory of your machine. If the number of inputs is too large, or the number of membership functions is too big, then it may also be difficult to analyze the FIS using the other GUI tools.
B. Membership Function Editor:To define the shapes of all the membership functions associated with each variable
C.Rule Editor:To edit the list of rules that defines the behavior of the system
D. Rule Viewer: To view the fuzzy inference diagram. Use this viewer as a diagnostic to see, for example, which rules are active, or how individual membership function shapes influence the results.
E. Surface Viewer:To view the dependency of one of the outputs on any one or two of the inputs—that is, it generates and plots an output surface map for the system.

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VIII. SIMULATION MODEL

The transformer-less boost converter is simulated in the MATLAB-SIMULINK version R2013a. The converter was tested with V_{in}= 25V DC and V_o= 400V DC. The simulation circuits are shown below.

TABLE I: Component List of Transformer-less Boost Converter with PI Controller

PARAMETERS	VALUE
Frequency	40kHz
Inductor L_1, L_2	253 µH
Blocking Capacitor C_A, C_B	10 µH
Output Capacitor C_1, C_2	250 µF
Resistor R	400 Ω

The parameter values of the simulation are given in table I for reference.

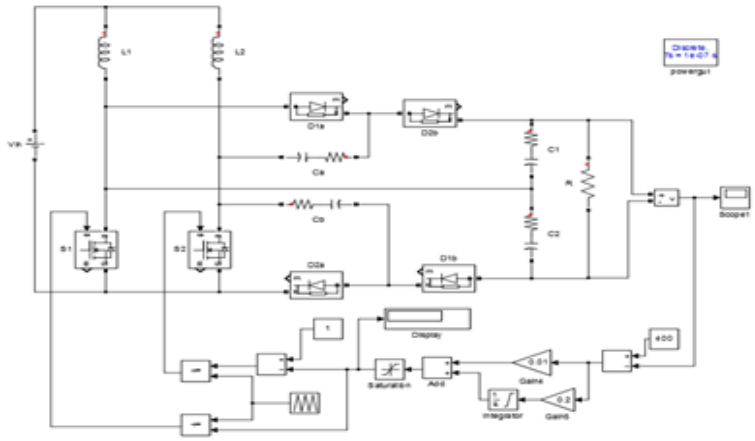
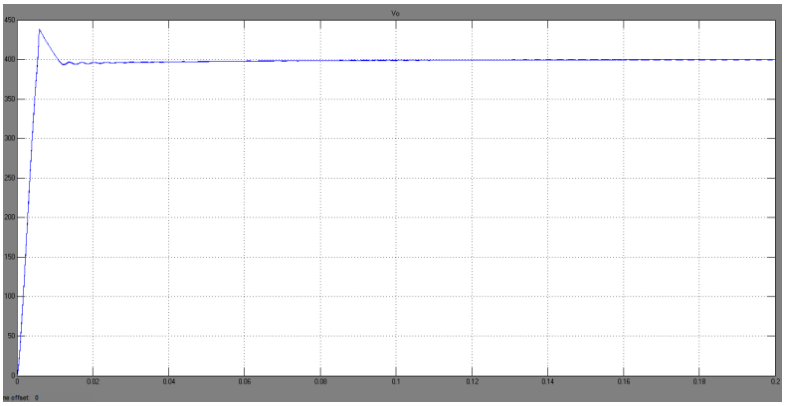


Fig. 6Simulation Model of the Converter PI Controller.

The closed loop circuit of transformer-less boost converter is obtained with PI controller. Fig.6 shows simulation model for closed circuit with PI controller. The output of proportional unit gives the input "error" and the integral unit produces the second input "error change".



Time (sec)

Fig. 7 Output Voltage Waveform of the Converter PI Controller

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The switching frequency is chosen to be 40 kHz, both duty ratios of S_1 and S_2 equal to 0.75. The output voltage waveform of the converter with PI controller is shown in Fig. 7. The output voltage obtained gives a peak-over shoot of 9.5%. The maximum percent overshoot M_P is the maximum peak value of the response curve, measured from c(∞).

Fig.8 shows the simulation model of the quadrupler voltage converter with FLC. The output voltage is compared with reference voltage which is taken as error. Then again a second time this error is given to a delay to obtain the error changes. Thus the 2 inputs: error and error-change is given to the FLC with rule base as a single input using MUX. Again the output of saturation block is given to delay and added to output of FLC, thus boosting the progress.

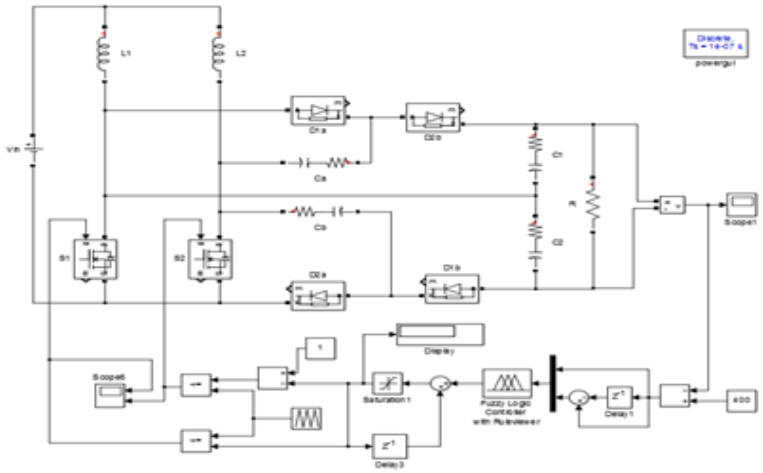

Fig. 8 Simulation Model of the Quadrupler Voltage Boost Converter using FLC

Then the output is compared with less than or equal to [<=] block and the corresponding pulses are given to gate of two MOSFETs. To ensure 180^0 phase shift, one output of saturation block is deducted from 1 and the other output of saturation block is given to and compared with PWM.

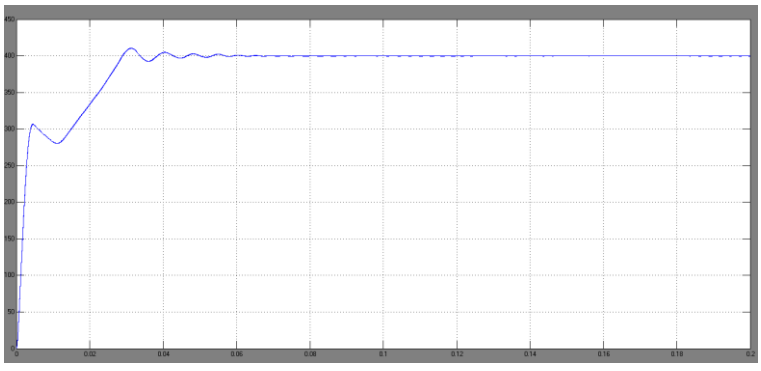

Fig. 9 Output Voltage Waveform of Quadrupler Voltage Boost Converter using FLC

The output voltage waveform with fuzzy logic converter is given in Fig. 9. The settling time of output voltage waveform is obtained as 0.06sec. The settling time Ts is the time required for the response curve to reach and stay within the 2% of the of the final value

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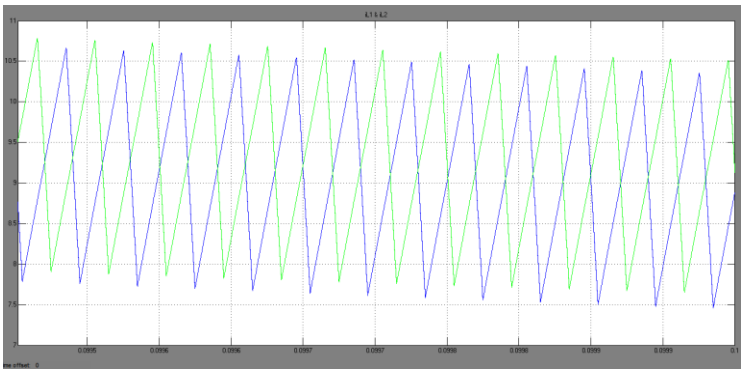

Fig. 10 Input Inductor Current of Quadrupler Voltage Boost Converter using FLC

Fig.10 shows the input inductor current for inductors L_1 and L_2. Both simulated inductor current ripples are about 2.75A. From the waveform it clear that the proposed converter possesses inherent automatic uniform current sharing capability.

TABLE.II Comparison between PI controller and FLC

Controller used	Delay Time(Td) in sec	Rise Time(Tr) in sec	Settling Time(Ts)in sec	Peak Overshoot(Mp) in %	Transient Behaviour
PI Controller	2.84sec	3.95sec	0.1sec	9.5	Oscillatory
Fuzzy Controller	2.19sec	6.45sec	0.06sec	2.75	Smooth when compared to PI

From Table II, it was inferred that the peak overshoot of the quadrupler voltage boost converter with PI controller was 9.5% and with FLC it was 2.75%. The delay time and the settling time of the quadrupler voltage boost converter with FLC is less compared with that of the PI controller.

IX.CONCLUSION

Even though it is possible to achieve high voltage gain, the closed loop control of the transformer-less boost converter with PI controller produces a peak overshoot of 9.5% which will damage the system components and reduces the system responses. So, inorder to overcome these drawbacks a quadrupler voltage boost converter with FLC is proposed. The various waveforms of the quadrupler voltage boost converter with uncoupled interleaved inductor topology and FLC have been simulated using MATLAB. Using these results, comparison between transformer-less boost converter with PI controller and the quadrupler boost converter with FLC has been done. By making use of FLC it is possible to reduce the peak overshoot, delay time and the settling time of the converter thereby improving the system response and prevent the damage caused to the components of the system

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