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PD-PWM Based Cascaded H-Bridge Multilevel Inverter for Photovoltaic Systems

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ABSTRACT: This paper aims at using (PD-PWM) Phase disposition pulse width modulation technique to reduce leakage current in a transformerless cascaded multilevel inverter for PV systems.As the transformerless inverters are of lesser weight, simple and has higher efficiency than that which has transformer. Along with these merits we have certain demerits , this topology provides a path for the leakage current to flow through the parasitic capacitance formed between the PV module and the ground. Modulation technique reduces leakage current with an added advantage without adding any extra components.

KEYWORDS : Cascaded H-bridge transformerless inverter, Leakage current, Space vector pulse width modulation, Multi carrier pulse width modulation, Phase disposition pulse width modulation , Phase opposition disposition pulse width modulation .

I. INTRODUCTION

The renewable energy resources have more scope in the modern technology as they have more advantages than that of non-renewable energy, they have less pollution, less noise and are completely nature-friendly. Two and three level inverters are unable to provide higher efficiency and grid code requirements for higher power and voltage ratings. Therefore medium and megawatt scale PV inverters are moving towards the multilevel structures. Cascaded H-Bridge type has shown to be more advantageous than other methods and also the proposed system in this paper mainly concentrates on the PD-PWM modulation technique implemented on the cascaded H- bridge inverter.

II. LITREATURE SURVEY

The PV modules have higher installation costs in order to reduce the overall cost of a cascaded H-bridge inverter for PV systems[1]-[2], we can make it transformerless, which not only makes it cost effective but also will reduce the weight and gives higher efficiency.

By making it transformerless , one of the challenges that has to be faced is that , the PV module with respect to the ground has high amount of leakage current flowing through it, which when a living being comes in contact with , will lead to a fatal injury [4]-[5]. In order to reduce it, many researches have suggested that the multi-carrier pulse width modulation can be used to the switches of the inverter that can reduce the leakage current to a significant amount, as the SVM technique is very tedious and requires more computational task carrier based modulation technique is more preferred rather than SVM methods[6]–[11].

III.MULTILEVEL INVERTERS AND THEIR TOPOLOGIES

The concept of multilevel inverters was introduced during 1970's for industrial applications as alternative in high power and medium voltage situations. The multilevel inverters are used to obtain high output power from medium voltage sources like solar panels, batteries, super capacitors etc.

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TYPES OF MULTILEVEL INVERTERS

Multilevel inverters are usually of three types:

- Diode clamped multilevel inverter.
- Capacitor clamped multilevel inverter.
- Cascaded H-bridge multilevel inverter.

A. Diode clamped multilevel inverter:

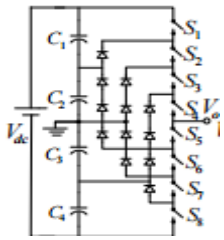

Fig 1: Diode clamped multilevel inverter

Figure 1 illustrates the diode clamped multilevel inverter topology of five level(0, $\pm\frac{V_{DC}}{2}$,$\pm V_{DC}$)which uses diodes and gives m-levels as per the user requirement to reduce the harmonic content in the output voltage. The more the levels, less is the harmonic content and also sinusoidal output voltage will be of more quality. As the number of levels increases, complexity increases in controlling the control circuit of the topology as switching devices are increased.

B.Capacitor clampedmultilevel inverters

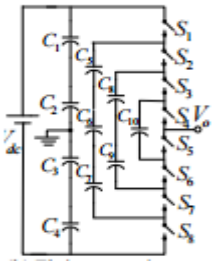

Fig 2: Capacitor clampedmultilevel inverters

Figure 2 shows capacitor clamped multilevel inverter which is five level (0, $\pm\frac{V_{DC}}{2}$,$\pm V_{DC}$) , that is very similar to diode-clamped multilevel inverter except that it has capacitors instead of diodes.In this topology the component count gets decreased as one capacitor replaces two diodes.But the only disadvantage of this topology is that it has very high value of capacitors used and also balancing the voltage becomes more complicated task.

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C. Cascaded H-bridge multilevel inverter

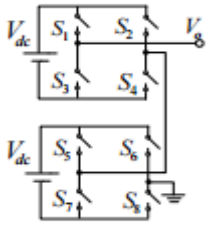

Fig 3: Cascaded H-bridge multilevel inverter

The figure 3 shows the five level cascaded H-bridge which has five levels of voltage (0, $\pm\frac{V_{DC}}{2}$,$\pm V_{DC}$). The disadvantages of the above two types is overcome by cascaded H-bridge multilevel inverter, it uses capacitors, switches and requires very less number of components in each level, thus reducing in price and weight than the other two above. And also the main uniqueness in this topology is that it has separate DC sources for each bridge. The complexity of the entire system is decreased due to reduced number of switching devices.

IV.DIFFERENT MC-PWM FOR MI

Most widely used pulse width modulation techniques are Space vector modulation (SVM) and multicarrier pulse width modulation (MCPWM) .

The main drawback of SVM is that the number of computations is very large even though the user selects the best switching sequences. Selection of switching states is one more difficult task to implement on practical basis.

To overcome these demerits of SVM, MCPWM are developed. There are different classification of multi carrier pulse width modulations like Level shifted pulse width modulation, Phase disposition pulse width modulation and Phase opposite disposition pulse width modulation etc.

A. Phase disposition pulse width modulation:

Phase disposition PWM has carriers in same phase above and below zero reference line. All the carriers are in same phase in this method of PWM. Most widely used method as it provides load voltage and current with lower harmonic distortion.

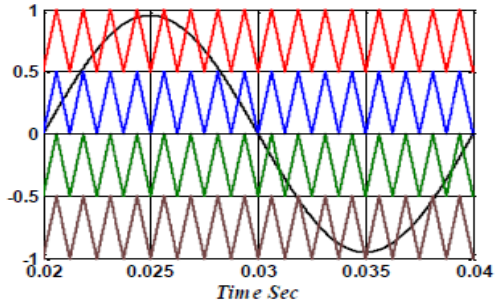

Fig 4:Phase disposition PWM carrier arrangement

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B. Phase opposite disposition pulse width modulation:

Unlike the phase disposition this method has all carriers at the same frequency with adjustable amplitudes. The only difference that it has when compared to the above method is that it has carriers above zero level reference in phase among them but in opposition usually 180 degrees phase shifted with those of below.

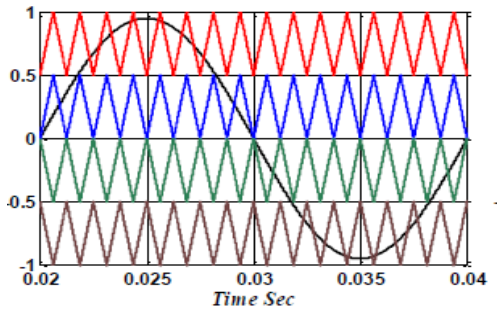

Fig 5: Phase opposite disposition PWM carrier arrangement

C. Alternative phase opposite disposition pulse width modulation:

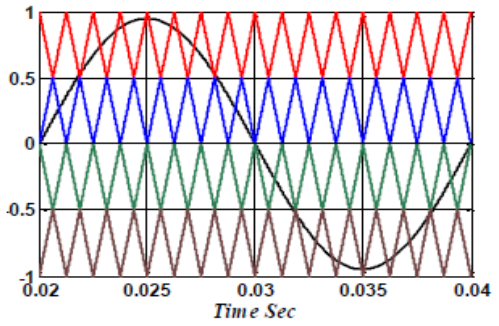

Fig 6:Alternative Phase opposite disposition PWM carrier arrangement.

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Fig 6 shows Alternate phase disposition method. This method of multicarrier pulse width modulation is quite different from the above two which has all the carriers alternately in opposite disposition.

V. PROPOSED SYSTEM

Cascaded H- bridge Multilevel inverter is used in this system which is very simple than the other topologies as it has lesser DC link value per bridge. In the simulation as shown in Fig 7 has grid represented as resistor, as grid has no effect on the leakage current. The MC-PWM that has been applied to the above proposed system is PD-PWM has it has proven to be providing more encouraging results.

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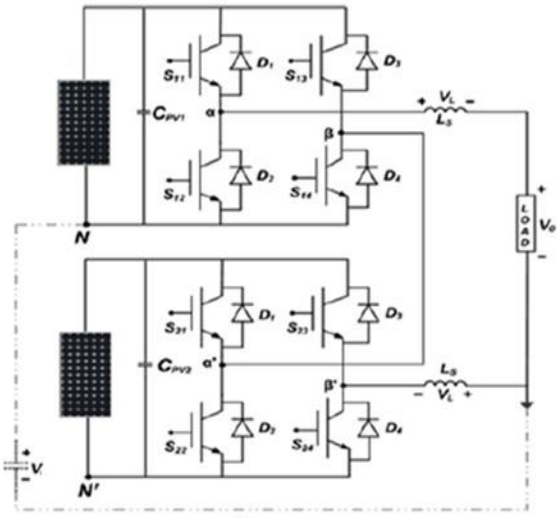

Fig 6: Proposed Single –phase five-level cascaded multilevel inverter

VI. OPEN LOOP SIMULATION

Open loop simulation circuit is as shown in Fig 7, it is done using MATLAB simulation tool, and the values chosen for the simulation is tabulate in the table 1.

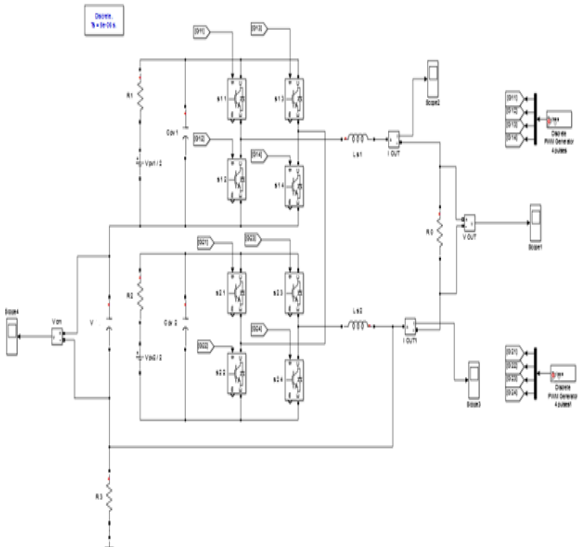

Fig 7: Open loop Simulink mode

The Grid connection at the output of the inverter here is represented as load resistor of value 10K, as the researches have shown that grid has no effect on the leakage current that is flows through PV Panel module to ground, hence it is considered has to be a simple resistor for simplicity in the simulation.

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Table 1. Parameters used in the simulation

Sl no	Parameters	Values considered for simulation
1	PV module	50W
2	DC-link capacitance	2200uF
3	Switching frequency	3KHz
4	Inductance	5mH
5	Load Resistance	10K

Table 1 shows the values that are considered for the open loop simulation. Switching frequency is chosen to be high as the switching losses decreases at higher frequency.

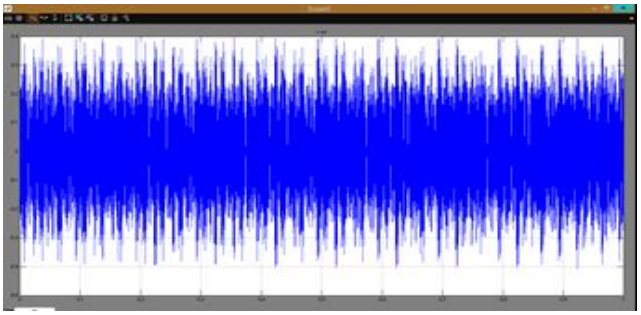

Fig8 : Leakage current of the open loop simulation

Fig 8 shows leakage current of open loop simulation. It was obtained around 0.3 A. This can be further reduced by making the system closed loop. Leakage current of the open loop system when applied with PD-PWM modulation technique on the inverter bridge chosen showed significant effect rather than other conventional carrier based modulation technique.

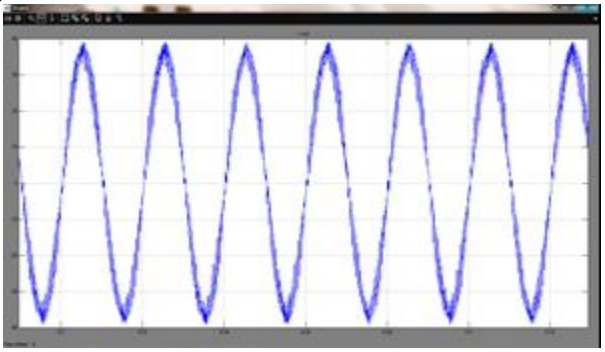

Fig 10: Output voltage of Cascaded H-bridge inverter

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Fig 10 shows output voltage of the chosen topology. The Cascaded H-bridge inverter was given input of 20 V(DC) for each bridge that is cascaded, two PV panels of each giving 20V(DC) output is given as input to the inverter, output of the inverter of 40V (AC) is obtained. The output of the inverter can be increased by increasing the number of bridges cascaded with also increasing the number separate DC sources (PV panel modules).

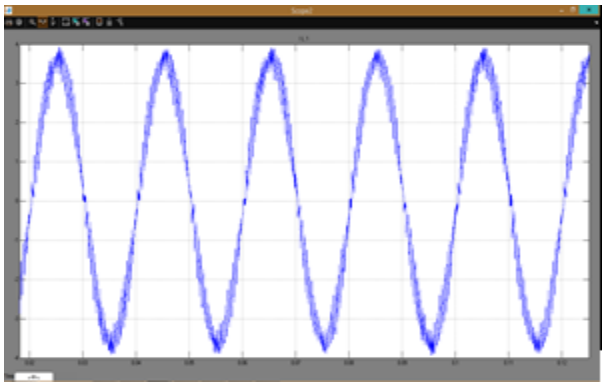

Fig 11: Output current in the Cascaded H-bridge inverter

The output of the proposed topology is shown in Fig 11. It was obtained to be 4A as output voltage is 40V(AC) and with the load resistor of 10K value. The above proposed topology chosen can be further be improved by making it closed loop and also the value of the leakage current can be further decreased and also this avoids the threat to human life.

VII. FUTURE WORK

The closed loop control will be developed using MATLAB Simulation tool, the control will be simulated using PI and PD – PWM modulation technique can be applied of which the results can be compared with the previous results of the open loop system. Using the above results the coding for the PIC controller can be developed for the hardware implementation.

REFERENCES

[1] R. Gonzalez, J. Lopez, P. Sanchis, and L. Marroyo "Transformerless inverter for single-phase photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 693–697, Mar. 2007.

[2] Y. Wensong, L. Jih-Sheng, H. Qian, and C. Hutchens, "High-efficiency MOSFETinverter with H6-type configuration for photovoltaic nonisolated AC-module applications," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1253–1260, Apr. 2011.

[3] Y. Zhou, W. Huang, P. Zhao, and J. Zhao, "A transformerless grid connected photovoltaic system based on the coupled inductor single-stage boost three-phase inverter," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1041–1046, Mar. 2014.

[4] E. Koutroulis and F. Blaabjerg, "Design optimization of transformerless grid-connected PV inverters including reliability," *IEEE Trans. PowerElectron.*, vol. 28, no. 1, pp. 325–335, Jan. 2013.

[5] L. June-Seok and L. Kyo-Beum, "New modulation techniques for a leakage current reduction and a neutral-point voltage balance in transformerless photovoltaic systems using a three-level inverter," *IEEE Trans. PowerElectron.*, vol. 29, no. 4, pp. 1720–1732, Apr. 2014.

[6] Z. Li, S. Kai Sun, F. Lanlan,W. Hongfei, and X. Yan, "A family of neutral point clamped full-bridge topologies for transformerless photovoltaic grid tied inverters," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 730–739, Feb. 2013.

[7] Y. Bo, L. Wuhua, G. Yunjie, C. Wenfeng, and H. Xiangning, "Improved transformerless inverter with common-mode leakage current elimination for a photovoltaic grid-connected power system," *IEEE Trans. PowerElectron.*, vol. 27, no. 2, pp. 752–762, Feb. 2012.

[8] A. M. Hava and E. Un, "A high-performance PWM algorithm for common-mode voltage reduction in three-phase voltage source inverters," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1998–2008, Jul. 2011.

[9] K. Zhou and D. Wang, "Relationship between space-vector modulation and three-phase carrier-based PWM: A comprehensive analysis," *IEEETrans. Ind. Electron.*, vol. 49, no. 1, pp. 186–196, Jan. 2002.

[10] L. P. Chiang, D. G. Holmes, Y. Fukuta, and T. A. Lipo, "Reduced common-mode modulation strategies for cascaded multilevel inverters,"*IEEE Trans. Ind. Appl.*, vol. 39, no. 5, pp. 1386–1395, Sep./Oct. 2003.

[11] L. Poh Chiang, D. G. Holmes, and T. A Lipo, "Implementation and control of distributed PWM cascaded multilevel inverters with minimal harmonic distortion and common-mode voltage," *IEEE Trans. Power Electron.*,vol. 20, no. 1, pp. 90–99, Jan. 2005.