ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 7, July 2015

A Novel Architecture for Inverter Based Double-Tail Comparator

D.Bhavya[1], R. Manoj Kumar [2]

PG Student [Embedded Systems & VLSI Design] , Gayatri Vidya Parishad College of Engineering (Autonomous), Visakhapatnam, Andhra Pradesh, India[1]

Assistant Professor, Dept. of ECE, Gayatri Vidya Parishad College of Engineering (Autonomous), Visakhapatnam, Andhra Pradesh, India[2]

ABSTRACT: Comparators are the common analyzing units in the Analog-to-Digital converters. There is a need to use the high speed and the low power consumption based comparators. Hence, design of comparators is more challenging for smaller supply voltages. In this paper, a conventional Double-tail comparator is implemented. Based on the results, a new Double-tail comparator with low power, low voltage is designed. There is a beter performance for proposed Double-tail comparator in terms of delay and power consumption, when it is compared with conventional Double-tail comparator.

KEYWORDS: Analog-to-Digital converter, Double-tail comparator, Delay, Power consumption.

I.INTRODUCTION

A comparator is a device which is used to sense when an arbitrary varying signal reaches some threshold or reference level. Comparator is a primary building block in most Analog-to-Digital converters. Many high speed ADCs, such as flash ADC, require high speed, low-power comparators with small chip area. Designing high-speed comparator is more important with a low supply voltage. Comparators find application in many electronic systems, providing suitable limit. The comparator outputs may be used to drive logic circuits. Power minimization is important parameter for designers today, especially in the portable electronic-device market, where devices have become increasingly feature rich and power hungry. Low supply voltages play a significant role in determining the power consumption in portable electronic-device circuits. Therefore a Low-voltage, Low-power Double-Tail Comparator design is implemented[1].

II. CONVENTIONAL DOUBLE-TAIL COMPARATOR

Conventional Double-tail comparator[1] is shown in figure 1. In this comparator circuit, the transistor M7-M9 and M8-M10 forms back-to-back connection of inverters, called as regeneration circuit. During the Precharge mode the clock is applied with '0', the transistors Mtail1 and Mtail2 turns off. The transistors M3 and M4 turns on and charge the node fn and fp to V_{dd}. Then the transistors MR1 and MR2 discharges to ground. During the evaluation mode by applying clock with $V_{dd,}$ the transistors Mtail1 and Mtail2 turns on. The transistors M3 and M4 turns off, and the nodes fn and fp starts to drop with different discharging rates. The transistors MR1 and MR2 forms an intermediate stage and passes $\Delta V_{f\,(np)}$ to the latch stage i.e., back-to-back connection of inverters and it provides a good shielding between input and output.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 7, July 2015

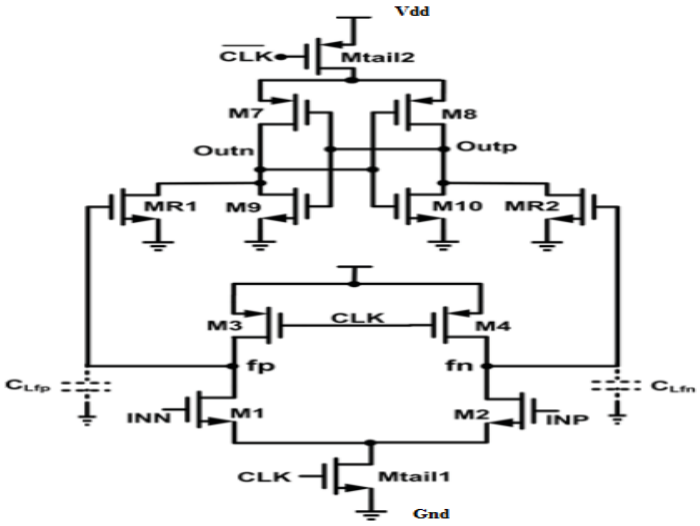

Fig: 1.Conventional Double-tail comparator

III. MODIFIED DOUBLE-TAIL COMPARATOR

The Modified Double-tail comparator[1] is shown in figure 2. As there is better performance for double tail architecture in low-voltage applications, the Modified Double-tail comparator is based on double tail structure. The main idea of this circuit is to increase the speed of regeneration circuit. To increase the regeneration speed, two control transistors MC1 and MC2 are added in cross coupled manner to the conventional double tail comparator. During the Precharge mode by applying clock with zero, the transistors Mtail1 and Mtail2 turns off, thus both the transistors M3 and M4 pulls fn and fp nodes to Vdd. Therefore transistors MC1 and MC2 are in cut-off state. Intermediate stage transistors, MR1 and MR2 discharges both latch output nodes to ground. During evaluation mode by applying clock with V_{dd}, the transistors Mtal1 and Mtail2 turns on, M3 and M4 turns off. At the beginning of the stage, the control transistors are in off state. Since the nodes fn and fp slowly precharge to V_{dd}. Thus fn and fp starts to drop with different discharging rates based on the input voltages applied. If VINP>VINN, then fn drops faster than fp. Since transistor M2 provides more current than M1. As long fn continues falling, the corresponding pmos control transistor, MC1starts to turn on, pulling fp node back to the V_{dd}. As fp node is at voltage V_{dd}, the transistor MR1 turns on and whatever the voltage is present at node outn, it discharges to ground. Mean while the node outp reaches to $V_{dd.}$

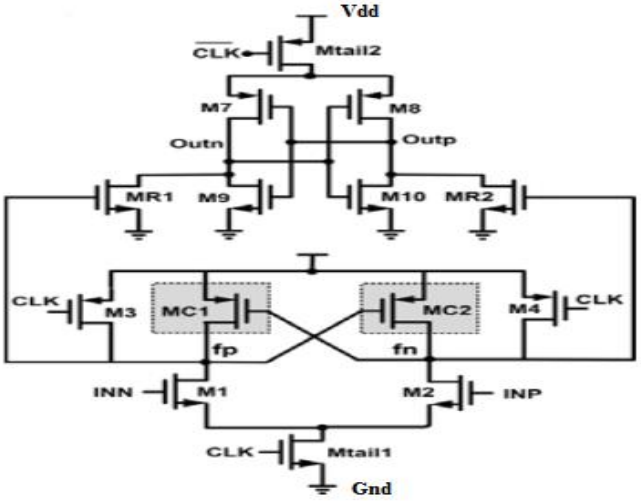

Fig: 2. Modified Double-tail comparator

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 7, July 2015

IV. PROPOSED DOUBLE-TAIL COMPARATOR

Proposed Double-tail comparator i.e. Inverter based Double-tail comparator is shown in figure 3. During the Precharge mode by applying clock with zero, the transistors Mtail1 and Mtail2 turns off, thus M3 and M4 pulls both transistors fn and fp nodes to V_{dd}. Therefore transistors MC1 and MC2 are in cutoff state. Intermediate stage transistors, MR1 and MR2 discharges both latch output nodes to ground. During evaluation mode by applying clock with V_{dd}, the transistors Mtail1 and Mtail2 turns on, M3 and M4 turns off. At the beginning of the stage, the control transistors are in off state. Since the nodes fn and fp Precharged to V_{dd}. The fn and fp nodes starts to drop with different discharging rates based on the input voltages applied. If VINP>VINN, then fn drops faster than fp. Since transistor M2 provides more current than M1. As long fn continues falling, the corresponding pmos control, MC1 starts to turn on, by pulling fp node back to the V_{dd}. So that the transistor MR1 turns on and discharges the node outn to ground, thus the node outp charges to V_{dd}.

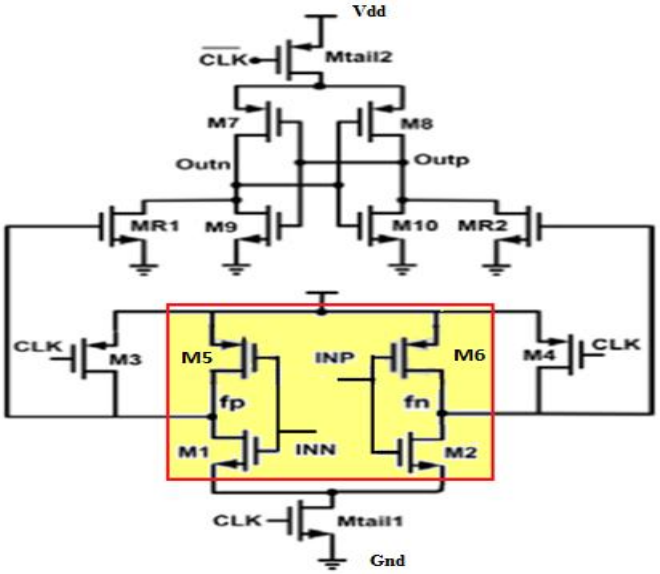

Fig: 3. Proposed Double-tail comparator

V. RESULT AND DISCUSSION

This result is obtained for conventional double-tail comparator from figure 4. For this circuit, outp obtained as 0.8V and outn is 0V when INP>INN.

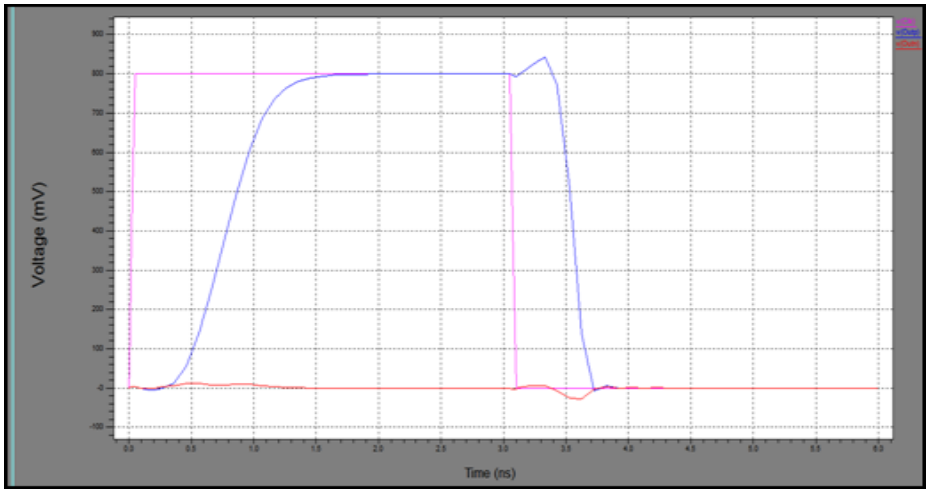

Fig: 4 Transient simulations of the Conventional Double-tail comparator for Vin = 5 mV, Vcm = 0.7 V, and V_{DD} = 0.8 V.packets

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 7, July 2015

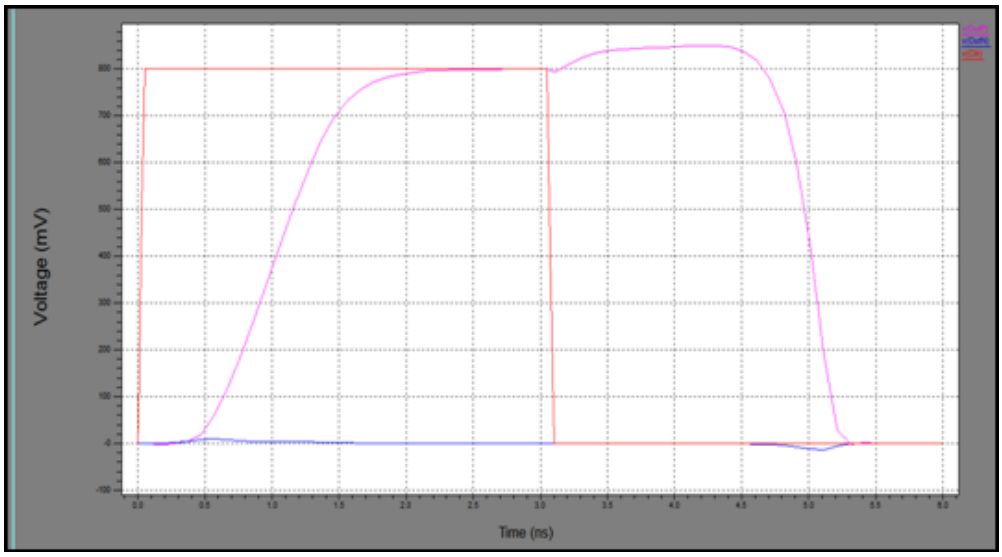

Fig: 5Transient simulations of the Modified Double-tail comparator for Vin = 5 mV, Vcm = 0.7 V, and V_{DD} = 0.8 V.

When INP>INN, the outputs 0.8V and 0V is obtained at 'Outp' and 'Outn' respectively. This result is obtained for modified Double-tail comparator from figure 5.

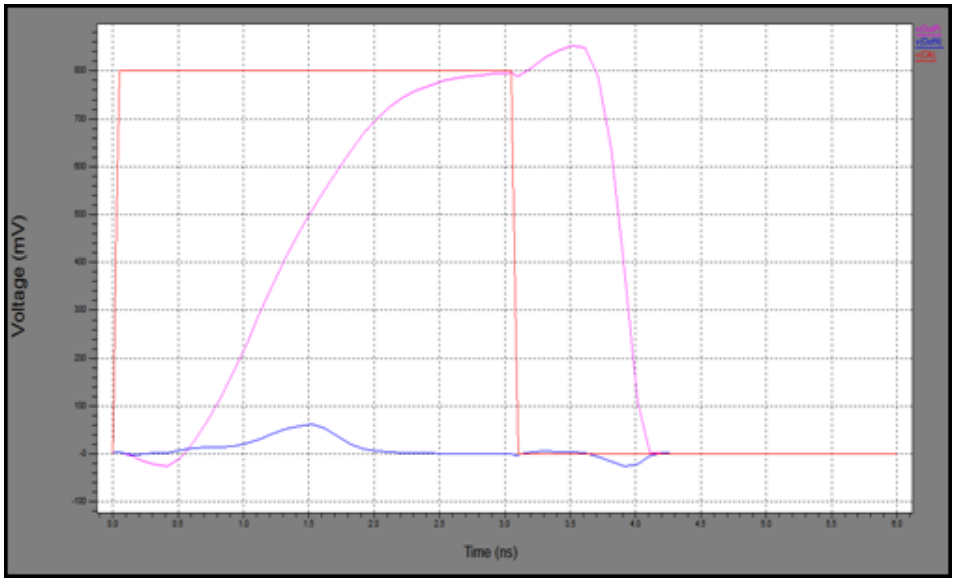

Fig: 6 Transient simulations of the Proposed Double-tail comparator for Vin = 5 mV, Vcm = 0.7 V, and V_{DD} = 0.8 V.

Similar to the above circuit, from the figure 6, the outputs obtained for the proposed circuit are 0.8V and 0V at 'outp' and 'outn' respectively.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 7, July 2015

S.No	Name of the comparator	Technology	No of transistors	Average Power (watts)	Delay (ps)
1	Conventional Double-tail comparator	180nm	12	140.477nW	201
2	Modified Double-tail comparator	180nm	14	132.5327nW	193
3	Proposed comparator	180nm	14	107.955nW	81

Table: 1. Comparison results.

In the table 1, the delay and power consumption values are mentioned for different Double-tail comparators. From that we can say that the delay and power consumption are improved from conventional Double-tail comparator to Proposed Comparator.

VI.CONCLUSION

In this paper, two structures of conventional Double-tail comparator and a Modified Double-tail comparator were implemented and obtained respective simulation results. A new double-tail comparator with low-voltage low-power capability was designed in order to improve the performance of the comparator. From the simulation results, the delay and power consumption of proposed comparator is reduced when compared to other Double-tail comparator circuits. As the Proposed Double-tail comparator has less delay, it can be used in ADC's to yield faster outputs.

REFERENCES

[1] Samaneh Babayan-Mashhadi, "Analysis and design of a low-voltage low- power Double-tail comparator",*IEEE* Trans. Feb-2014.
[2] B. Goll and H. Zimmermann, "A comparator with reduced delay time in 65-nm CMOS for supply voltages down to 0.65," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 56, no. 11, pp. 810–814, Nov. 2009.
[3] S. U. Ay, "A sub-1 volt 10-bit supply boosted SAR ADC design in standard CMOS," *Int. J. Analog Integr. Circuits Signal Process.*, vol. 66, no. 2, pp. 213–221, Feb. 2011.
[4] A.Mesgarani, M.N. Alam, F.Z. Nelson, and S.U. Ay, "Supply boosting technique for designing very low-voltage mixed-signal circuits in standard CMOS," in *Proc. IEEE Int.* Midwest Symp. Circuits Syst. *Dig. Tech. Papers*, Aug. 2010, pp. 893–896.
[5] J. kim, b. s. leibowits, j. ren, and c. j. madden, "simulation and analysis of random decision errors in clocked comparators," *IEEE* trans.circuits syst. i, reg. papers, vol. 56, no. 8, pp. 1844–1857, aug. 2009.