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Modification of Accumulator Based on Weight Patterns

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ABSTRACT: Weighted pseudorandom built-in self test (BIST) schemes have been utilizing the number of vectors to achieve complete fault coverage in BIST applications. Weighted sets comprising three weights, namely 0, 1, 0.5 have been successfully utilized so far for test pattern generation, since they result in both low testing time and low consumed power. Accumulators are commonly found in current VLSI chips, this scheme can be efficiently utilized the hardware of BIST pattern generation, as well. Comparisons with previously presented schemes indicate that the proposed scheme compares favorably with respect to the required hardware.

KEYWORDS: Built-in self test (BIST), test per clock, VLSI testing, weighted test pattern generation.

1. INTRODUCTION

Pseudorandom Built-in Self Test (BIST) generators have been successfully utilized for the testing of integrated circuits and systems. The pseudorandom generators includes Linear Feedback Shift Registers (LFSRs), Cellular Automata and Accumulators accumulating a constant value.

However, Some circuits faults for which large number of random patterns have to be generated before high fault coverage is achieved. Therefore, weighted pseudorandom techniques have been proposed; in weighted pseudorandom techniques inputs are biased by changing the probability of a 0 or a 1 on a given input from 0.5(for pure pseudorandom tests) to some other value. Weighted random pattern methods that rely on a single weight assignment, usually fail to achieve complete fault coverage using a reasonable number of test patterns, Since, although the weights are computed to be suitable for most faults, some faults may require long test sequences to be detected with weight assignments that do not match their activation and propagation requirements.

Proposed method that dynamically walks through the range of possible test generation approaches, starting from pure pseudorandom tests to detect easy-to-detect faults at low hardware cost, then reducing the number of inputs which are allowed to be specified randomly, fixing an increasing number of the inputs to 0 or 1 according to a given deterministic test set, to detect faults that have more requirements on input values and cannot be detected by a purely random sequence of reasonable length. Thus, the method proposed it can be viewed as a weighted random test generation method that uses three weights: 0, 0.5 and 1. A weight of 0 corresponds to fixing an input to 0; a weight of 1 corresponds to fixing an input to 1; and a weight of 0.5 indicates pure random values. Consequently, every weight is generated using a single LFSR cell primary input, and a small number of logic gates to account for the weights 0 and 1. Current VLSI circuits, e.g. data path architectures, or digital signal processing chips commonly contain arithmetic modules. Utilizing accumulators for Built-in Testing has been shown to result in low hardware overhead and low impact on the circuit normal operating speed. It was proved that the test vectors generated by an accumulator whose inputs are driven by a constant pattern can have quit good pseudorandom characteristics,

In this paper, an Accumulator Based test pattern generation scheme that compares favorably to previously proposed schemes. It was proved that the test vectors generated by an accumulator whose inputs are driven by a constant pattern

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can have acceptable pseudorandom characteristics, if the input pattern is properly selected. However, modules containing hard-to-detect faults still require extra test hardware either by inserting test points into the mission logic or by storing additional deterministic test patterns [13].

In order to overcome this problem, an accumulator-based weighted pattern generation scheme was proposed .the scheme generates test patterns having one of three weights, namely 0,1,0.5 therefore it can be utilized to reduce the test application time in accumulator-based test pattern generation, However, the scheme proposed three major drawback: 1) it can be utilized only in the case that the adder of the accumulator is a ripple carry adder; 2) it requires redesigning the accumulator; this modification, apart from being costly, requires redesign of the core of the datapath, a practice that is generally discouraged in current BIST schemes; and 3) it increases delay, since it affects the normal operating speed of the adder.

Accumulator-based 3-weight generation is presented. The proposed scheme copes with the inherent drawbacks of the scheme proposed [12]. 1) it does not impose any requirements about the design of the adder(i.e., it can be implemented using any adder design); 2) it does not require any modification of the adder; and hence. 3) does not affect the operating speed of the adder. Furthermore, the proposed scheme compares favorably to the scheme proposed in and in terms of the required hardware overhead.

TABLE I

TRUTH TABLE OF THE FULL ADDER

#	Cin	A[i]	B[i]	S[i]	Cout	Comment
1	0	0	0	0	0	
2	**0**	0	1	1	**0**	Cout=Cin
3	**0**	1	0	1	**0**	Cout=Cin
4	0	1	1	0	1	
5	1	0	0	1	0	
6	**1**	0	1	0	**1**	Cout=Cin
7	**1**	1	0	0	**1**	Cout=Cin
8	1	1	1	1	1	

II. DESIGN METHODOLOGY

The implementation of the weight Pattern Generator scheme is based on the full adder truth table, presented in Table I. From Table I we can see that in lines #2,#3,#6, and #7 of the truth table, Cout=Cin. Therefore, in order to transfer the carry input to the carry output, it is enough to set A[i]= NOT(B[i]). The proposed scheme is based on this observation [1-2].

The implementation of the proposed weighted pattern generation scheme is based on the accumulator cell presented in Fig 1, which consists of a Full Adder cell and a D-type flip-flop with asynchronous set and reset inputs whose output is also driven to one of the full adder inputs. In Fig 1, We assume, without loss of generality, that the set and reset the active high signals. In the same figure the respective cell of the driving regiser B[i] is also shown. For this accumulator cell, one of three configurations can be utilized, as shown in Fig.2 .

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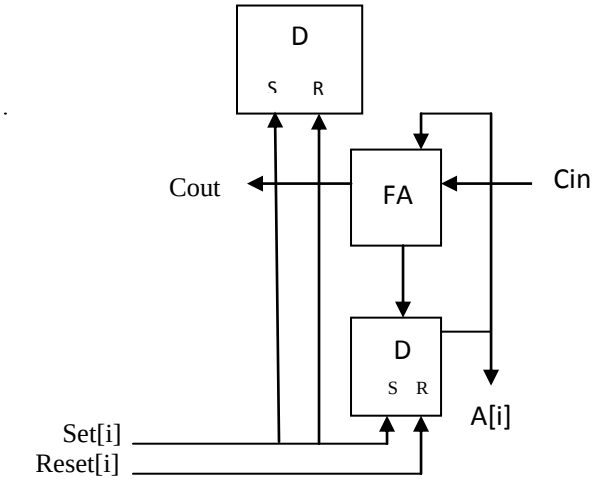
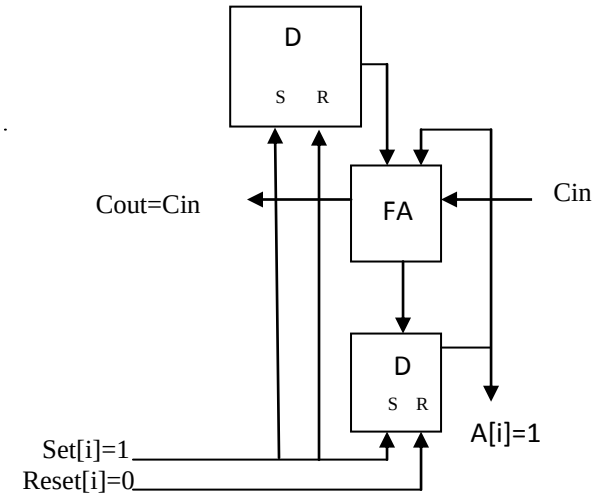


In Fig.2(a) we present the configuration that drives the CUT inputs when A[i] =1 is required. Set[i]=1 and Reset[i] =0 and hence A[i] =1 and B[i] =0. Then the output is equal to 1, and Cin is transferred to Cout [3-4].

In Fig.2(b), we presented the configuration that drives the CUT inputs when A[i] =0 is required . Set[i] =0 and Reset[i]= 1 and hence A[i] =0 and B[i] =1.Then , the output is equal to 0 and Cin is transferred to Cout.

In Fig.2(c), we present the configuration that drives the CUT inputs when A[i]= "--" is required. Set[i]=0 and Reset[i] =0. The D input of the flip-flop of register B is driven by either 1 or 0, depending on the value that will be added to the accumulator inputs of the CUT [10-11].

In Fig.3, the general configuration of the proposed scheme is presented. The Logic module provided the Set[n-1:0] and Reset[n-1:0] signals that drive the S and R inputs of the Register A and Register B inputs. Note that the signals that drive the S inputs of the flip-flop of Register B and vice versa [5].



(a)

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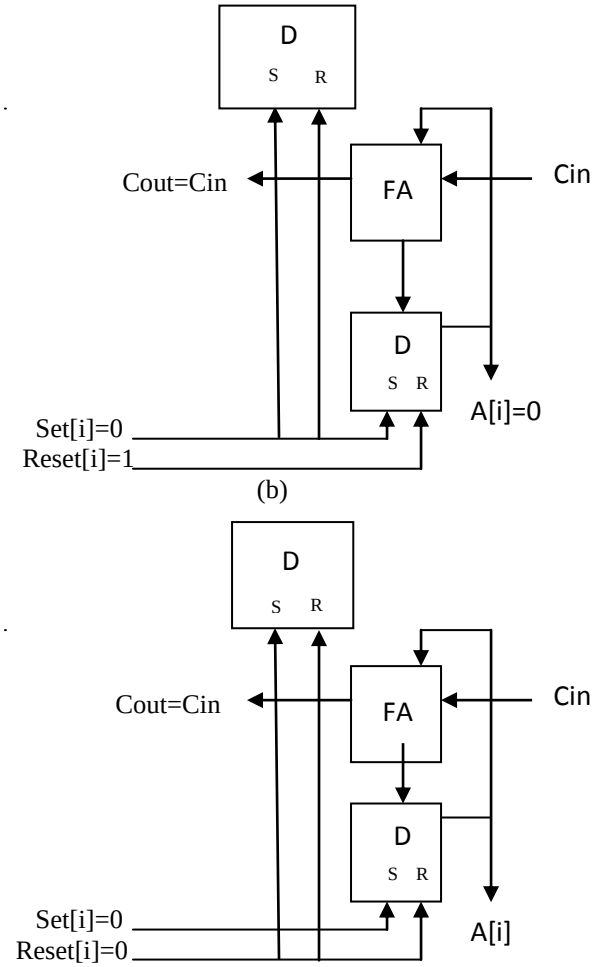

Fig. 2 Configurations of the accumulator cell of Fig.1

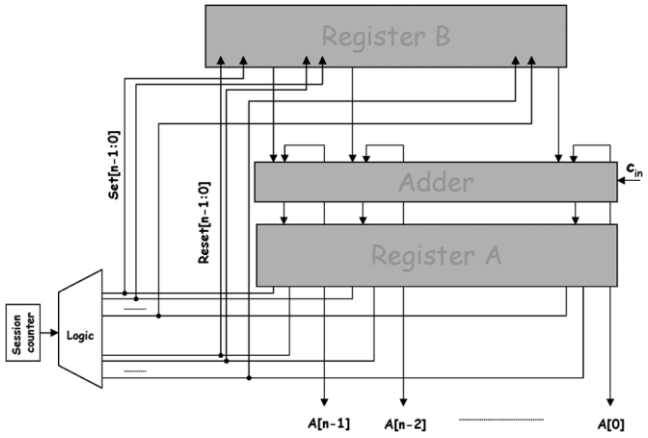

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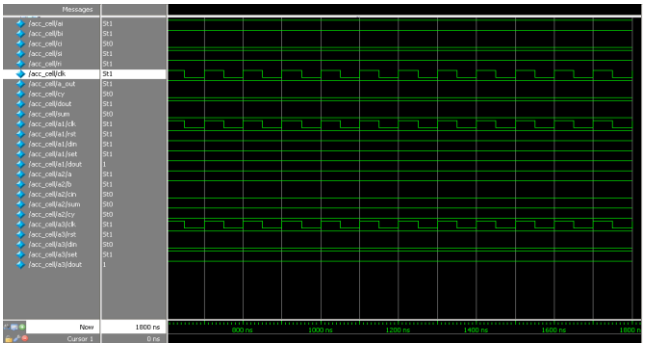
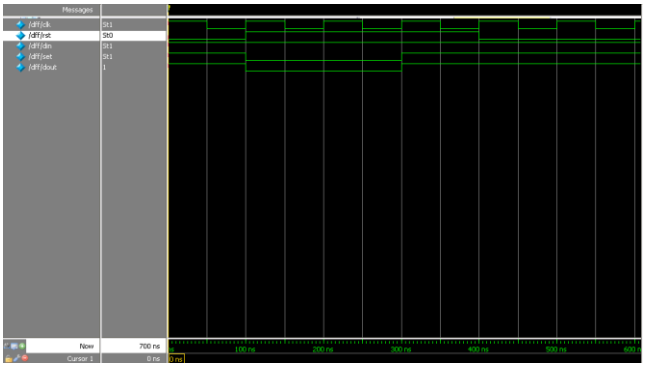
Fig. 3. Proposed Scheme

Weighted –pattern generation schemes require a session counter in order to alter amoung the different weight sessions; the session counter consists of $\log_2 k$ bits, where k is the number of test sessions (i.e., weight assignment) of the weighted test set [6], [9]. The scheme proposed in requires the redesign of the adder; more precisely, two NAND gates are inserted in each cell of the ripple carry adder. In order to provide the inputs to the set and reset input of the flip flops, decoding logic is implemented. For the proposed scheme, no modification is imposed on the adder of the accumulator. Therefore , there is no impact on the data path timing characteristics [7-8].

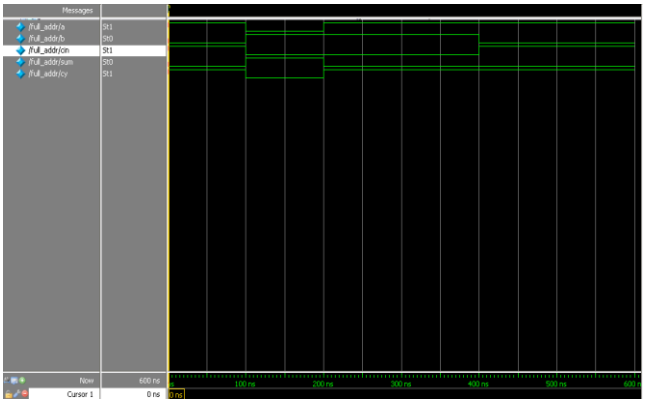
III. ACCUMULATOR



2. D-FLIPFLOP



3. FULL ADDER



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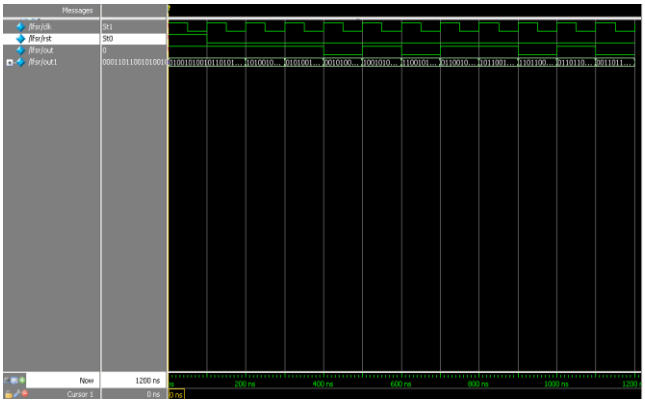
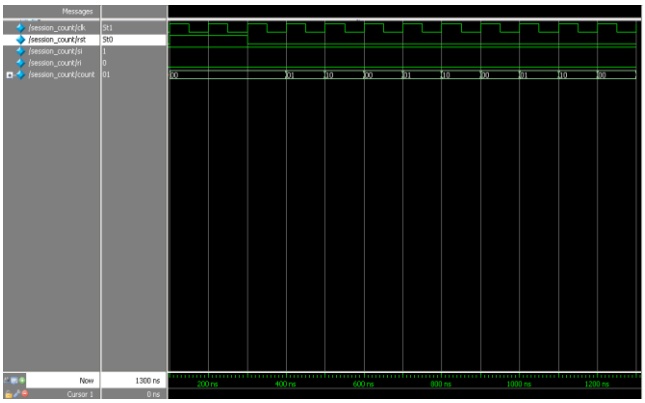
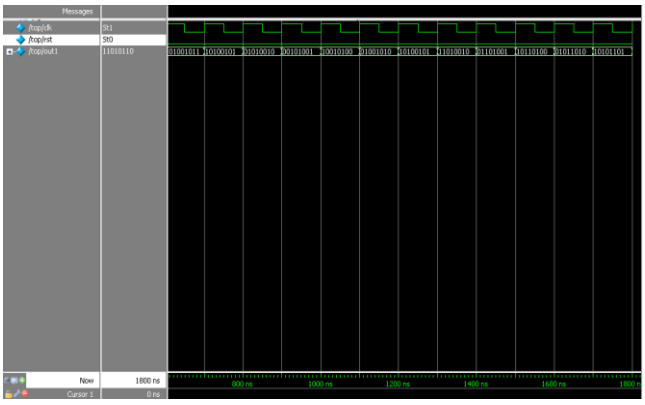
4. LINEAR FEEDBACK SHIFT REGISTER



5. SESSION COUNTER



6. TOP MODULE



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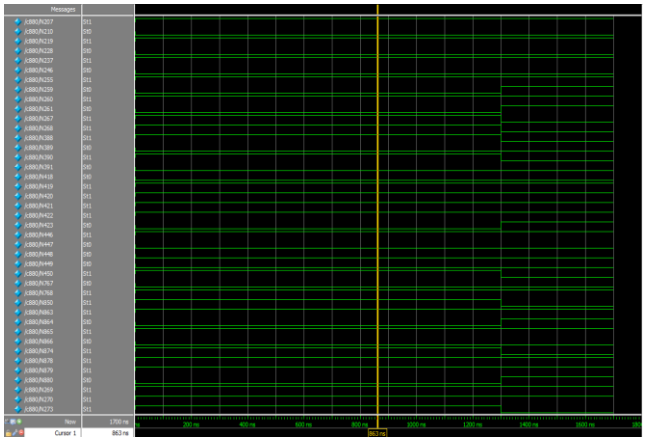
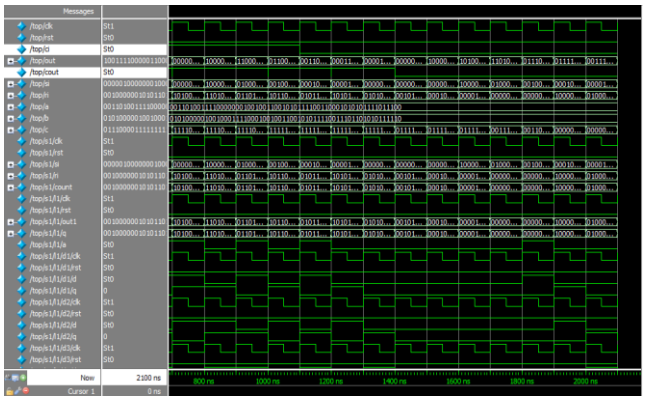
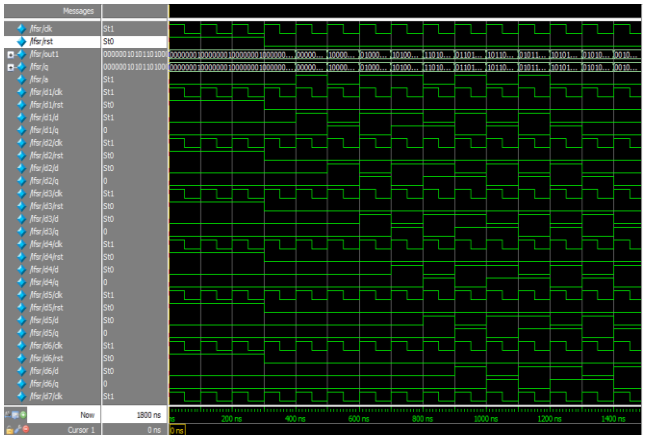
C880 BENCHMARK CIRCUIT



TOPMODULE FOR BENCHMARK CIRCUIT



LFSR FOR BENCHMARK CIRCUIT



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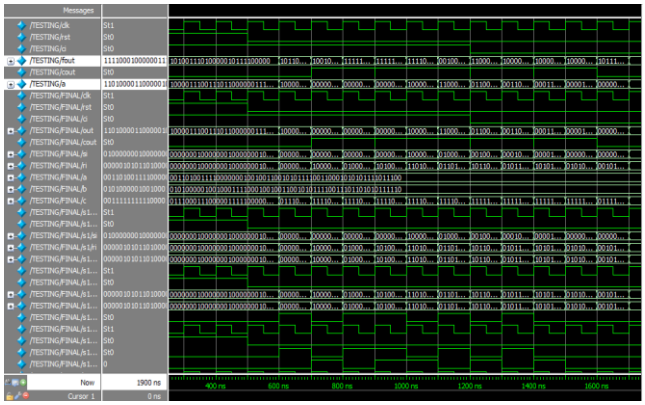
BENCHMARK CIRCUIT WITH TOPMODULE



IV. CONCLUSION

We have presented an accumulator-based 3-weight (0,0.5, and 1) test-per-clock generation scheme, which can be utilized to efficiently generate weighted pattern without altering the structure of the adder.

Comparisons with a previously proposed accumulator-based 3-weight pattern generation technique indicate that the hardware overhead of the proposed scheme is lower (75%), while at the same time no redesign of the accumulator is imposed, thus reduction of 20%--95% in test application time. Comparison with scan based schemes show that the proposed schemes results in lower hardware overhead. Finally, comparisons with the accumulator-based scheme proposed in reveal that the proposed scheme results in significant decrease (95%) in hardware overhead.

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