ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 7, July 2015

Design of Area Efficient Pulse Triggered Flip-Flop Using Inverter Replaced by a NMOS Gate

D.P.Balasubramanian[1], S. Philomina[*2]

Assistant Professor, Dept. of ECE, Jerusalem College of Engineering, Chennai, Tamil Nadu, India [1]

Assistant Professor, Dept. of ECE, Bharath University, Chennai, Tamil Nadu, India[2]

* Corresponding Author

ABSTRACT: The pulse generation logic replaces two input AND gate by a transmission gate which reduces the circuit complexity and hence the overall area is reduced. Pulses for discharging are generated only when there is a need, so this reduces circuit activity and also provides faster discharge operation. So the extra power consumed can also be eliminated. The delay inverters which consume more power for stretching the pulse width are replaced by the PMOS transistors. Transistor sizes are also reduced to provide area and power saving. Power consumption is reduced compared to conventional methods.

KEYWORDS: Pulse triggered, low power, flip-flop

I. INTRODUCTION

Despite these advantages, pulse generation circuitry requires delicate pulse width control in the face of process variation and the configuration of pulse clock distribution network [4].

Depending on the method of pulse generation, P-FF designs can be classified as implicit or explicit [6]. In an implicit-type P-FF, the pulse generator is a built-in logic of the latch design, and no explicit pulse signals are generated. In an explicit-type P-FF, the designs of pulse generator and latch are separate. Implicit pulse generation is often considered to be more power efficient than explicit pulse generation. This is because the former merely controls the discharging path while the latter needs to physically generate a pulse train. Implicit-type designs, however, face a lengthened discharging path in latch design, which leads to inferior timing characteristics. The situation deteriorates further when low-power techniques such as conditional capture, conditional pre-charge, conditional discharge, or conditional data mapping are applied [7]–[10]. As a consequence, the transistors of pulse generation logic are often enlarged to assure that the generated pulses are sufficiently wide to trigger the data capturing of the latch. Explicit-type P-FF designs face a similar pulse width control issue, but the problem is further complicated in the presence of a large capacitive load, e.g., when one pulse generator is shared among several latches.

II. IMPLICIT-TYPE P-FF DESIGN WITH PULSE CONTROL SCHEME

A. ip-DCO(implicit pulsed-Data Close to Output)

Some conventional implicit-type P-FF designs, which are used as the reference designs in later performance comparisons, are first reviewed. A state-of-the-art P-FF design, named ip-DCO, is given in Fig 1(a) [6]. It contains an AND logic-based pulse generator and a semi-dynamic structured latch design. Inverters I5 and I6 are used to latch data and inverters I7 and I8 are used to hold the internal node. The pulse generator takes complementary and delay skewed clock signals to generate a transparent window equal in size to the delay by inverters I1-I3. Two practical problems exist in this design. First, during the rising edge, nMOS transistors N2 and N3 are turned on.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 7, July 2015

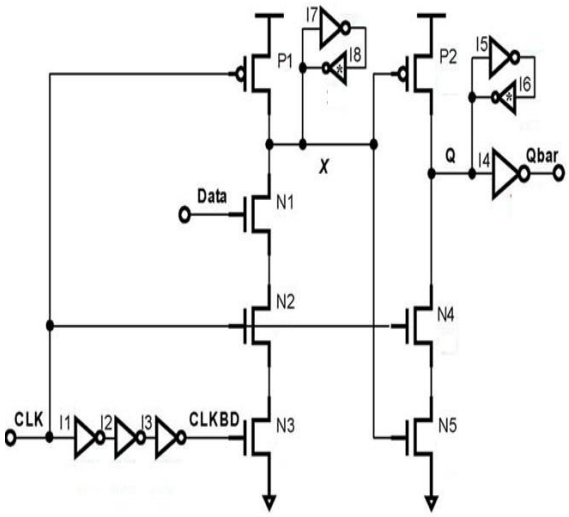

Figure 1(a). ip-DCO

B. MHLLF(Modified Hybrid Latch Flip-flop)

An improved P-FF design, named MHLLF Fig.1 (b) MHLLF, by employing a static latch structure presented in [10]. Node is no longer pre charged periodically by the clock signal. A weak pull-up transistor P1 controlled by the FF output signal Q is used to maintain the node level at high when Q is zero. This design eliminates the unnecessary discharging problem at node. However, it encounters a longer Data-to-Q (D-to-Q) delay during "0" to "1" transitions because node is not pre-discharged. Larger transistors N3 and N4 are required to enhance the discharging capability [5]. Another drawback of this design is that node becomes floating when output Q and input Data both equal to "1 ". Extra DC power emerges if node X is drifted from an intact "1".

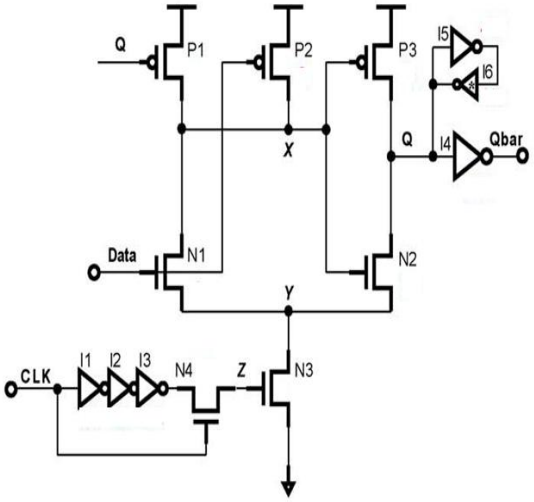

Figure 1 (b). MHLLF

C. SCCER(Single Ended Conditional Capture Energy Recovery)

A refined low power P-FF design named SCCER using a conditional discharged technique [9], [8]. In this design, the keeper logic (back-to-back inverters I7 and I8 in Fig. 1(a) is replaced by a weak pull up transistor P1 in

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 7, July 2015

conjunction with an inverter I2 to reduce the load capacitance of node [8]. The discharge path contains nMOS transistors N2 and N1 connected in series. In order to eliminate superfluous switching at node, an extra nMOS transistor N3 is employed. Since N3 is controlled by Q_fdbk, no discharge occurs if input data remains high. The worst case timing of this design occurs when input data is "1" and node is discharged through four transistors in series, i.e., N1 through N4, while combating with the pull up transistor P1. A powerful pull-down circuitry is thus needed to ensure node can be properly discharged. This implies wider N1 and N2 transistors and a longer delay from the delay inverter I1 to widen the discharge pulse width.

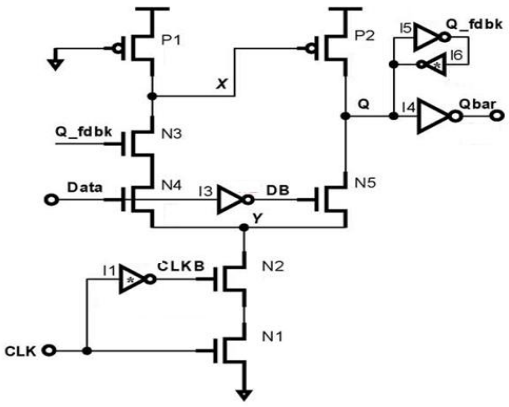

Figure 1(c). SCCER

D. P-FF Design with conditional pulse enhancement scheme

The design, as shown in Fig. 1(d), adopts two measures to overcome the problems associated with existing P-FF designs. The first one is reducing the number of nMOS transistors stacked in the discharging path. The second one is supporting a mechanism to conditionally enhance the pull down strength when input data is "1." Refer to Fig. 1(d), the upper part latch design is similar to the one employed in SCCER design [12]. As opposed to the transistor stacking design in Fig. 1(a) and (c), transistor N2 is removed from the discharging path.Transistor N2, in conjunction with an additional transistor N3, forms a two-input pass transistor logic (PTL)-based AND gate [13], [14] to control the discharge of transistor N1. Since the two inputs to the AND logic are mostly complementary (except during the transition edges of the clock), the output node is kept at zero most of the time. When both input signals equal to "0" (during the falling edges of the clock), temporary floating at node is basically harmless. At the rising edges of the clock, both transistors N2 and N3 are turned on and collaborate to pass a weak logic high to node , which then turns on transistor N1 by a time span defined by the delay inverter I1. The switching power at node can be reduced due to a diminished voltage swing. Unlike the MHLLF design [11], where the discharge control signal is driven by a single transistor, parallel conduction of two nMOS transistors (N2 and N3) speeds up the operations of pulse generation.With this design measure, the number of stacked transistors along the discharging path is reduced and the sizes of transistors N1-N5 can be reduced also.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 7, July 2015

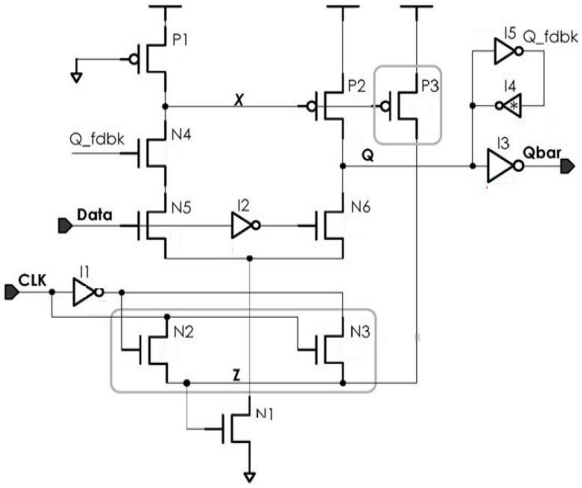

Figure 1(d). *P-FF Design with conditional pulse enhancement scheme*

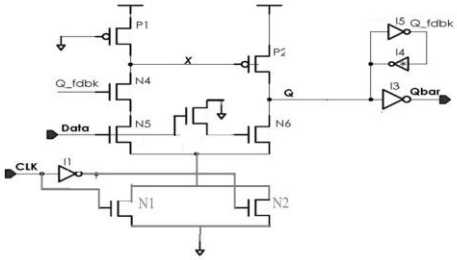

Figure 2 .Proposed design

III. PROPOSED DESIGN

*The de*sign is shown in figure 2. It overcomes the problem of the above described flip-flop. Referring figure 1© , the proposed design is similar to it in case of latching circuit and it differs only in the pulse generation circuit. It replaces two-input pass transistor logic (PTL)-based AND gate by a transmission gate and N1 and P3 is removed from the design. nMOS pass transistor logic passes only strong 0 whereas transmission gate passes strong 0 and strong 1. By doing so we get reduced transistor count and hence area gets reduced which is an important criteria in this modern era with the improved VLSI technology [1-2]. Use of transmission gate reduces the voltage drop across the pass transistor and hence power dissipation gets reduced. It also doubles the area and interconnects but the overall size of the circuit gets reduced. At rising edge of the clock N1 turns on and at falling edge of the clock N2 gets turns on. If both clock and Data are high transistors N1, N5, N4 and P2 turns on while N2 and N6 turns off. If data is low transistor N6 turns on and transistor N5 turns off [3]. Hence output occurs with low switching activity.In this design the inverter between N5 and N6 is also replaced by a single NMOS transistor,so as to reduce the transistor count further and also reduce the power consumption

IV. SIMULATION RESULTS

The simulation is mainly done sing microwind where the power consumption is shown on the bottom portion of the window,while the main part in the window is composd of sub graphs which show the v-I relation and also v-t relation of input and output.. Generate the layout again and run the simulations till you achieve your target

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 7, July 2015

delays. Depending on the input the output simulated and is observed in the simulation window . To demonstrate the optimality of the proposed design, post layout simulations on various P-FF designs were conducted to obtain their performance figures.

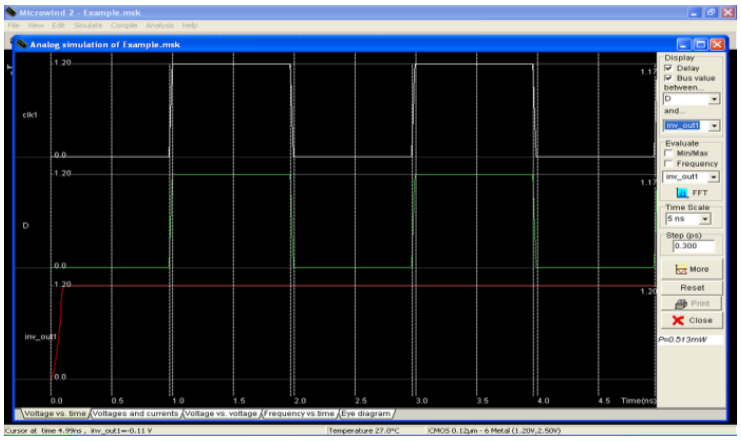

Figure 3(b) Transistor count in tanner

These designs include the three P-FF designs shown in Fig. 1 (ip-DCO [16], MHLLF [9], SCCER [15]), another P-FF design called conditional capture FF (CCFF) [7], and two other non-pulse-triggered FF designs, i.e., a sense-amplifier-based FF (SAFF) [2], and a conventional transmission gate-based FF (TGFF). The target technology is the UMC 90-nm CMOS process. The operating condition used in simulations is 500 MHz/1.0 V which can be seen from the time period of the clk pulse through the wave form windoow. Since pulse width design is crucial to the correctness of data capturing as well as the power consumption, the pulse generator logic in all designs are first sized to function properly across process variation [17]. All designs are further optimized subject to the tradeoff between power and D-to-Q delay, i.e., minimizing the product of the two terms.

COMPARISON TABLE

FF	*Ip-DCO*	*MHLLF*	*SCCER*	*PFF*	*Propoed*
Transistor Count	*23*	*19*	*17*	*19*	*16*
Power (µw)	*41.48*	*32.48*	*35.18*	*30.65*	*27.32*

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 7, July 2015

V. CONCLUSION

In this paper, the various pulse triggered and normal Flip-flop design like, ip-DCO, MHLLF and SCCER were discussed. These were also designed in Microwind tool and the result compared in the form of transistor count and power. With these all results analysis the proposed design performed better than the other design.

REFERENCES

[1] H. Kawaguchi and T. Sakurai, "A reduced clock-swing flip-flop (RCSFF) for 63% power reduction," *IEEE J. Solid-State Circuits*, vol.33, no. 5, pp. 807-811, May 1998.
[2] A. G. M. Strollo, D. De Caro, E. Napoli, and N. Petra, "A novel high speed sense-amplifier-based flip-flop,"*IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 13, no. 11, pp. 1266-1274, Nov. 2005.
[3] Shanthi B., Revathy C., Devi A.J.M., Subhashree, "Effect of iron deficiency on glycation of haemoglobin in nondiabetics", Journal of Clinical and Diagnostic Research, ISSN : 0973 - 709X, 7(1) (2013) pp.15-17.
[4] H. Partovi, R. Burd, U. Salim, F. Weber, L. DiGregorio, and D. Draper, "Flow-through latch and edge-triggered flip-flop hybrid elements," in *IEEE Tech. Dig. ISSCC*, 1996, pp. 138-139
[5] F. Klass, C. Amir, A. Das, K. Aingaran, C. Truong, R. Wang, A. Mehta, R. Heald, and G. Yee, "A new family of semi-dynamic and dynamic flip flops with embedded logic for high-performance processors," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 712-716, May 1999.
[6] Jeyanthi Rebecca L., Dhanalakshmi V., Sharmila S., "Effect of the extract of Ulva sp on pathogenic microorganisms", Journal of Chemical and Pharmaceutical Research, ISSN : 0975 – 7384 , 4(11) (2012) pp.4875-4878.
[7] S. D. Naffziger, G. Colon-Bonet, T.Fischer, R. Riedlinger, T.J.Sullivan, andT.Grutkowski, "The implementation of the Itanium 2 microprocessor," *IEEE J. Solid-State Circuits*, vol. 37, no. 11, pp.1448-1460, Nov. 2002.
[8] J. Tschanz, S. Narendra, Z. Chen, S. Borkar, M. Sachdev, and V. De, "Comparative delay and energy of single edge-triggered and dual edge triggered pulsed flip-flops for high-performance microprocessors," in Proc. ISPLED, 2001, pp. 207-212.
[9] Menon R., Kiran C.M., "Concomitant presentation of alopecia areata in siblings: A rare occurrence", International Journal of Trichology, ISSN : 0974-7753, 4(2) (2012) pp.86-88.
[10] B. Kong, S. Kim, and Y. Jun, "Conditional-capture flip-flop for statis- tical power reduction," *IEEE J. Solid-State Circuits*, vol. 36, no. 8, pp.1263-1271, Aug. 2001.
[11] Rayen R., Hariharan V.S., Elavazhagan N., Kamalendran N., Varadarajan R., "Dental management of hemophiliac child under general anesthesia", Journal of Indian Society of Pedodontics and Preventive Dentistry, ISSN : 0970-4388, 29(1) (2011) pp.74-79.
[12] N. Nedovic, M. Aleksic, and V. G. Oklobdzija"Conditional precharge techniques for power-efficient dual-edge clocking," in Proc. Int. Symp. Low-Power Electron. Design, Monterey, CA, Aug. 12-14, 2002, pp. 56-59.
[13] P. Zhao, T. Darwish, and M. Bayoumi, "High-performance and low power conditional discharge flip- flop," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 12, no. 5, pp. 477-484, May 2004.
[14] Sharmila S., Rebecca L.J., Saduzzaman M., "Effect of plant extracts on the treatment of paint industry effluent", International Journal of Pharma and Bio Sciences, ISSN : 0975-6299, 4(3) (2013) pp.B678-B686.
[15] C. K. Teh, M. Hamada, T. Fujita, H. Hara, N. Ikumi, and Y. Oowaki, "Conditional data mapping flip-flops for low-power and high-perfor-mance systems," *IEEE Trans. Very Large Scale Integr. (VLSI) Systems*, vol. 14, pp. 1379-1383, Dec. 2006.
[16] A.Selvakumar and T.Prabakaran "Design of pulse triggered flip-flop using pulse enhancement scheme," in *IJCER, vol. 2,no.2 march 2012.*
[17] Design of Low Power Negative Pulse-Triggeredflip Flop with Enhanced Latch D.S.R.Krishna kaala D.V.Ramana(M.Tech (VLSI & ES), E.C.E GMRIT J.N.T.U (Kakinada)India IOSR Journal of VLSI and Signal Processing (IOSR JVSP) Volume 3, Issue 3 (Sep. Oct. 2013), PP 06-12e-ISSN: 2319 –4200, p-ISSN No. : 2319 –4197
[18] B Karthik, TVUK Kumar, Noise Removal Using Mixtures of Projected Gaussian Scale Mixtures, World Applied Sciences Journal, 29(8), pp 1039-1045, 2014.
[19] Daimiwal, Nivedita; Sundhararajan, M; Shriram, Revati; , Non Invasive FNIR and FMRI system for Brain Mapping .
[20] Daimiwal, Nivedita; Sundhararajan, M; , Functional MRI Study for Eye Blinking and Finger Tapping.
[21] Shriram, Revati; Sundhararajan, M; Daimiwal, Nivedita; , Effect of change in intensity of infrared LED on a photoplethysmogramIEEE Communications and Signal Processing (ICCSP), 2014 International Conference on, PP 1064-1067,2014.
[22] Kanniga, E; Srikanth, SMK; Sundhararajan, M; , Optimization Solution of Equal Dimension Boxes in Container Loading Problem using a Permutation Block AlgorithmIndian Journal of Science and Technology, V-7, I-S5,PP 22-26, 2014.
[23] Muralibabu, K; Sundhararajan, M; , PAPR performance improvement in OFDM system using DCT based on adjacent symbol groupingTrans Tech Publ, Applied Mechanics and Materials, V-550,PP 204-209, 2014