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# A LED Driver Design based on Fly-back Convert without Auxiliary winding

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**ABSTRACT:** For boosting and taking advantage of itsmany outstanding advantages, LED needsespecially designed power supplies driver. Based on fly-back convert topology, a LED driver design is proposed but without auxiliary winding. According to the fly-back ampere-turns ratio conservation, the peak current through secondary side can be specified. The ratio of the interval time of secondary side flowing current to the switching period can also be set under performance of Zero Cross Detection schematic. In the role of filter and charge conservation, the output drive current will be constant. A more stable operation condition can be controlled by limiting the maximum and minimum interval time of secondary side flowing current. The elaborate adjust circuit in ZCD can magnify the resonance signal for better catching ring signal. Simulation results meet the schematic theoretical analysis and design specification.

**KEYWORDS:** LED,power supply, fly-back, auxiliary winding, ZCD

## I. INTRODUCTION

Light Emitting Diode (LED) is widely used in vehicles and traffic lights, house and street lighting, commercial signs and so on. By concerning its outstanding characteristics, like high theoreticalluminous efficacy, long lifetime, environmentally friendly, chromatic variety, LED will be the trend in lighting[1].

For boosting and taking advantage the aforementioned advantages, LED need new power supply topology especially designed for them. In general, LED driver uses photoelectric couple in secondary side feedback solutionor auxiliary winding in primary side feedback solution to detect drivecurrent. Inevitability, it reduces the effect of isolation which has been widely used in LED driver for safety and both raises the manufacturing cost accordingly[2,3].

Based on the fly-back ampere-turns ratio conservation, the peak current on secondary side can be specified. The ratio of the interval of secondary side flowing current to the switching period can also be achieved under performance of Zero Cross Detection schematic. In the role of filter and charge conservation, the output drive current is constant. A more stable operation condition can be controlled by limiting the maximum and minimum time of secondary side flowing current. The elaborate adjust circuit in ZCD magnify the resonance signal[4,5].

## II. FLY-BACK TOPOLOGY

Fig.1 shows the topology schematic based on fly-back converter used in the proposed driver design. Itconsists of Rectifier Bridge, power up capacitor, fly-back transformer without auxiliary, filter capacitor, and RCD for absorption peak pulse. The off chip Power NMOS is for its parasitic capacitors $C_{dss}$ and $C_{gss}$ which is vital in resonance for Zero Cross Detection (ZCD). The on chip Switch NMOS can be used to turn on or turn off the primary current. The energy stored in transformer is delivered to secondary load side in each cycle[6,7,8,9].

There are three different current states in discontinuous mode fly-back converter. As depicted in Fig.2 (a), when Switch NMOS turns on, except bridge diodes,all rectifier diodesbecome reverse-biased, and alloutput load currents are supplied from the output filter capacitors. The transformer acts like apure inductor and primary current builds up linearly in it to a peak value. When Switch NMOS turns off, all winding voltages reverse under fly-back action, bringingthe output diode into conduction and the primary stored energy $1/2\,L_P I_{ppk}^2$ isdelivered to the output to supply load current and replenish the charge onthe output capacitors[8], as shown in Fig.2 (b).

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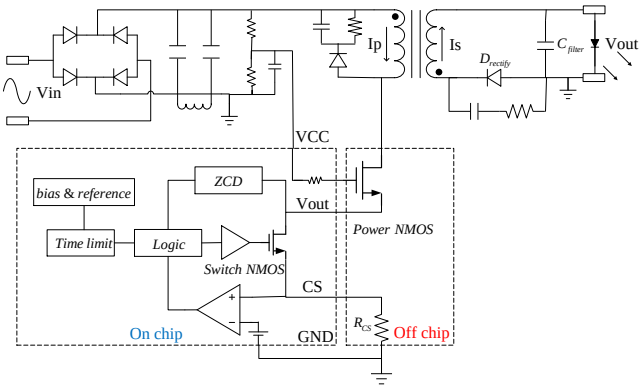


Fig. 1. Topology based on fly-back convert

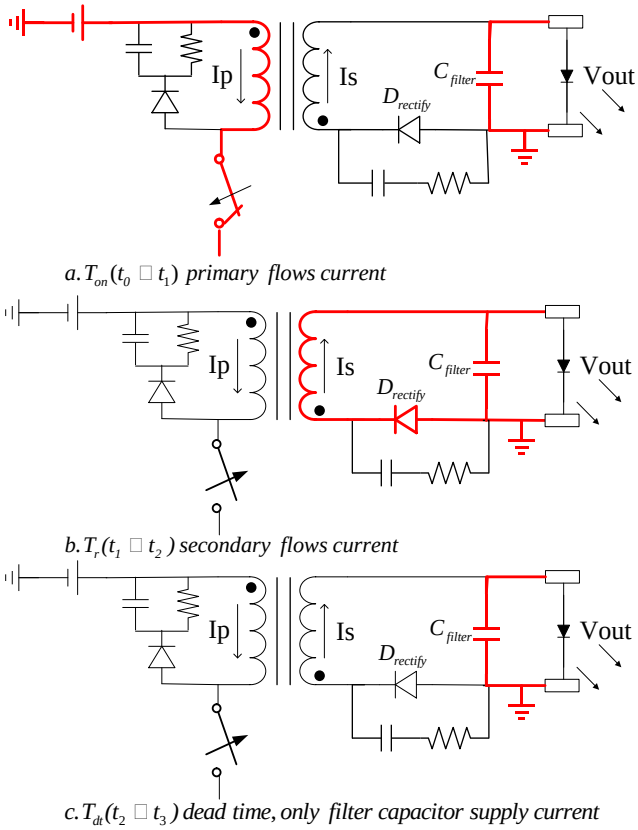


Fig. 2. Different current flowing states in fly-back converter

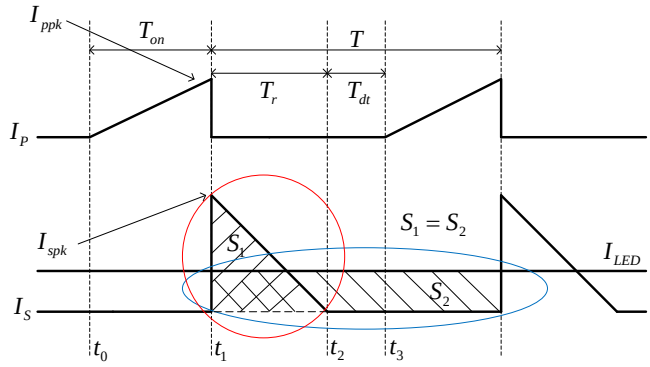


Fig. 3. Waveforms of DCM fly-back converter current

In the proposed solution, the secondary side current drops to zero before the startof the next turn on period of Switch NMOS, as depicted in Fig.2 (c). It also called discontinuous current mode (DCM) or complete energy transfer mode. The rules for an inductor withmore than one winding are as follows:The primary to secondary ampere-turns ratios is conserved.

$$N_p \times I_{ppk} = N_s \times I_{spk} \quad (1)$$

It follows that $I_{spk} = I_{ppk} \times N_p / N_s$ (2)

## III. PRINCIPLE OF CONSTANT DRIVE CURRENT

As depicted in Fig.3, the output current $I_{LED}$ is an average value for the area of $S_1$ distributed uniformity on the region of $S_2$ in an entire period T under the influence of filter capacitor $C_{filter}$ .That is,

$$\frac{1}{2} I_{spk} \times T_r = I_{LED} \times T \quad (3)$$

By combining Eq. (2), consequently, $I_{LED} = \frac{1}{2}(T_r / T) \times (N_p / N_s) I_{ppk}$ (4)

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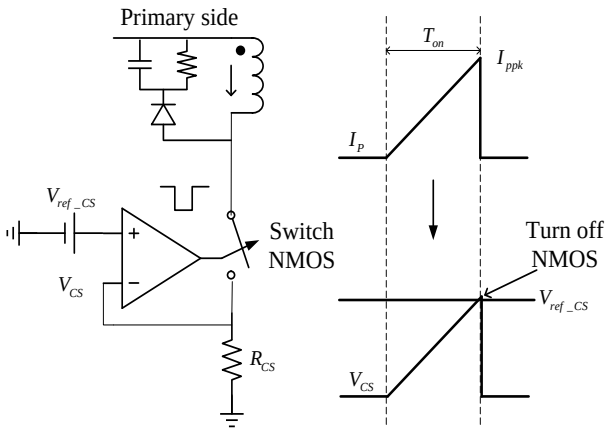


Fig. 4. Schematic of specify primary peak current

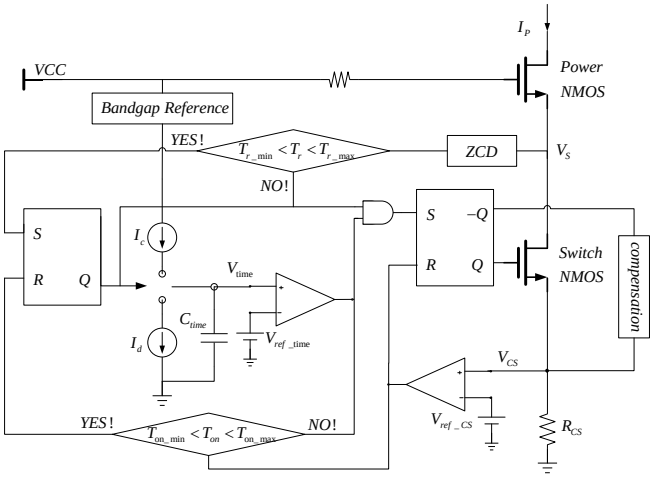


Fig. 5. Schematic of timing control

$N_p / N_s$ is depend on the physics structure of the fly-back transformer, and it can be concerned a constant value. A constant output drive current can be obtained if the $I_{ppk}$ and $T_r / T$ are also specified in the proposed solution. These can be achieved by the primary-side feedback without auxiliary winding, but using a voltage coupled network circuit to specify the ratio $T_r / T$ and a current sense circuit to set the peak primary current $I_{ppk}$ .Based on above discussion, the two decisive factors for constant output drive current is the primary peak current $I_{ppk}$ and ratio of duration of secondary side flowing current to period $T_r / T$ .

## IV. SPECIFY PRIMARY PEAK CURRENT AND THE RATIO

As discussion above, under the fly-back convert topology, the constant drive current depends the peak primary current $I_{ppk}$ and the ratio of duration of secondary side flowing current $T_r$ to the entire switching period $T$ .

### A. Specify the peak primary current

The primary peak current $I_{ppk}$ can be specified by Current Sense circuit which is depicted in the following Fig.4. When primary current $I_P$ reaches to specified peak value $I_{ppk}$ during Switch NMOS turns on $T_{on}$, current sense voltage $V_{CS}$ across sampling resistor $R_{CS}$ will rise to reference voltage $V_{ref\_CS}$ . At the same time, voltage comparator shut down Switch NMOS.That is,

$$I_{ppk} = \frac{V_{ref\_CS}}{R_{CS}} \qquad (5)$$

$$I_{spk} = \frac{N_P}{N_S} \cdot \frac{V_{ref\_CS}}{R_{CS}} \qquad (6)$$

### B. Specify the ratio of duration of secondary side flowing current to the switching period

This can be achieved by Timing Control Logic circuit, as depicted in Fig.5. Based on the work ofWeidongNieet al [10], a timing control with time checking function and cable compensation is proposed. The time checking circuit can make sure the entire system operate in a stable conduction by limiting the interval time of secondary conducting $T_{r\_min} < T_r < T_{r\_max}$ and the interval time of primary conducting $T_{on\_min} < T_{on} < T_{on\_max}$ . More details on the time

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checking will be explained in next section.After the voltage $V_{time}$ across the timing capacitor $C_{time}$ within charging state rises to the reference voltage $V_{ref\_time}$, Switch NMOS will be turned on.At the same, primary conducting current increases linearly with a slope $V_{in}/L_P$. Here $V_{in}$ is the rectified input voltage.

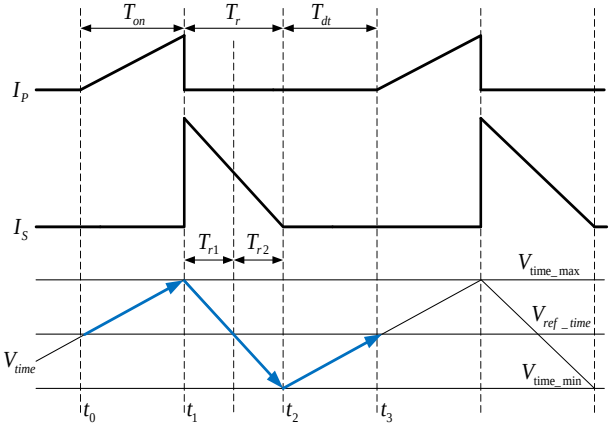


Fig. 6. Waveform of voltage across timing capacitor

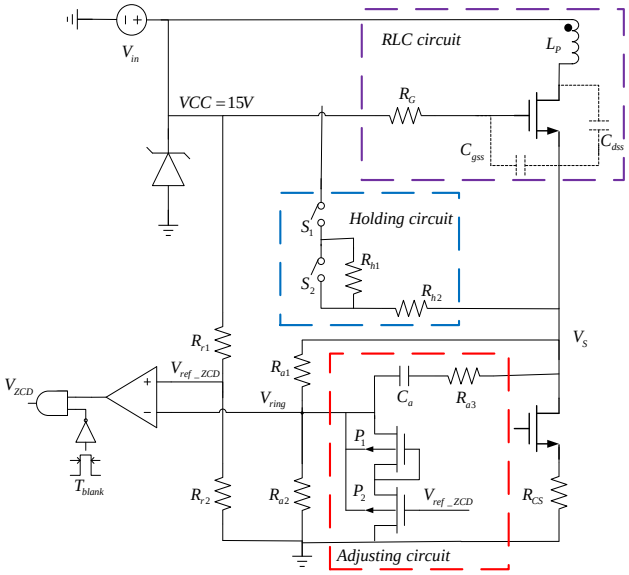


Fig. 7. Zero cross detection schematic

As illustrated above, the Current Sense circuit can specify the primary peak current $I_{ppk}$. So when current sense voltage $V_{CS}$ reaches to the setting reference point $V_{ref\_CS}$, the timing capacitor will be switched to discharging state. The termination of interval $T_r$ is depended on ZCD. At the moment when secondary current decreases to zero, the drain of Power NMOS will lost part voltage and a resonance will occur for RLC circuit consisted by primary inductance $L_P$, parasitic capacitor $C_{dss}$ and gate resistor $R_{gate}$ .Only after timing capacitor $C_{time}$ is recharged and $V_{time}$ climbs to $V_{ref\_time}$, a new cycle begin with turning on Switching NMOS.

The charging or discharging current of timing capacitor $I_c$ and $I_d$ are mirrored from a same current source for $I_c = \eta_1 I_{ref}$ and $I_d = \eta_2 I_{ref}$ .The duration of Switching NMOS turning on $T_{on}$ can be expressed as

$$T_{on} = \frac{(V_{\text{time\_max}} - V_{ref\_time}) \cdot C_{time}}{I_c} \quad (7)$$

Secondary side conducting current during $T_r$ and $T_r = T_{r1} + T_{r2}$, where

$$T_{r1} = \frac{(V_{\text{time\_max}} - V_{ref\_time}) \cdot C_{time}}{I_d} \quad (8)$$

$$T_{r2} = \frac{(V_{ref\_time} - V_{\text{time\_min}}) \cdot C_{time}}{I_d} \quad (9)$$

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From the zero cross of secondary side current to starting another new cycle, the dead time can be depicted as

$$T_{dt} = \frac{(V_{ref\_time} - V_{\text{time\_min}}) \cdot C_{time}}{I_c} \quad (10)$$

The each period is

$$T = T_{on} + T_r + T_{dt}$$
$$= (\frac{1}{\eta_1} + \frac{1}{\eta_2}) \cdot \frac{(V_{\text{time\_max}} - V_{\text{time\_min}}) \cdot C_{time}}{I_{ref}} \quad (11)$$

And the dead time can be expressed as

$$T_r = T_{r1} + T_{r2}$$
$$= \frac{1}{\eta_2} \cdot \frac{(V_{\text{time\_max}} - V_{\text{time\_min}}) \cdot C_{time}}{I_{ref}} \quad (12)$$

So the ratio of secondary side conducting duration $T_r$ to the period $T$ can be obtained

$$\frac{T_r}{T} = \frac{\eta_1}{\eta_1 + \eta_2} \quad (13)$$

In conclusion, a constant LED drive current can be achieved with a specified primary peak current $I_{ppk}$ and the ratio of $T_r$ to theperiod $T$, and be given by:

$$I_{LED} = \frac{1}{2} \cdot \frac{\eta_1}{\eta_1 + \eta_2} \cdot \frac{N_p}{N_s} \cdot \frac{V_{ref\_CS}}{R_{CS}} \quad (14)$$

## V. ADJUST RESONANCE RING SIGNAL

For detecting the time point of secondary side current reaching to zero, Zero Cross Detection (ZCD) circuit is elaborated designed. As shown in Fig.7, ZCD sensing circuit consists of a resonant RLC circuit, Holding circuit, and Adjusting circuit.

### A. RLC resonance circuit

During dead time interval $T_r$, secondary side current $I_s$ drops linearly from peak value $I_{spk}$ .The drain voltage $V_D$ of PowerNMOS is $V_{in} + (N_P / N_S) \times V_{LED}$. The primary winding inductance $L_P$, parasitic capacitors $C_{dss}$ and $C_{gss}$ of Power NMOS and gate resistor $R_G$ are combined into a RLC circuit as shown in Fig.8. After secondary current $I_s$ dropping to zero, fly-back transformer will be in high resistor state without current[11]. And the drain voltage of Power NMOSlost $(N_P / N_S) \times V_{LED}$ immediately. That is reason resonance occurringat thezero crossing point of secondary current.

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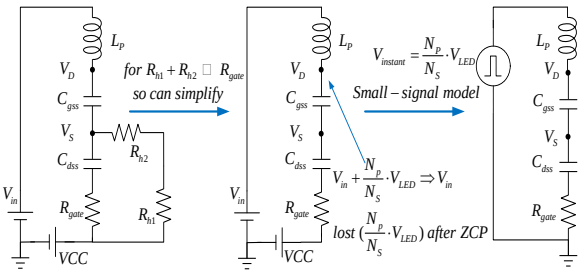


Fig. 8. Resonance caused by RLC

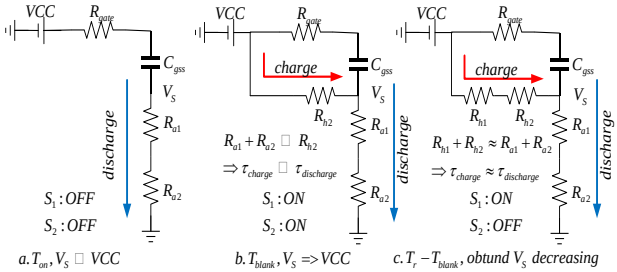


Fig. 9. Hold circuit under different states

A damped oscillation voltage at drain node of Power NMOS can be expressed as,[10]

$$\Delta V_D(t)=\frac{N_P}{N_S}\times V_{LED}\times e^{-\alpha t}\cos(2\pi f_r t) \quad (15)$$

where $\alpha=\frac{R_G}{2L_P}$, $f_r=\frac{1}{2\pi\sqrt{L_P C_d}}$, $\omega_0=\frac{1}{\sqrt{L_P C_d}}$, $C_{sum}=C_{dss}+C_{gss}$.

A useful parameter is the damping factor, $\varsigma$ which is defined as the ratio of $\alpha$ to $\omega_0$,

$$\varsigma=\frac{\alpha}{\omega_0}=\frac{R_G}{2}\sqrt{\frac{C_d}{L_P}} \quad (16)$$

The special case of ζ = 1 is called critical damping and represents the case of a circuit that is just on the border of oscillation. It is the minimum damping that can be applied without causing oscillation. Under the reason, the design should guarantee ζ>1.

So the source voltage $V_S$ experiences a voltage change $\Delta V_S(t)$ during resonant period which can be given by

$$\Delta V_S(t)=(\frac{-j}{\omega C_{dss}}//\frac{-j}{\omega C_{gss}}+R_G)\cdot(\frac{-j}{\omega C_{dss}}+R_G)\cdot\Delta V_D(t) \quad \text{Where } \omega=2\pi f_r \text{ .If } R_G=\left|\frac{-j}{\omega C_{dss}}//\frac{-j}{\omega C_{gss}}\right|,$$

$\Delta V_S(t)$ can be simplified as $\Delta V_S(t)\approx\frac{-1}{\omega^2(C_{dss}+C_{gss})C_{dss}}\cdot\Delta V_D(t)$ (17)

B. **Holding circuit**

Holding circuit which is consisted by two MOSFET switches and two resistors helps to set a proper DC voltage for $V_S$ before resonance occurring. The purpose of Hold circuit is to obtund the decrease of $V_S$ during $(T_r-T_{blank})$ after charged to $VCC$ in the blanking period. Before the secondary side current decreasing to zero, a proper voltage of $V_S$ should be set for compared with reference voltage $V_{ref\_ZCD}$ after divided. If without Hold circuit, the voltage $V_S$ decreases to an unspecified value after an undefined $(T_r-T_{blank})$. Without knowing the center voltage of $V_S$ when resonant occurs after current $I_S$ dropping to zero, the compare cannot be achieved for ambiguous and undefined reference voltage.

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The purpose of keeping a resistors network consisted by $R_{h1}$ and $R_{h2}$ is to obtund the decrease of $V_S$ during $(T_r - T_{blank})$ after increasing to $VCC$ during blanking time.

If without the resistors network consisted by $R_{h1}$ and $R_{h2}$, which can be achieved by open the $S_1$ and $S_2$ both, the decreases of $V_S$ during $(T_r - T_{blank})$ can be given by

$$\Delta V_S = VCC \cdot (1 - e^{-t/\tau}) \quad (18)$$

Where $\tau = (R_g + R_3 + R_4) \cdot C_{gss}$.

Under this circumstance, if unfortunately $V_S$ drop to $V_{ref\_ZCD}$ before zero cross of secondary side current will cause logic error.With Hold circuit performance, as depicted in Fig.9 (c), $C_{gss}$ experiences a discharger and charge both and,

$$\Delta V_S = \frac{R_{h1} + R_{h2}}{R_{a1} + R_{a2} + R_{h1} + R_{h2}} \cdot VCC \cdot (1 - e^{-t/\tau}) \quad (19)$$

Where $\tau = [R_G + (R_{h1} + R_{h2}) / /(R_{a1} + R_{a2})] \cdot C_{gss}$, and $t = T_r - T_{blank}$.

At $t = t_2$ , $V_S = VCC - \Delta V_S$. At this time, the divider voltage $V_{resonant}$ must be higher than $V_{ref\_ZCD}$ . Otherwise the ZCD sense circuit will output a signal to indicate a ZCD signal, although there is no ZCD signal in fact.

C. **Adjusting circuit**

For taking the input scope op comparator into concerned, $V_S$ should be divided into a suitable value for compared. So the resistor $R_{a1}$ usually is very larger, even larger enough to damp the resonant seriously. At the worst situation, although there is ringing happened on $V_S$ , the voltage $V_{resonant}$ cannot be detected with resonant signal and an error happened.To avoid it, the Adjusting circuit is proposed in the ZCD schematic. It is consisted by an ResonanceMagnify RC and Carriers Release PMOS, as depicted in Fig.07.

The Body of each Release PMOSs is connected to $V_{resonant}$ but not $VCC$ . After interval $T_{on}$ , the Switch NMOS is turned off. Due to the leakage inductance of transformerand the parasitic capacitance of Power NMOS, the ringing occurs.If unfortunately, the ring is larger enough to be missed consider as ZCD signal, the system will be fail for logic error.If $V_{resonant} - V_{ref\_ZCD} > V_{thP}$ during the ringing, the Release PMOS can be turn on and release the carriers for weaken the unintended ringing.During the ZCD resonant, the RC magnify circuit can deliver the ringing through its RC. A more explicit ZCD can be transformed to the comparator.

By using complex resistor concept, the whole resistors can be expressed as,

$$Z_{sum} = R_{a2} + \frac{R_{a1} \cdot \frac{1}{j\omega C_a}}{R_{a1} + \frac{1}{j\omega C_a}} = R_{eq} + jX_{eq} = |Z| e^{j\phi} \quad (20)$$

where $R_{eq} = R_{a2} + \frac{R_{a1}}{(\omega C_a R_{a1})^2 + 1}$, $X_{eq} = -\frac{\omega C_a R_{a1}^2}{(\omega C_a R_{a1})^2 + 1}$, $|Z| = \sqrt{R_{eq}^2 + X_{eq}^2}$, $\phi = \tan^{-1} \frac{X_{eq}}{R_{eq}}$.

The capacitor $C_a$ is used in the Adjust circuit for blocking direct current while allowing alternating current to pass. So

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the DC part of $V_{ring}$ can be expressed as $V_{ring\_DC} = \frac{R_{a2}}{R_{a1}+R_{a2}} \cdot V_{S\_DC}$ (21)

And AC part of $V_{ring}$ is depicted follow, $V_{ring\_AC} = \frac{R_{a2}}{Z_{all}} \cdot V_{S\_AC}$ (22)

If without the ring magnify capacitor $C_a$, $V_{ring\_AC} = \frac{R_{a2}}{R_{a1}+R_{a2}} \cdot V_{S\_AC}$ (23)

For $\left|\frac{R_{a2}}{Z_{all}}\right| > \frac{R_{a2}}{R_{a1}+R_{a2}}$, the Adjusting circuit can magnify the ring from original version.

## VI. TIME CHECKING AND COMPENSATION

### A. Time checking

For a stable and precision operation condition, the duration time $T_r$ of Secondary side flowing current should be limited in a certain scope. Unusually larger or smaller of dead time $T_r$ are both not allowed in this proposed schematic system.

Confining the minimum $T_r$ schematic is shown in Fig.10.

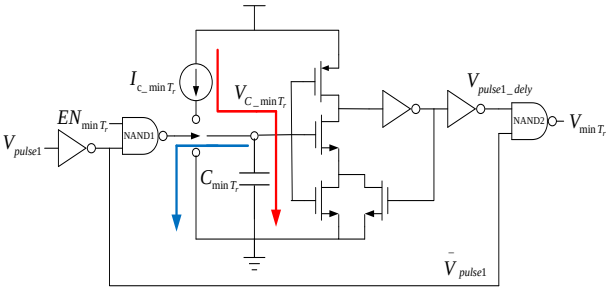


Fig. 10. Confining the minimumTr

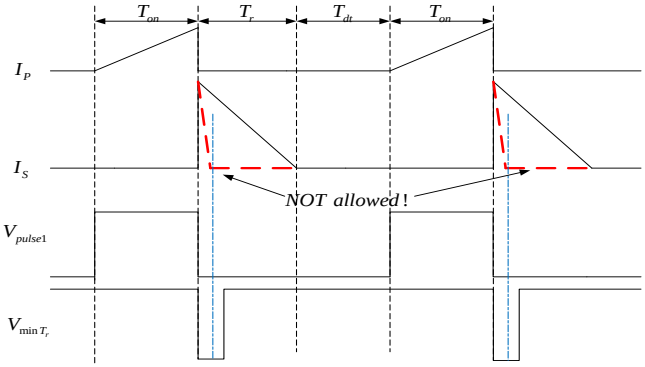


Fig. 11. Wareform of confining the minimum Tr

During in the interval $T_{on}$ primary side flowing current, the low level signal "0" voltage $\bar{V}_{pulse1}$ will closes the NAND2 outputting a high level signal "1". When Switching NMOS is shut off, the energy stored in the transformer will be transformed to secondary side while current $I_s$ linearly descend from the peak current $I_{spk}$. As depicted in Fig., $V_{pulse1}$ switch to low level signal "0" lead the voltage $V_{\min T_r}$ turning over to "0", and also through two inverses the low level signal "0" from output of NAND1 result in the capacitor $C_{\min T_r}$ connectingto the current source $I_{c\_\min T_r}$.

The current $I_{c\_\min T_r}$ charges capacitor $C_{\min T_r}$ and the voltage $V_{C\_\min T_r}$ increase linearly until reaching to the threshold voltage $V_{thN}$ of NMOSFET.

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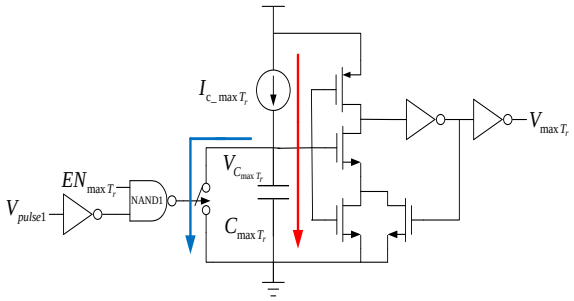


Fig. 12. Confining the maximum Tr

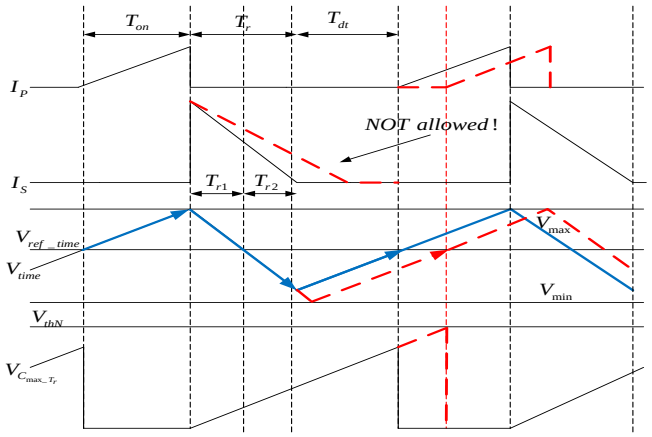


Fig. 13. Wareform of confining the maximum Tr

Only after the voltage crossing $C_{\min T_r}$ larger enough to turn on the NMOS, $V_{C\_\min T_r}$ can return to high level signal "1". So the duration time of $V_{\min T_r}$ being on "0" can be expressed as,

$$t_{\min T_r} = \frac{V_{thN}}{I_{c\_\min T_r}} \times C_{\min T_r} \quad (24)$$

Confining the maximum $T_r$ schematic is shown in Fig.12.

As discussion above, When Switching NMOS is shut off, energy stored in the transformer will be transformed to Secondary side while $I_s$ linearly descend from $I_{spk}$. As depicted in Fig.12, $V_{pulse1}$ will switch to "0" then the low level signal "0" from output of NAND1 allow current source $I_{C\_\max T_r}$ change the capacitor $C_{\max T_r}$. The voltage $V_{C_{\max T_r}}$ across $C_{\max T_r}$ increaselinearly, until beginning of a new cycle. If unfortunately, the duration time $T_r$ is so long even $V_{C_{\max T_r}}$ up to $V_{thN}$ casing a turning over on voltage signal $V_{\max T_r}$.

So the maximum duration time of $T_r$ can be expressed as,

$$t_{\max T_r} = \frac{V_{thN}}{I_{c\_\max T_r}} \times C_{\max T_r} - \frac{V_{\min}}{I_{c\_timing}} \times C_{timing} \quad (25)$$

The process of checking of Switching NMOS turning on time $T_{on}$ is similar with $T_r$. Dut to space constrains, it does't give detail in this paper.

### B. **Cable compensation**

Cable compensation has been used to compensate the voltage drop due to cable impedance. In the proposed driver design based on fly-back topology, a higher primary peak current means a larger output drive current impling greater voltage drop on cable. It uses a cable minus compensation, as depicted in Fig.14.

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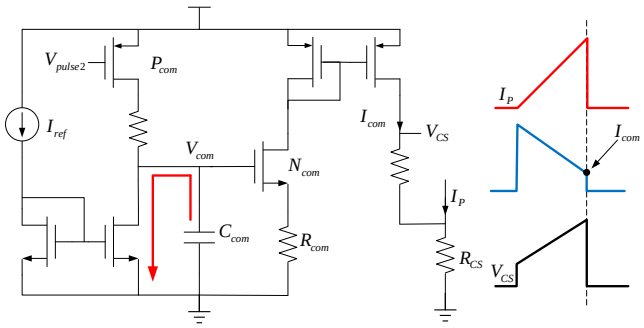


Fig. 14. Cable compensation schematic

During Switching NMOS turning on, the pulse voltage is a signal "1" shutting down the PMOS. After that, the carries storing in the capacitor will be decreased through mirrored current form reference current. Accordingly, the voltage across capacitor linearly decreases causing compensate current reducing at the same time. So a higher primary peak current will get a smaller compensatory current.

## VII. SIMULATION RESULTS AND CONCLUSION

The proposed LED driving IC is implemented in Shanghai Huahong 1um5V/40V CMOS process. It is used Cadence Spectre to simulate the schematic.

TABLE I. CIRCUIT PARAMETERS

| Symbol | Description | Value |
|---|---|---|
| $N_P / N_S$ | Number of turns | 173/51 |
| $V_{in\_AC}$ | Alternating input | 90-250V |
| $VDD$ | IC power | 5V |
| $T_{r\_\min}$ | Minimum $T_r$ | 2 $\mu s$ |
| $T_{r\_\max}$ | Maximum $T_r$ | 40 $\mu s$ |
| $I_{LED}$ | Output current | 1.5A |
| $\Delta I_{LED}$ | Output current ripple | $\pm 10mA$ |
| $T_{blank}$ | Blanking time | 500ns |
| $f$ | frequency | 60-70KHz |
| $\mu$ | efficiency | 87% |

As shown in Table1, by adjusting the number of turns in transformer and current sense resistor, a desirable output LED driving current can be realized.

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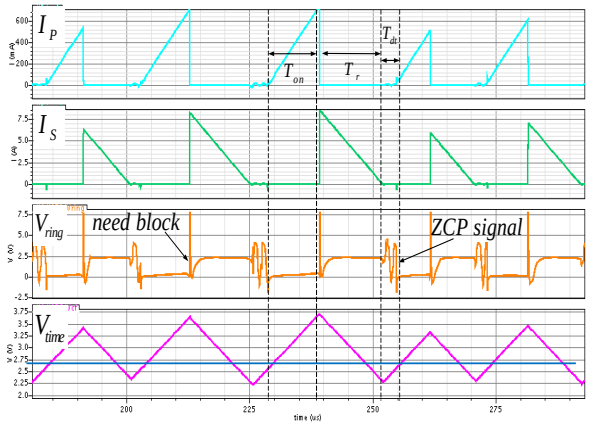


Fig. 15. A set ratio Tr/Tsimulation

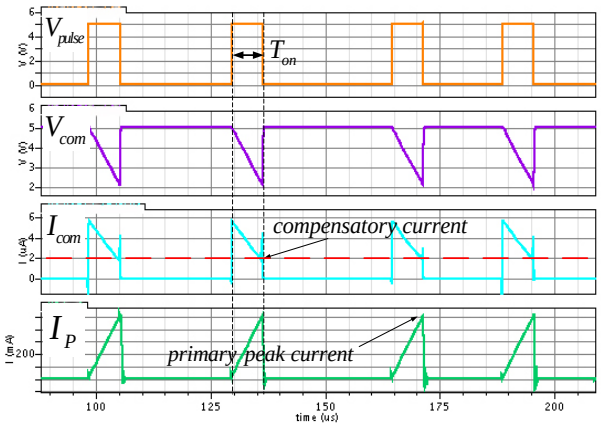


Fig. 16. Current compensation simulation

As depicted in Fig.15, due to leaking inductance, a resonance occurs during switching NMOS converting from turning on to turning off. This ring signal can be wrong regarded as zero cross point. A 500ns blanking time has been set to eliminate this influence. After secondary side current dropping down to zero, for RLC circuit, a resonance occurs. And Zero Cross Detection schematic will check this ring and timing voltage rising again. In Fig.16, the compensatory current adds to the primary peak current for decreasing cable drop influence.

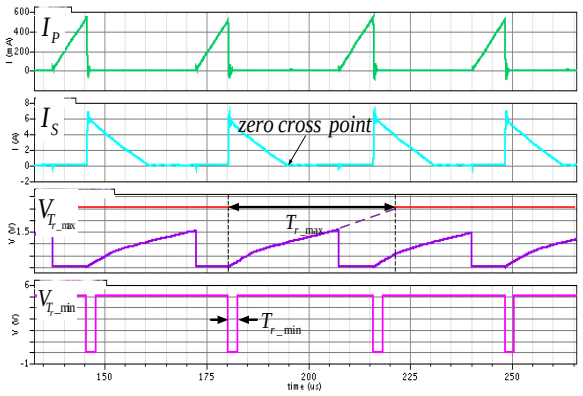


Fig. 17. Time checking simulation

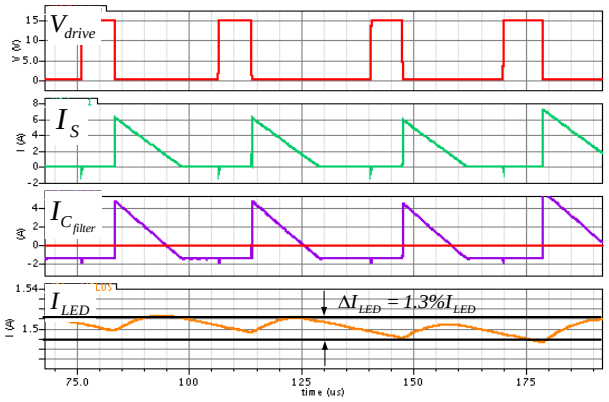


Fig. 18. Output current simulation

As depicted in Fig.17, the secondary side flowing current duration time Tr is limited between 2us and 40us for generating the system operation stability. In Fig.18, a constant LED driving current with 1.3% ripple is achieved.

The simulation result shows the proposed LED driver design based on fly-back topology without auxiliary can achieve a constant output current. ZCD can detect the point of secondary current dropping to zero and set a constant ratio or Trto period T.Time checking schematic limits the scope of Trand make the system operates in stable conduction. Besides, the cable compensation improves the precise of constant output.

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