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A New Interleaved Three Level AC–DC Converter

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ABSTRACT: A new single stage ac-dc converter with an interleaved input section is proposed in this paper to reduce line current harmonics while achieving power factor correction. The proposed converter can operate with a continuous output current for all load conditions and minimize the input electromagnetic interference filter size. In this paper, the operation of the new converter is explained, its features and design are discussed in results, and its operation is confirmed with experimental results obtained from a prototype.

KEYWORDS: Three- level converters, three-phase, power factor correction, single stage AC–DC power conversion.

I. INTRODUCTION

Power factor correction (PFC) is needed in ac–dc power supplies for them to comply with harmonic standards such as IEC 1000-3-2 [1]–[3]. Although it is possible to satisfy these standards by adding passive filter elements to the traditional passive diode rectifier/*LC* filter input combination, the resulting converter would be very bulky and heavy due to the size of the low-frequency inductors and capacitors. The most common approach to PFC is to use two-stage power conversion schemes. These two-stage schemes use a front-end ac–dc converter stage to perform ac–dc conversion with PFC with the output of the front-end converter fed to a back-end dc–dc converter stage that produces the desired isolated dc output voltage [4].

In order to reduce the cost, size, and complexity associated with two-stage ac–dc power conversion and PFC, researchers have tried to propose single-stage converters that integrate the functions of PFC and isolated dc–dc conversion in a single power converter.
Previously proposed three-phase single-stage ac–dc converters, however, have at least one of the following drawbacks that have limited their widespread use.

1) They are implemented with three separate ac–dc single-stage modules [13]–[15].
2) The converter components are exposed to very high dc bus voltages so that switches and bulk capacitors with very high voltage ratings are required [17], [18], [22], [23].
3) The input currents are distorted and contain a significant amount of low-frequency harmonics because the converter has difficulty performing PFC and dc–dc conversion simultaneously [16].
4) The converter must be controlled using very sophisticated techniques and/or nonstandard techniques [5]–[11]. This is particularly true for resonant-type converters that need variable-switching-frequency control methods to operate.
5) The output inductance must be very low, which makes the output current to be discontinuous. This results in a very high output ripple so that secondary diodes with high peak current ratings and large output capacitors to filter the ripple are needed [13]–[20].
6) Most of them are in discontinuous conduction mode at the input and need to have a large input filter to filter out large high-frequency harmonics [4], [13]–[15], [17], [18], [22]–[24].

The authors proposed a three-phase single-stage three-level converter to mitigate these drawbacks in [24]. Although the converter proposed in that paper was an advance over previously proposed three-phase single-stage converters, it still suffered from the need to have a discontinuous output inductor current at light-load conditions to keep the dc bus

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capacitor voltage < 450 V, and it needed to operate with discontinuous input current, which resulted in high component current stress and the need for significant input filtering due to the large amount of ripple.[25-27]
This paper presents a new interleaved three-phase single-stage rectifier that does not have any of these drawbacks. The work presented in this paper can be considered to be a follow-up work in relation to what was presented in [28]. In comparison to the converter presented in [24], the converter presented in this paper has an interleaved structure, requires two fewer diodes in the dc bus, has an output current which is continuous for all load ranges, has a dc bus voltage that is less than 450 V for all load conditions, and has a much better input current harmonic content. In this paper, the operation of the new converter is explained, its features and design are discussed in results, and its operation is confirmed with experimental results obtained from a prototype.[29-30]

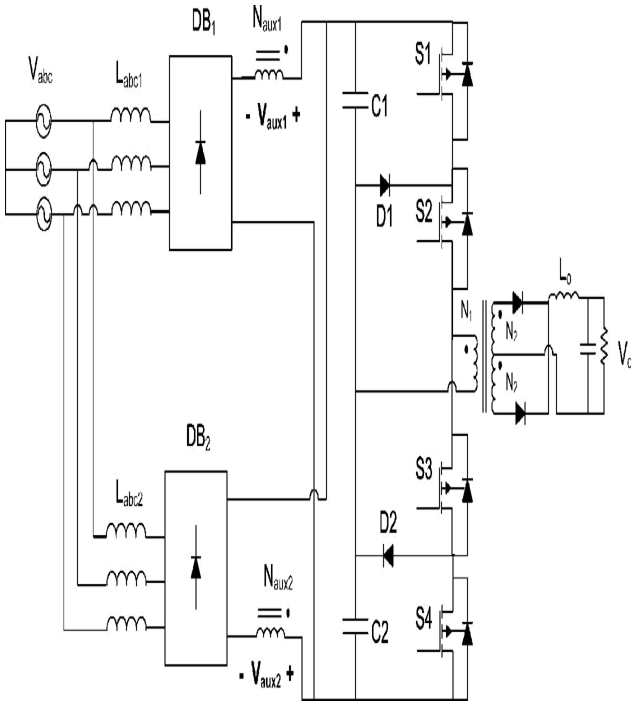

Fig. 1. Proposed interleaved three-level converter from a prototype.

II. CONVERTER OPERATION

The proposed converter and its key waveforms are shown in Figs. 1 and 2, respectively. The proposed converter uses auxiliary windings that are taken from the converter transformer to act as "magnetic switches" to cancel the dc bus capacitor voltage so that the voltage that appears across the diode bridge output is zero. When the primary voltage of the main transformer is positive, auxiliary winding 1 ($N_{aux1}/N_1 = 2$) cancels out the dc bus voltage so that the output voltage of diode bridge 1 (DB_1) is zero and the currents in input inductors L_{a1}, L_{b1}, and L_{c1} rise. When the primary voltage of the main transformer is negative, auxiliary winding 2 ($N_{aux2}/N_1 = 2$) cancels out the dc bus voltage so that the output voltage of diode bridge 2 (DB_2) is zero and the currents in input inductors L_{a2}, L_{b2}, and L_{c2} rise. When there is no voltage across the main transformer primary winding, the total voltage across the dc bus capacitors appears at the output of the diode bridges and the input currents fall since this voltage is greater than the input voltage. If the input currents are discontinuous, the envelope of the input current will be sinusoidal and in phase with the input voltages.

The converter modes of operation are explained in this section. The typical converter waveforms are shown in Fig. 2. The equivalent circuit in each stage is shown in Fig. 3. The converter goes through the following modes of operation.

Mode 1 ($t_0 < t < t_1$) [Fig. 3(a)]: During this interval, switches S_1 and S_2 are ON. In this mode, the energy from dc bus capacitor C_1 flows to the output load. Due to magnetic coupling, a voltage appears across auxiliary winding 1 which is

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equal to the dc bus voltage but has opposite polarity and cancels the total dc bus capacitor voltage; the voltage at the diode bridge output is zero, and the input currents in L_{a1}, L_{b1}, and L_{c1} rise.

Mode 2 ($t_1 < t < t_2$) [Fig. 3(b)]: In this mode, S_1 is OFF, and S_2 remains ON. The energy stored in L_1($L_1 = L_{abc1}$) during the previous mode starts to transfer into the dc bus capacitors. The voltage that appears across auxiliary winding 1 is zero. The primary current of the main transformer circulates through D_1 and S_2.

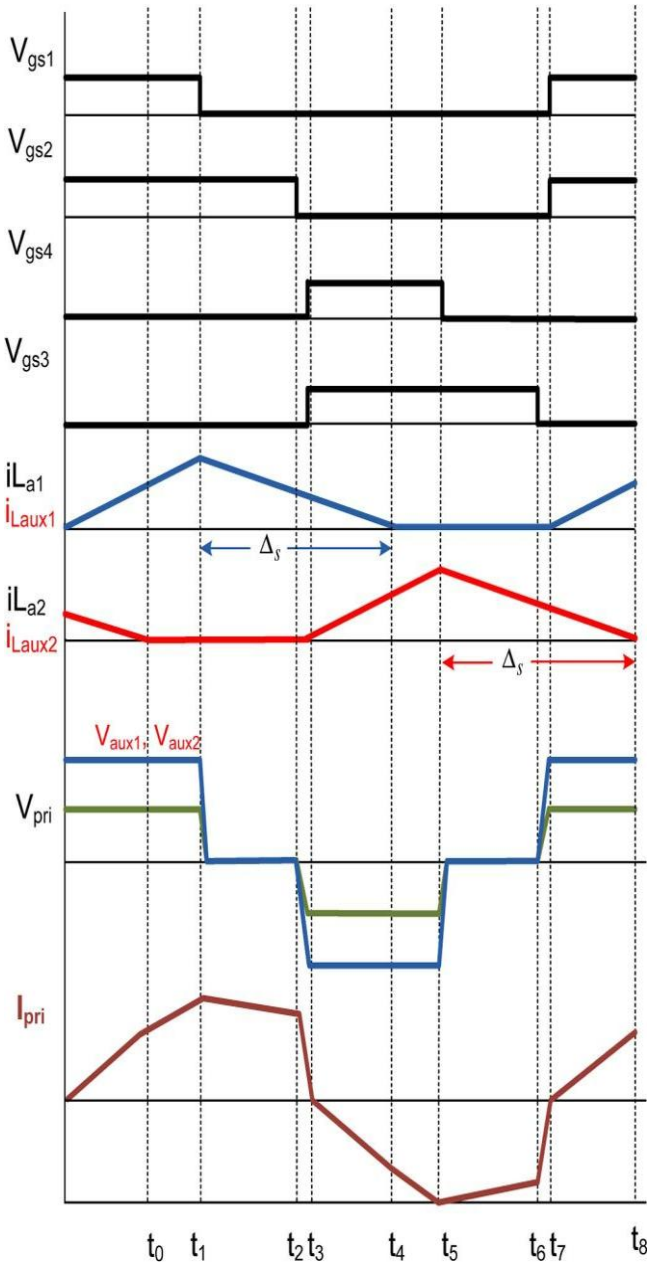

Fig. 2. Typical waveforms describing the modes of operation.

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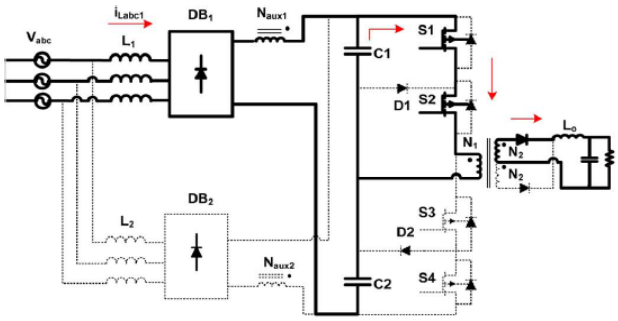
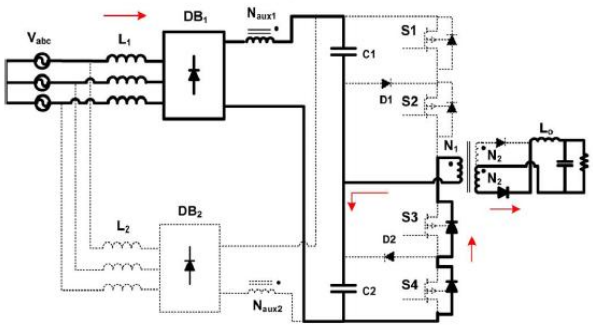


(a)



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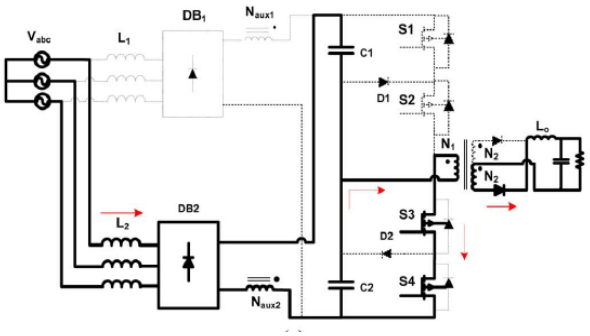

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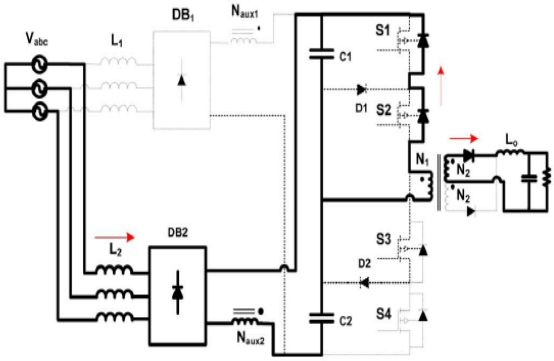
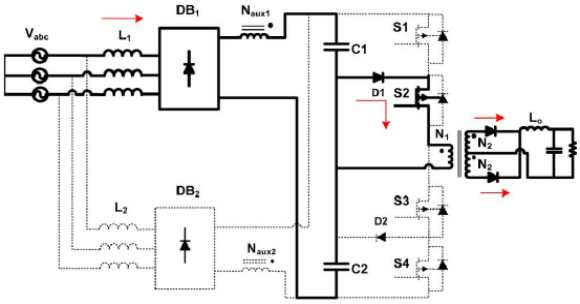


(g)



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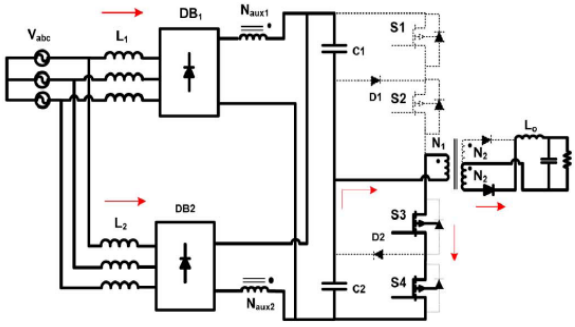

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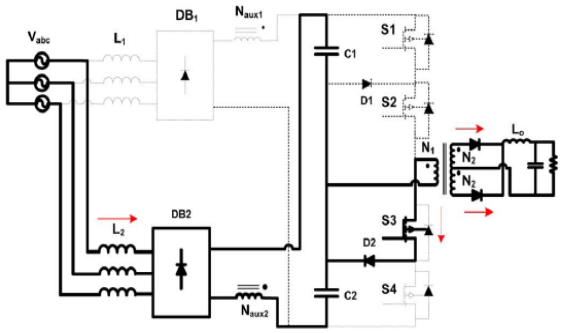
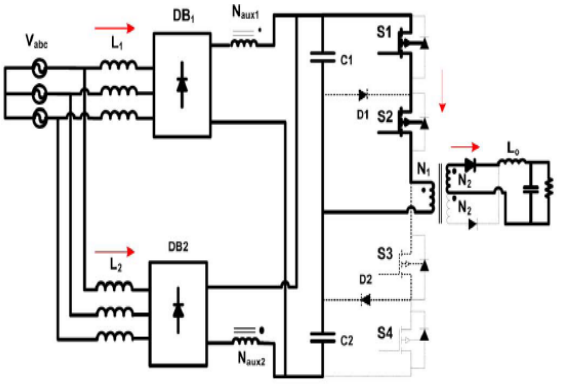


(f)



(h)

Fig. 3. Modes of operation. (a) Mode 1 ($t_0 < t < t_1$). (b) Mode 2 ($t_1 < t < t_2$). (c) Mode 3 ($t_2 < t < t_3$). (d) Mode 4 ($t_3 < t < t_4$). (e) Mode 5 ($t_4 < t < t_5$). (f) Mode 6 ($t_5 < t < t_6$). (g) Mode 7 ($t_6 < t < t_7$). (h) Mode 8 ($t_7 < t < t_8$).

With respect to the converter's output section, the load inductor current freewheels in the secondary of the transformer, which defines a voltage across the load filter inductor equal to $-V_L$.

Mode 3 ($t_2 < t < t_3$) [Fig. 3(c)]: In this mode, S_1 and S_2 are OFF. The energy stored in L_1 still is transferring into the dc bus capacitor. The primary current of the transformer charges C_2 through the body diodes of S_3 and S_4. Switches S_3 and S_4 are switched ON at the end of this mode.

Mode 4 ($t_3 < t < t_4$) [Fig. 3(d)]: In this mode, S_3 and S_4 are ON, and the energy flows from capacitor C_2 into the load. The voltage appears across auxiliary winding 2 which is equal to the dc bus voltage but acts like a magnetic switch and cancels out the dc bus voltage.

The voltage across the boost inductors $L2$ ($L2 = L\text{abc}2$) becomes only the rectified supply voltage of each phase, and the current flowing through each inductor increases. This mode ends when the energy stored in $L1$ completely transfers into the dc bus capacitor. For the remainder of the switching cycle, the converter goes through modes 1–4 but with $S3$ and $S4$ ON instead of $S1$ and $S2$ and with DB2 instead of DB1.

Mode 5 ($t_4 < t < t_5$) [Fig. 3(e)]: In this mode, S_3 and S_4 are ON, and a symmetrical period begins. In this mode, the energy flows from capacitor C_2 into the load. The voltage across the boost inductors L_2 becomes only the rectified supply voltage of each phase, and the current flowing through each inductor increases.

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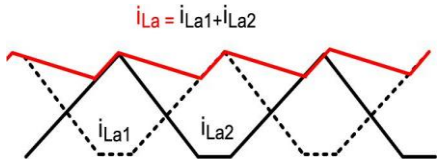

Fig. 4. Interleaving between two input inductor currents.

Mode 6 ($t_5 < t < t_6$) [Fig. 3(f)]: In this mode, S_3 is ON and S_4 is OFF, and the primary current of the main transformer circulates through diode D_2 and S_3. The energy stored in the boost inductors L_2 during the previous mode starts transferring into the dc bus capacitor. The output inductor current also freewheels in the secondary of the transformer during this mode.

Mode 7 ($t_6 < t < t_7$) [Fig. 3(g)]: In this mode, S_3 and S_4 are OFF, and the primary current of the transformer charges capacitor C_1 through the body diodes of S_1 and S_2. The energy stored in the boost inductors L_2 transfers into the dc bus capacitor.

Mode 8 ($t_7 < t < t_8$) [Fig. 3(h)]: In this mode, S_1 and S_2 are ON. In this mode, the energy from dc bus capacitor C_1 flows to the output load. This mode ends when the energy in the inductors L_2 completely transfers into the dc bus capacitors. Time t_8 is the end of the switching cycle, and another switching cycle begins with the same modes.

It should be noted that the input current is the summation of inductor currents i_{L1} and i_{L2} which are both discontinuous. However, by selecting appropriate values for L_1 (= L_{a1} = L_{b1} = L_{c1}) and L_2 (= L_{a2} = L_{b2} = L_{c2}) in such a way that two inductor currents such as i_{La1} and i_{La2} have to overlap each other, the input current can be made continuous as shown in Fig. 4, thus reducing the size of the input filter significantly. There is a natural 180° phase difference between the currents in L_1 and the currents in L_2 as one set of currents rises when the transformer primary is impressed with a positive voltage and the other set rises when the transformer primary is impressed with a negative voltage—these two events occur 180° apart during a switching cycle.

III. CONVERTER ANALYSIS AND DESIGN

A procedure for the design of the converter is presented in this section and is demonstrated with an example. The following criteria should be considered when trying to design the converter:

1. The energy-storage capacitor voltage Vbus should not be excessive. The value of Vbus should be kept to below 800 V if possible so that the use of bulkier, more expensive capacitors can be avoided.
2. Excessive peak output and input currents should be avoided.
3. The input line current must satisfy the necessary regulatory agency requirements of harmonic content such as IEC1000-3-2 Class A.

A design procedure for the selection of converter components based on the characteristic curves presented in the previous sections of this paper is given along with an example to illustrate how the converter can be designed. The converter is to be designed with the following parameters for the example:

Input voltage: Vin = 208 10% V*l-l*, rms
Output voltage: Vo = 48 V
Maximum output power: Po = 1100 W
Switching frequency: fsw = 1/Tsw = 100 kHz
Maximum capacitor voltage: (for each capacitor) 450 V
Input current harmonics: EN61000-3-2 for Class A electrical equipment.

Step1: Determine Value for Turns Ratio of Main Transformer N

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N is an important parameter as it affects the amount of reflected load current that is available at the transformer primary to discharge the bus capacitors.
If N is very low, then there is little reflected load current available to discharge the bus capacitors, which can result in an extremely high DC bus voltage. If N is high, then the primary current may be very high as there will be a high amount of current circulating in the transformer primary, which will create significant conduction losses. A trade-off between high values of N and low values of N, therefore, must be considered when selecting a value of N.

Selecting a value of N, however, cannot be done with a simple equation and must be done using some other method. One way of doing so is to use the computer program described in [25] to examine a wide range of potentially valid combinations of L_o and L_{in} – combinations that allow the converter to work for the two most extreme line and load conditions: high line, light load and low line, full load. For this particular design, a value of N = 2.5 is selected as an appropriate value.

As a check to see if this value makes sense, equation (1) -which shows the relation between V_{bus}, D, V_o and N – can be used.

$$V_o = \frac{V_{bus}}{2N} D \qquad (1)$$

For this check, the operation of the converter at minimum input line when it operates with minimum primary-side dc bus voltage $V_{bus,min}$ and maximum duty cycle D_{max} should be considered. If the converter can produce the required output voltage and can operate with discontinuous input and continuous output currents in this case, then it can do so for all cases. Substituting $V_{bus,min}$ and maximum duty cycle D_{max} into equation (1) gives

$$V_{bus,min} = \frac{2V_o}{D_{max}} . N \qquad (2)$$

Substituting V_o = 48, N = 2.5, and D_{max} = 0.8 (0.8 has been selected as a conservative D_{max} to provide some margin) gives

$$V_{bus,min} = \frac{2(48)}{0.8} . (2.5) = 300V \qquad (3)$$

A bus voltage of $V_{bus,min}$ = 300 V or $V_{bus}/2$ = 150 V is acceptable. If a very low value of $V_{bus,min}$ = 100 V or a value of D_{max} > 1 would have been found based on equation (2), then the value of N under consideration would have been unacceptable and another value would have to be considered. It should be noted that the dc bus voltage has not been determined yet. All that has been determined thus far is a value of N that can operate with an acceptable duty cycle for an acceptable minimum dc bus voltage.

Step2: Determine Value for Output Inductor Lo

For having CCM at output, the minimum value of L_o should be the value of L_o with which the converter's output current will be continuous on the when the converter is operating with maximum input voltage, minimum duty cycle (D_{min}), and minimum Load (10% of $P_{o,max}$). If this condition is met, then the output current will be continuous for all other converter's operating conditions. The minimum value of L_o can therefore be determined to be

$$L_{o,min} \geq \frac{V_o^2}{0.1.P_{o,max}} . \frac{(1-D_{min})}{2} . \frac{T_{sw}}{2} \qquad (4)$$

This results in a low ripple at output and low peak current rating for secondary diodes and consequently lower output capacitor needs to filter the ripple. Substituting V_o = 48, $P_{o,max}$ =1100W, D_{min} = 0.1 and f_{sw}=100Khz, therefore the value of L_o should be larger than 47 µH. In this case L_o=100 µH is chosen to have less ripple at output and decrease the output capacitance filter.

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Step 3: Determine Value for Input Inductor Lin

The value for L_1 and L_2 should be low enough to ensure that their currents are fully discontinuous under all operating conditions, but not so low as to result in excessively high peak currents. This can be done using the computer program with the following equations, which are based on the descriptions given in [25]. For the case where $L_1 = L_2 = L$ are such that the i_{L1} and i_{L2} remain discontinuous for all operating conditions, then the average input power can be expressed as;

$$P_{in} = \frac{3}{\pi}*\left(\frac{1}{T_{su}}\int_0^{T_{su}} |v_{s,k}|\, i_{s,k}\, d_{w_k} t\right) = \frac{3}{\pi}\cdot\frac{1}{f_{sn}}\sum_{k=0}^{f_{sn}-1} |v_{s,k}| i_{s,k} \tag{5}$$

where f_{su} is the input ac frequency and $f_{su} = \frac{2f_{sw}}{f_{su}}$ and

$$i_{s,k} = \frac{(D+\Delta_s)}{2} i_{L_{in},max} = \frac{1}{4}\cdot\frac{D^2}{L_{in}\cdot f_{sw}}\cdot\frac{|v_{s,k}|}{1-\frac{|v_{s,k}|}{V_{bus}}} \tag{6}$$

By substituting the value of $i_{s,k}$ (21), P_{in} can be expressed as:

$$P_{in} = \frac{3}{\frac{\pi}{2}}\cdot\frac{1}{f_{sn}}\sum_{k=0}^{f_{sn}-1}|v_{s,k}| i_{s,k} \tag{7}$$

$$= \frac{3.D^2}{8.\frac{\pi}{2}.L_{in}.f_{sw}}\cdot\frac{1}{f_{sn}}\sum_{k=0}^{f_{sn}-1}\frac{|v_{s,k}|^2}{1-\frac{|v_{s,k}|}{V_{bus}}}$$

By assuming the $P_{in} = P_o$, L_{in} can be achieved:

$$L_{in} = \frac{1}{f_{sn}}\sum_{k=0}^{f_{sn}-1}|v_{s,k}| i_{s,k} \tag{8}$$

$$L_{in} = \frac{D^2}{4.\pi.P_o.f_{sw}}\cdot\frac{1}{f_{sn}}\sum_{k=0}^{f_{sn}-1}\frac{|v_{s,k}|^2}{1-\frac{|v_{s,k}|}{V_{bus}}} \tag{9}$$

IV. EXPERIMENTAL RESULTS

An experimental prototype of the proposed converter was built to confirm its feasibility. The prototype was designed according to the following specifications:

Input voltage V_{in} = 208 ± 10% V_{rms} (line−line)

Output voltage V_o = 48 V

Output power P_o = 1.1 kW

Switching frequency f_{sw} = 100 kHz.

The typical converter waveforms are shown in Fig. 5. It can be seen that the proposed converter can operate with nearly sinusoidal input currents. It is a multilevel full-bridge converter that the switch stresses are half the dc bus voltage; it also can operate with a continuous output current, unlike most other converters of the same type.

The converter in [24] is a single-stage three-level PFC converter and is a non interleaved version of the proposed converter with just one set of input inductors instead of two. The output inductor current in [24] was designed to be continuous for heavy loads and discontinuous for light loads to keep the dc bus voltage less than 450 V.

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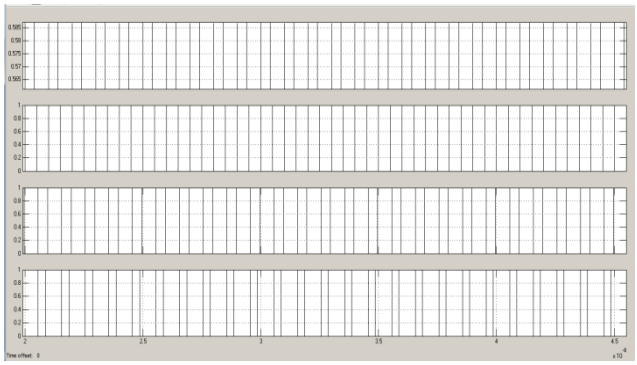
Compared to the non interleaved converter that was presented in [24], the interleaved converter that is proposed in this paper has several advantages in addition to reduced input current ripple. The proposed converter can operate with a continuous current at the output from 10% of the full load to full load, which makes the output current have less ripple. This is because the proposed converter has an interleaved structure that results in a change of the energy equilibrium at the dc bus (the net equivalent inductance at the input is larger in the proposed converter), which makes the dc bus small enough to permit the output inductor to be sufficiently large.

A larger output inductor means that there is considerably less ripple in the output inductor current of the interleaved converter than there is in the non interleaved converter proposed in [24]. This helps reduce secondary component stresses and filtering. It should be noted that the converter has been implemented with an output inductor that is larger than necessary to show that the proposed converter can operate with a continuous output current and a primary-side dc bus voltage that is not excessive.
It should also be noted that no additional input filtering was used for the proposed interleaved converter, and the input current waveform is just the summation of an input phase current of diode bridge 1 and the corresponding phase current of diode bridge 2.

It should be noted that the proposed converter has a higher efficiency than the converter proposed in [24]. This is because it does not have any diode in the dc link, whereas the converter proposed in [24] must have. It is also due to the fact that the switch voltage turn-on losses have been reduced considerably as there is much less voltage across the switch; it is because the proposed converter has much less dc bus voltage in comparison to that in [24].



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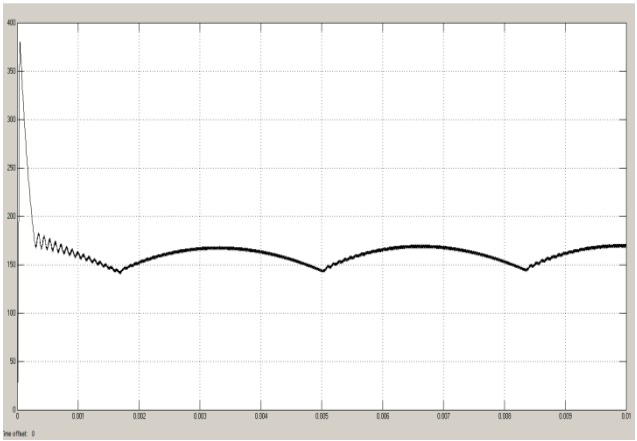

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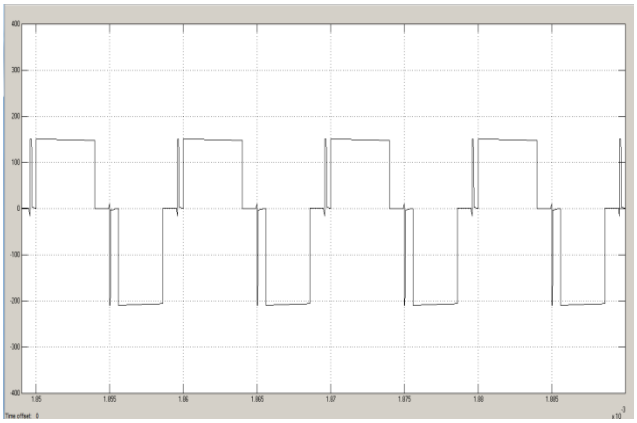

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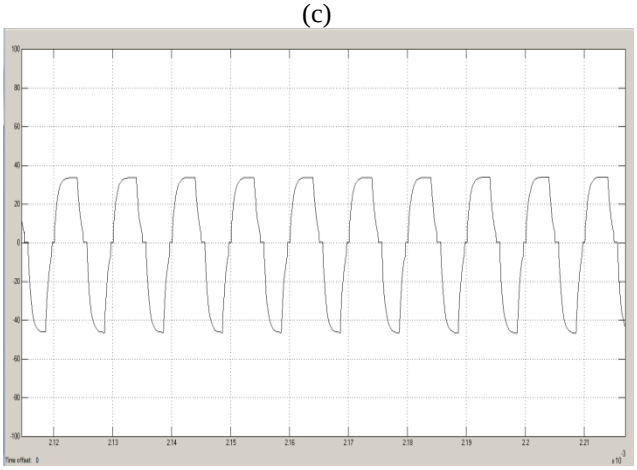

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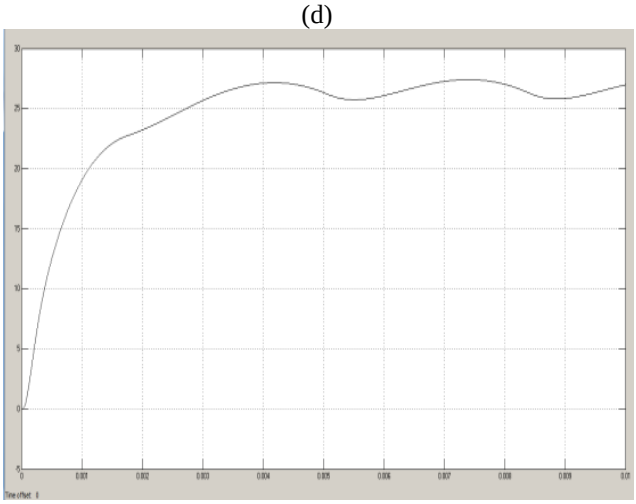

(e)

Fig. 5. EXPERIMENTAL RESULTS. (a) Pulse. (b) Input Voltage. (c) Three Level Output Voltage. (d) Transformer AC Supply. (e) Output Voltage.

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V. CONCLUSION

A new interleaved three-level ac–dc converter using single-stage power-factor correction was presented in this paper. The proposed converter uses auxiliary windings taken from its power transformer as magnetic switches to cancel the dc bus voltage so that the input section operates like a boost converter. The proposed converter has the following features.

1) The proposed converter can operate with lower peak voltage stresses across its switches and the dc bus capacitors as it is a three-level converter. This allows for greater flexibility in the design of the converter and ultimately improved performance.
2) The proposed converter has a much better input current harmonic content that meets the EN61000-3-2 Class A standard with reduced input filter due to the interleaved structure.
3) The larger output inductor of the proposed converter can be designed to work in continuous conduction mode over a wide range of load variation and input voltage. This results in a lower output inductor current ripple than the non interleaved converters which helps reduce secondary component stresses and filtering.
4) The proposed interleaved converter operates with greater efficiency than the converter proposed in [24] because it has fewer diodes in the dc bus and it has less switch voltage turn-on losses.

REFERENCES

[1] *Limits for Harmonic Current Emission (Equipment Input Current >16 A per Phase)*, IEC1000-3-2 Int. Std., 1995.
[2]Sathyanarayana H.P., Premkumar S., Manjula W.S., "Assessment of maximum voluntary bite force in adults with normal occlusion and different types of malocclusions", Journal of Contemporary Dental Practice, ISSN : 1526-3711, 13(4) (2012) pp.534-538.
[3]Selva Kumar S., Ram Krishna Rao M., Deepak Kumar R., Panwar S., Prasad C.S., "Biocontrol by plant growth promoting rhizobacteria against black scurf and stem canker disease of potato caused by Rhizoctonia solani", Archives of Phytopathology and Plant Protection, ISSN : 0323-5408, 46(4) (2013) pp.487-502.
[4] *Limits for Harmonic Current Emission (Equipment Input Current >16 A per Phase)*, IEC1000-3-4 Int. Std., 1998.
[5]*IEEE Recommended Practices and Requirements for Harmonic Control in Electric Power Systems*, IEEE Std. 519-1992, Apr. 1993.
[6]Mahalakshmi K., Prabhakar J., Sukumaran V.G., "Antibacterial activity of Triphala, GTP & Curcumin on Enterococci faecalis", Biomedicine, ISSN : 0970 2067, 26(Mar-4) (2012) pp. 43-46.
[7]Bhuvaneswari B., Hari R., Vasuki R., Suguna, "Antioxidant and antihepatotoxic activities of ethanolic extract of Solanum torvum", Asian Journal of Pharmaceutical and Clinical Research, ISSN : 0974-2441, 5(S3) (2012) pp. 147-150.
[8] B. Tamyurek and D. A. Torrey, "A three-phase unity power factor singlestage AC–DC converter based on an interleaved flyback topology," *IEEE Trans. Power Electron.*, vol. 26, no. 1, pp. 308–318, Jan. 2011.
[9]J. M. Kwon, W. Y. Choi, and B. H. Kwon, "Single-stage quasi-resonant flyback converter for a cost-effective PDP sustain power module," *IEEE Trans. Ind. Electron.*, vol. 58, no. 6, pp. 2372–2377, Jun. 2011.
[10]Hariharan V.S., Nandlal B., Srilatha K.T., "Efficacy of various root canal irrigants on removal of smear layer in the primary root canals after hand instrumentation: A scanning electron microscopy study", Journal of Indian Society of Pedodontics and Preventive Dentistry, ISSN : 0970-4388, 28(4) (2010) pp.271-277.
[11] H. L. Cheng, Y. C. Hsieh, and C. S. Lin, "A novel ingle-stage high-powerfactor AC/DC converter featuring high circuit efficiency," *IEEE Trans. Ind. Electron.*, vol. 58, no. 2, pp. 524–532, Feb. 2011.
[12]S. K. Ki and D. D.-C. Lu, "Implementation of an efficient transformer-less single-stage single-switch AC/DC converter," *IEEE Trans. Ind. Electron.*, vol. 57, no. 12, pp. 4095–4105, Dec. 2010.
[13] H. Ma, Y. Ji, and Y. Xu, "Design and analysis of single-stage power factor correction converter with a feedback winding," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1460–1470, Jun. 2010.
[14] H. J. Chiu, Y. K. Lo, H. C. Lee, S. J. Cheng, Y. C. Yan, C. Y. Lin, T. H. Wang, and S. C. Mou, "A single-stage soft-switching flyback converter for power-factor-correction applications," *IEEE Trans. Ind. Electron.*, vol. 57, no. 6, pp. 2187–2190, Jun. 2010.
[15] J. Zhang, D. D.-C. Lu, and T. Sun, "Flyback- based single-stage power factor correction scheme with time-multiplexing control," *IEEE Trans. Ind. Electron.*, vol. 57, no. 3, pp. 1041–1049, Mar. 2010.
[16] H. S. Ribeiro and B. V. Borges, "New optimized full-bridge single-stage AC/DC converters," *IEEE Trans. Ind. Electron.*, vol. 58, no. 6, pp. 2397–2409, Jun. 2011.
[17] P. Barbosa, F. Canales, J.-C. Crebier, and F. C. Lee, "Interleaved three phase boost rectifiers operated in the discontinuous conduction mode: Analysis, design considerations and experimentation," *IEEE Trans. Power Electron.*, vol. 16, no. 5, pp. 724–734, Sep. 2001.
[18] H. M. Suraywanshi, M. R. Ramteke, K. L. Thakre, and V. B. Borghate, "Unity-power-factor operation of three phase AC–DC soft switched converterbased on boost active clamp topology in modular approach," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 229–236, Jan. 2008.
[19] U. Kamnarn and V. Chunkag, "Analysis and design of a modular three phase AC-to-DC converter using CUK rectifier module with nearly unity power factor and fast dynamic response," *IEEE Trans. Power Electron.*, vol. 24, no. 8, pp. 2000–2012, Aug. 2009.
[20] U. Kamnarn and V. Chunkag, "A power balance control technique for operating a three-phase AC to DC converter using single-phase CUK rectifier modules," in *Proc. IEEE Conf. Ind. Electron. Appl.*, 2006, pp. 1–6.
[21] J. Contreas and I. Barbi, "A three-phase high power factor PWM ZVS power supply with a single power stage," in *Proc. IEEE PESC*, 1994, pp. 356–362.
[22] F. Cannales, P. Barbosa, C. Aguilar, and F. C. Lee, "A quasi-integrated AC/DC three-phase dual-bridge converter," in *Proc. IEEE PESC*, 2001, pp. 1893–1898.

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[23] F. S. Hamdad and A. K. S. Bhat, "A novel soft-switching high-frequency transformer isolated three-phase AC-to-DC converter with low harmonic distortion," *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 35–45, Jan. 2004.
[24] C. M. Wang, "A novel single-stage high-power-factor electronic ballast with symmetrical half-bridge topology," *IEEE Trans. Ind. Electron.*, vol. 55, no. 2, pp. 969–972, Feb. 2008.
[25] D. Wang, H. Ben, and T. Meng, "A novel three-phase power factor correction converter based on active clamp technique," in *Conf. Rec. ICEMS*, 2008, pp. 1896–1901.
[26] A. M. Cross and A. J. Forsyth, "A high-power-factor, three-phase isolated AC–DC converter using high-frequency current injection," *IEEE Trans. Power Electron.*, vol. 18, no. 4, pp. 1012–1019, Jul. 2003.
[27] P. M. Barbosa, J. M. Burdio, and F. C. Lee, "A three-level converter and its application to power factor correction," *IEEE Trans. Power Electron.*, vol. 20, no. 6, pp. 1319–1327, Nov. 2005.
[28] Y. Xie, Y. Fang, and H. Li, "Zero-voltage-switching three-level three-phase high-power-factor rectifier," in *Proc. IEEE IECON*, 2007, pp. 1962–1967.
[29] M. Narimani and G. Moschopoulos, "A novel single-stage multilevel type full-bridge converter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 1, pp. 31– 42, Jan. 2013.
[30] S.P. Vijayaragavan, B. Karthik, T.V.U. Kiran Kumar and M. Sundar Raj, Analysis of Chaotic DC-DC Converter Using Wavelet Transform, Middle-East Journal of Scientific Research 16 (12): 1813-1819, 2013, ISSN 1990-9233.
[31] Thooyamani, K.P., Khanaa, V., Udayakumar, R., "Wireless cellular communication using 100 nanometers spintronics device based VLSI", Middle - East Journal of Scientific Research, v-20, i-12, pp:2037-2041, 2014.
[32] Vanangamudi, S., Prabhakar, S., Thamotharan, C., Anbazhagan, R., "Dual fuel hybrid bike", Middle - East Journal of Scientific Research, v-20, i-12, pp:1819-1822, 2014.
[33] Udayakumar, R., Kaliyamurthie, K.P., Khanaa, Thooyamani, K.P., "Data mining a boon: Predictive system for university topper women in academia", World Applied Sciences Journal, v-29, i-14, pp:86-90, 2014.
[34] Satheesh, S., Lingeswaran, K., "High efficiencytransformer less inverter for single-phase photovoltaic systems using switching converter", Middle - East Journal of Scientific Research, v-20, i-8, pp:956-965, 2014.
[35] Vijayaragavan, S.P., Karthik, B., Kiran Kumar, T.V.U., "A DFIG based wind generation system with unbalanced stator and grid condition", Middle - East Journal of Scientific Research, v-20, i-8, pp:913-917, 2014.