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Algorithm-Based Output Phase Optimization for PLA's

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ABSTRACT: In the paper an application of evolutionary algorithm to design and optimization of PLA-based two-level realization of circuits using a good choice of output phases of the sub functions. This approach based on the logic synthesis and optimization. Two-level realization produces the more advantages over multilevel realization due to their minimum delay configurations. This algorithm-based approach for selection of output phases to optimize the PLA for area and power. Optimization results are superior over the ESPRESSO results. This logic is one of the most effective circuit configurations for implementing high speed logic designs. A new power cost model of state encoding is proposed here to reduce the consumption of power. It has been shown that the different range of solutions over the ESPRESSO. In this optimization results are more superior to the previous results.

KEYWORDS- PLA, logic optimization, area minimization, power minimization, genetic algorithm.

I. INTRODUCTION

Programmable logic array (PLA) is a structure that provides regular structure for implementing combinational and sequential logic functions. It has been used to control the logic in cmos is constructed in two main ways, with two level sum of product logic and with multi-level logic. It realizes logic functions in Two-level form. Two-level realization enjoys advantages over multilevel ones due to their minimum delay configurations. Traditionally, the major optimization goal for PLAs has been area reduction and power minimization.

The area of a PLA can be reduced if the number of product terms forming the AND plane can be minimized. For a multi-output function, greater the sharing of product terms between sub functions, greater will be the saving in the AND-plane.

Traditional Two-level minimizers like ESPRESSO [4] attempt to increase the sharing between the Traditional Two-level minimizers like ESPRESSO [4] attempt to increase the sharing between the sub functions. Another avenue through which AND-plane reduction can be achieved is by selecting the output phases of the sub functions. Consider the following example of a 3-variable input, 2-variable output function consisting of the following sub functions. Another avenue through which AND-plane reduction can be achieved is by selecting the output phases of the sub functions. Consider the following example of a 3-variable input, 2-variable output function consisting of the following sub functions:

$$f_1 = x + yz,$$
$$f_2 = y + z.$$

If both f1 and f2 are implemented in their true form, four product lines corresponding to x, yz, y', z' are needed. However, if f2 is implemented in the complemented form, the function becomes,
$f_1 = x + yz$, $f_2' = yz$, which needs only two products terms x, yz.

Power minimization is a important aspect that has come up in recent years in circuit realization. This is true particularly because todays electronic circuits consist of more than hundreds of thousands of devices on the silicon

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floor area, thus increasing the power requirement. The devices are mostly portable, hand-held and plastic packaged. Thus it is essential to reduce the power consumption so that less dissipation in the form of heat takes place, thereby increasing battery life also. The output phase assignment may affect the expected switching activity (ESA), and thus control the power requirement of the AND-plane. For example, consider the function, f and x + yz. Assuming the ON probability of all primary inputs to be *0.5*, ESA for x is *0.5* and that of yz is *0.375*. Thus the total ESA in AND plane is equal to *0.875*.However, taking *f* in the complemented phase, f=x'y'+x'z', the ESA for AND plane is found to be 0.75. Thus from power reduction point of view, f should be realized in the complemented phase. This paper explores the idea of output phase assignment to get area and power optimized PLAs. It first uses a genetic algorithm (GA)-based approach to obtain the area-optimized PLAs using output phase assignment. It gives on an average 3–9% improvement over the existing works reported in the literature. Then the formulation has been extended to power minimization, which results in about 14–23% improvement over existing approaches.

II. LITERATURE SURVEY

Basically this method based on the logic optimization and naive approach. This to solve the output phase assignment problem is to generate all 2^mpossibleassignments form output functions, obtain a minimized PLA for each assignment and retain the one with minimum number of product terms. This is prohibitively expensive considering the cost of 2^m calls for a two-level logic minimizer, e.g., ESPRESSO [4]. To avoid such expensive computation many heuristic approaches have been proposed. The earliest approach was proposed by Sasao [1], which is used in Espresso under the option–*Dopo*. According to this approach, given a function F with *m* outputs, an auxiliary functions FF with 2^m outputs is constructed that is called a double-phase characteristic function. The first m scalar components of FF are the same as those of F. The second *m* scalars are their complements. The double-phase characteristic function is then minimized using a heuristic or exact minimizer. Then the minimized cover FFmin is examined in the search for the minimum set of product terms that cover each scalar component, either in the complemented or uncomplemented form.

Sasao's heuristic algorithm is based on the following observations:

1. The outputs (columns) of double-phase characteristic function with fewer ones may be less expensive to implement than the outputs with more ones. This is because a single 1 in a column represents a product term needed to implement the corresponding outputs.
2. If most of the product terms needed to implement an output can be used to implement the other outputs, then this output is potentially useful to reduce the overall cost.

A graph-based approach to find a near-optimal assignment for PLA minimization. This approach exploits the necessary and sufficient conditions to reduce the number of product terms needed for PLA implementation and permits the use of existing graph algorithms to solve the PLA output phase optimization problem. The work is based on the transformation of a PLA into a graph whose vertices are a set of conditions required to reduce each product term of the PLA and whose edges represent the relation between these conditions. The cliques in the graph correspond to the output phase assignment required to reduce the product terms represented by the vertices in the cliques. The optimal PLA output phase assignment problem is then formulated as a well-studied problem in graph theory: finding maximum cliques in the graphs.

In their analysis, in order to find a relationship between the switching activity and circuit structure, they have assumed that the output of each logic gate to be equally weighted. This is of course true for any regular VLSI structures like PLA. Although they have given a reduced power estimation technique, especially the ESA reduction for two as well as for multilevel, power minimization is achieved at the cost of increased literal count and number of product terms as compared to ESPRESSO. In this paper, we propose a genetic algorithm approach, which provides us with highly optimal solution to the PLA area minimization problem and we use the same approach for best-phase assignment targeting optimum expected switching activity for a PLA, which in turn optimizes power. We have also presented a trade-off analysis between the number of product terms and switching activities, thus trading off between the area and power requirements of a PLA.

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III. POWER DISSIPATION CALCULATION

In CMOS logic circuits total power dissipation [6] is given by

$P = 0.5CV\ 2dd\ f\ N + QscVdd\ f\ N + IleakageVdd,$

Where, Vdd is the supply voltage, f, the frequency of operation, C, the node capacitance, N,the switching activity, that is the number of gate output transitions per clock cycle. If the short-circuit power and leakage power dissipation (which are a small fraction of the total power dissipation) are neglected, then total power dissipation in CMOS logic circuits

TABLE I

AREA MINIMIZATION RESULTS

Method	Circuit	I/o/p	Product term	Phase assignment
ESRESSO	5xpl	7/10/74	65	l 0101010111
	aralis	10/41/74	100110111101000 00110010111100	
	decode	13/16/64	010000000101111 11	
	Average improvement over GA 11.57%			
ESPRESSO-DOPO	5xpl	7/10/74	59	l 0101010111
	aralis	10/41/74	55	100110111101000 00110010111100
	decode	13/16/64	18	010000000101111 11
	Average improvement over GA 2.24%			
GA	5xpl	7/10/74	58	l 0101010111
	aralis	10/41/74	28	100110111101000 00110010111100
	decode	13/16/64	22	010000000101111 11

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can be considered to be mainly due to dynamic or switching power. In a well-designed CMOS circuits, dynamic power accounts for more than 90% of the total power dissipation. Since for a particular technology, Vdd and *f* are fixed, C for two-level PLA circuit is also fixed. N,the switching activity factor, accounts for total power dissipation. In the above model, we have not considered the leakage power and short-circuit power to avoid complexity in their modelling. All the other methods mentioned in this article also use the same model.

ESA is defined as the expected number of changes that occur at the outputs of the gates of a Combinational logic circuit. For a change in the primary input to the system we assume that primary inputs are uncorrelated, that is, Prob(input = 1) = Prob(input = 0) = 1/2, and are statistically independent of each other. The expected switching activity at the output of a logic gate, *F*, is denoted by the term ESA (*F*).We first begin by considering the ESA for a single logic gate. Output of the logic gate changes its state if the current state of the output differs from the previous one. Thus the probability of the output of a gate changing state is: Prob(current output = 0) × Prob(previous output = 1) + Prob(current output = 1) × Prob(previous output = 0). Since we assume that the probability does not change with time, ESA (of logic gate) = 2 × Prob(output = 0) × Prob(output = 1).The ESA for an *i* input AND gate or an OR gate (with primary inputs) is 2 $(1/2^i)$ $[1 – (1 –2^i)]$. Expected switching activity of the PLA circuit is equal to the sum of all ESAs of all AND gates (Implicants) and of all OR gates (Outputs).

ESA = $\sum all\ gates 2(1/2i)[1 – (1/2i)]$,

where *i* is a variable which represents the number of inputs to the AND or an OR gate. We will be using this ESA expression as the measure of power consumed by the PLA.

IV. GA FORMULATION

Genetic Algorithms (GAS) are stochastic, non-derivative optimization method. They use popula-tions of acceptable solutions (genes) of the given problem, which evolve toward optimum. The genes in standard GAS are Boolean vectors. We now describe a GA-based approach to solve the output phase assignment problem. Genetic algorithms [7, 8] are stochastic optimization search algorithms based on the mechanics of natural selection and natural genetics. The genetic formulation of any problem involves the careful and efficient choice of (i) a proper encoding of the solutions to form chromosomes, (ii) a cross-over operator, (iii) mutation operator, and (iv) a cost function measuring the fitness of the chromosomes in a population. The chromosome corresponding to a solution is a binary string of size *m*, where *m* is the number of outputs for the PLA. The i^{th} element of the binary string represents phase of the i^{th} output function. A '0' in this bit string represents the function to be realized in the complemented form, while a '1' corresponds to an uncomplemented realization.

Two genetic operators' crossover and mutation have been used to evolve new generations. The crossover operator creates two new chromosomes by crossing over two parent chromosomes about randomly selected crossover points. The number of crossover points and their positions has been selected randomly. In our GA formulation, the selection of chromosomes participating in crossover is not uniformly random. In fact, it is biased towards the chromosomes with better fitness value. For this purpose the whole population is sorted according to the fitness value. A certain percentage of population with better fitness value is considered to be the "best class".

To select a chromosome participating in crossover, first a uniform random number between 0 and 1 is generated. If the number is greater than 0.5, a chromosome from the best class is selected randomly. Otherwise a chromosome is selected from the entire population. Let the population size be *n* and the cardinality of best class be *m*. Then the probability of a chromosome getting selected for crossover is $0.5/m + 0.5/n$ for chromosomes belonging to the best class, whereas for those not belonging to the best class, it is $0.5/n$. Since *m* is much lesser than *n*, the probability of a chromosome belonging to best class being selected is more than that of a chromosome not belonging to the best class. This approach of selecting more fit chromosomes to participate in crossover leads to the generation of better off springs as compared to truly random one.[1] After generating each pair of chromosomes, a check is made with the already generated chromosomes and duplicates are eliminated.

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The mutation operator simply modifies a chromosome by complementing the Boolean value at some of the randomly chosen points in the binary string. Again a check is made for duplicate. We have considered three separate fitness functions to achieve the different objectives of the GA formulation. These are, namely, area fitness measure, power fitness measure and combined area and power fitness measure[2].

For a given chromosome, the fitness measure for area minimization is the number of product terms required to realize the function with the sub functions assigned phases as depicted by the chromosome. The goal is to reduce the number of product terms required to realize the function.[3] To get the complemented version of a sub function within a multi-output function, the single output function is first extracted and then passed on to ESPRESSO with '-OR' option,

TABLE II

POWER MINIMIZATION RESULTS

Method	Circuit	I/o/p	ESA	Phase assignment
ESRESSO	5xpl	7/10/74	8.69	l 0101010111
	aralis	10/41/74	1.85	1001101111010000011001011 1100
	decode	13/16/64	11.26	01000000010111111
	Average improvement over GA 3.19%			
ESPRESSO-DOPO	5xpl	7/10/74	7.79	l 0101010111
	aralis	10/41/74	2.23	1001101111010000011001011 1100
	decode	13/16/64	4.95	01000000010111111
	Average improvement over GA 1.08%			
GA	5xpl	7/10/74	7.79	l 0101010111
	aralis	10/41/74	1.85	1001101111010000011001011 1100
	decode	13/16/64	3.21	01000000010111111

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Which produces the complement of the function as output. A new multi-output function is constructed by altering the phases of required sub function using the procedure outlined above[4]. This newly constructed function is then fed to ESPRESSO to get the minimized two-level form. The number of product terms in this minimized function is the number of product terms needed to realize the multi-output function, with phases of the sub functions indicated by the chromosome. This value is thus taken as the fitness value of the chromosome[5].

Population size is selected depending upon the number of output functions. We have used population size of 50 for outputs less than or equal to 20, and 200 for outputs greater than 20. Chromosomes are generated randomly as initial population and are sorted in ascending order of the fitness measure, as the more fit a chromosome is the lower its value is. Considering the case of 200 chromosomes, first 40 chromosomes are taken to be the *best class* chromosomes[6]. We copy the best class solutions directly to the next generation. We generate 120 chromosomes by crossover and 40 chromosomes by mutation as the population for the next generation keeping the population size fixed at 200. This process is repeated till there is no improvement in fitness function even after certain predefined number of generations, which is fixed at 50 in our experimentations[7].

V. EXPERIMENTAL RESULTS

Table I summarizes the area minimization results for 3 PLAs. The column I/O/P indicates the number of inputs, outputs, and product terms as present in the original circuit. The column Espresso notes the product terms obtained after running the tool ESPRESSOon it[8]. The column Espresso-Dopo notes the results of running ESPRESSO with "-D opo" option. This minimizes the circuit using heuristic output phase assignment as suggested by Sasao[9]. The column GA corresponds to the area optimization results obtained via genetic algorithm approach presented in this paper. The GA-based approach
required on an average 11.57% lesser product terms than that required by Espresso and 2.24% lesser product terms than that required by the Espresso-Dopo approach.[10]

Table II summarizes the power minimization results. Columns 3, 4, and 5 represent the expected switching activity obtained by the application of the three different types of approaches, performing on the same machine. In this case, the GA-based approach requires, on an average, 3.19% less switching activity than the Espresso-generated circuit.[12] With respect to Espresso-Dopo option, GA requires on an average 1.08% lesser switching. Thus, the GA-based approach works much superior to it.[13]

VI.CONCLUSION

Output phase assignment plays an important role in efficient realization of PLA. In this paper, we have shown that a genetic algorithm-based formulation can handle the problem very well, both from the point of view of area and power minimization. A weighted minimization scheme has established the trade-off between area and power that can be achieved, in realizing two.level circuits using PLA. In this particular work, while taking the power estimation model, we have not considered the leakage power and short-circuit power, to simplify the model. However, as we are now in the era of submicron VLSI technology, the effect of leakage and short-circuit current cannot be neglected and so these are to be included in the present model, which can be taken as the future work.

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