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An Efficient Implementation of Fir Filter on FPGA Using Micro Programmed Controller

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ABSTRACT:- Digital finite impulse response (FIR) filters play a very important role in digital signal processing (DSP) applications ranging from image and video processing to wireless communication. Digital FIR filter is primarily composed of multipliers, adders and delay elements. Several techniques have been reported in the open literature to implement digital FIR filters using Field Programmable Gate Array (FPGA). This paper also presents an FPGA implementation of FIR filter but using a novel micro programmed controller based design approach. The proposed controller controls the sequence of operation of the filter. To demonstrate the technique, design of a sequential 16-tap digital FIR filter based on the micro programmed controller is presented. The proposed FIR filter is coded in VHDL using modular design approach and implemented in Spartan-3E FPGA. Performance evaluation is done based on the implementation results obtained through Xilinx ISE tool

I. INTRODUCTION

In Signal processing applications such as cancellation of echo, noise equalization and biomedical applications, etc., digital filters are the most frequently used element [8-9]. Finite Impulse Response filter is the type of digital filter and it gives good stability and linear phase properties. The impact of word length also less in FIR filters. The essential elements used to design digital FIR filters are adders, multipliers, delay elements. The basic building block of the FIR filter will be designed by arranging the components in a different ways [1]. Equation 1 shows the operation of linear digital FIR filter.

$$y(n) = \sum_{k=0}^{N-1} h(k).x(-k)$$

Where, x(n-k) will be the delayed filter input and y(n) will be the filter output, h(k) will be the impulse -response. The above equation shows the convolution of the impulse response and the delayed filter input. *K=0,1,…N-1* will be the filter coefficients. The tapped delay line FIR filter can be realized as shown in fig. 1.It is also known as transversal filter or direct form filter. The N tap FIR filter has N delays, N adders and N+1 multipliers.

The Non recursive filter using Field Programmable Gate Array (FPGA) has been implemented by using several techniques [2-4]. The Existing system uses 4 tap FIR filter and micro programmed control instructions set for to control the filter. The objective of this paper is to establish a micro programmed controller [5-7] based design by using an example of sequential 8 tap FIR filter. In the proposed work we are implementing a pipelining techniques in FIR filter for to achieve high speed and compare the parameters such as area, speed and throughput by employing various adders. The FIR filter based on Pipelining technique achieves high speed and throughput than the conventional architecture [10].

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The paper is organized as follows. The design of the data path and the micro programmed controller architecture of the proposed 8 tap FIR filter are discoursed in section II and III respectively. In section IV the discussion about results. Eventually in section V conclusion and future work are presented.

II. DATA PATH ARCHITECTURE FOR NON RECURSIVE FILTER

The two main building blocks in data path architecture of proposed non recursive filters is data path unit and control unit [11]. The architecture of 8 tap non recursive filter with the data path and control unit as shown in fig..2. Fig..3. depicts the data path design of 8 tap FIR filter.

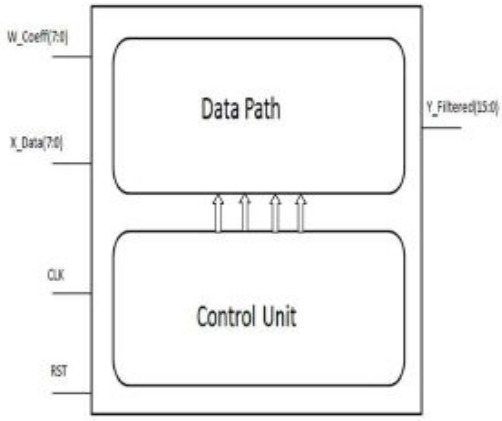

Fig.1. Block Diagram of FIR filter

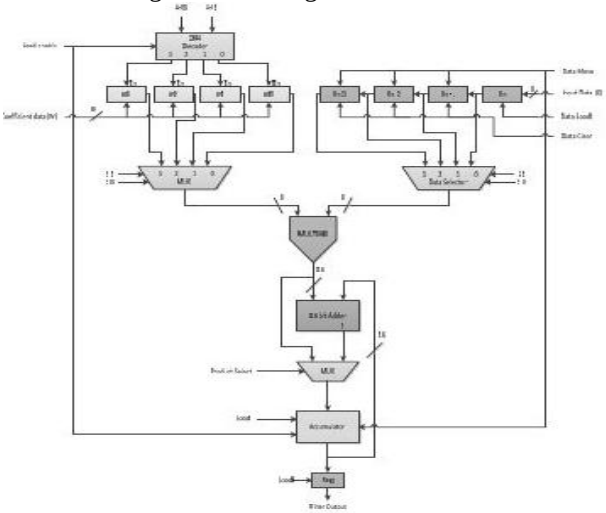

Fig.2.Data path architecture

The sub modules present in the data path design has 2:4 decoder for to decode the data, data selectors as two 4 to 1 multiplexer, four 8 bit coefficient registers for to store the weight, 16 bit adder, multiplier and to control the data flow one 2 to 1 multiplexer will be used,16 bit register to store the output [12]. The language used here is VHDL for to code each sub modules and integrated finally to obtain complete data path.

III. MICRO PROGRAMMED CONTROLLER FOR NON RECURSIVE FILTER

The Hardwired based controller and the micro programmed based controller are the different methods for designing the controller . The micro programmed controller will be used here for to control the flow of the FIR filter. It

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uses ROM based control memory to add or change the data by merely altering the micro program instructions is the main advantage of the micro programmed controller [13]. It consists of two important module addressing micro instructions and the second is holding and compute micro instructions.

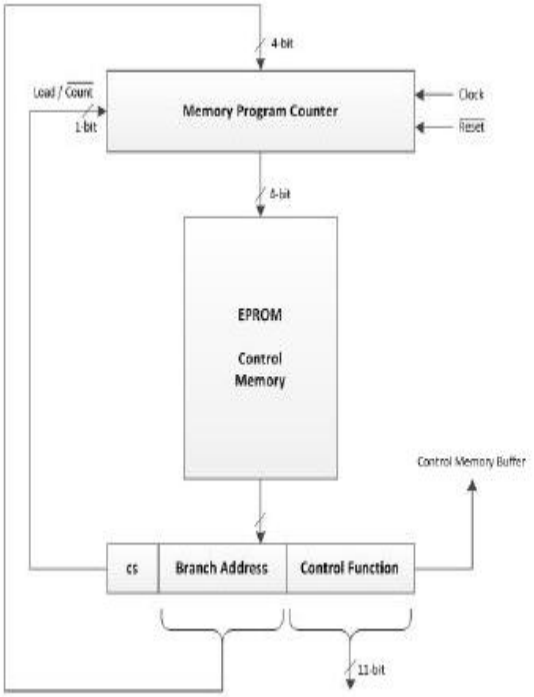

Fig.3. Micro programmed Controller

No.	Operations	Cs	Branch Address				LE	Ld1	Ld0	Dc	Di	S_1	S_0	Ps	Iacc	Dm	Y_L
1	Load w_0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
2	Load w_1	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0
3	Load w_2	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0
4	Load w_3 and Clear Accumulator	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0
5	Load Data x[n]	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
6	Acc <= w_0 * x[n]	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
7	Acc <= Acc + w_1 * x[n-1]	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0
8	Acc <= Acc + w_2 * x[n-2]	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0
9	Acc <= Acc + w_3 * x[n-3]	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0
10	Moving Input Data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
11	Latch output y[n]	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
12	Go to # 5	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0

Table.1.Control Signals

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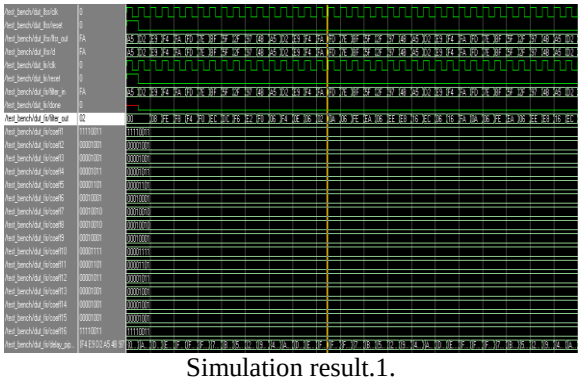
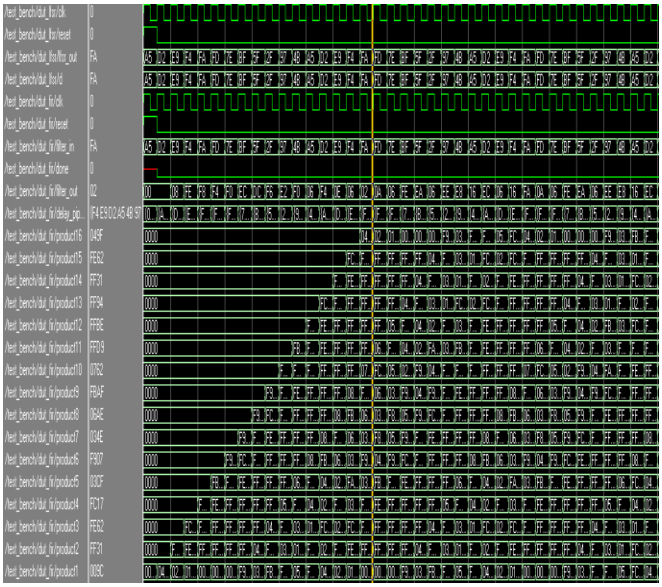
The following signals are used in micro programmed controller control signals, load enable signals (LE), decoder output signals (LD1 & LD0), select signal (s1 & s0), product select (ps) and load accumulator signal (lacc). After asserting the latch signal (Y_l), we obtain the filtered output data and when the data move(D_m) signal is high the process will be continued for the remaining registers [14].

IV. RESULTS AND DISCUSSION



Simulation result.1.



Simulation result.2.

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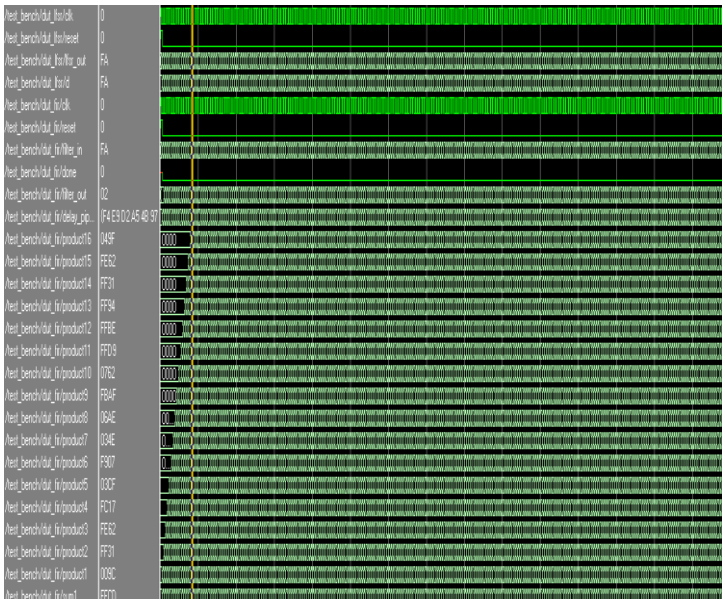

Simulation result.3.

V.CONCLUSION AND FUTURE WORK

In this paper we have presented a design of 16 tap FIR filter using micro programmed controller and its FPGA implementation. The micro programmed controller is used for controlling the operation of digital FIR filter. A sequential architecture utilizing single multiplier and adder along with other building blocks are used to demonstrate the proposed technique. Performance evaluation is done by synthesizing and implementing the design in target Spartan-3E FPGA using Xilinx ISE XST synthesis tool.

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