



A Multilevel Cascaded Inverter for Unbalanced DC Source using Carrier Based Neutral Voltage Modulation Strategy

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ABSTRACT: This paper proposes a pulse width-modulation strategy to achieve balanced line-to-line output voltages and to maximize the modulation index in the linear modulation range where the output voltage can be linearly adjusted in the multilevel cascaded inverter (MLCI) operating under unbalanced dc-link conditions. In these conditions, the linear modulation range is reduced, and a significant output voltage imbalance may occur as voltage references increase. In order to analyze these effects, the voltage vector space for MLCI is evaluated in detail. From this analysis, the theory behind the output voltage imbalance is explained, and the maximum linear modulation range considering an unbalanced dc-link condition is evaluated. After that, a neutral voltage modulation strategy is proposed to achieve output voltage balancing as well as to extend the linear modulation range up to the maximum reachable point in theory. In the proposed method, too large of a dc-link imbalance precludes the balancing of the output voltages. This limitation is also discussed. Both the simulations and the experiments for a seven-level phase-shifted modulated MLCI for electric vehicle traction motor drive show that the proposed method is able to balance line-to-line output voltages as well as to maximize the linear modulation range under the unbalanced dc-link conditions.

KEYWORDS: Multilevel Cascaded Inverter (MLCI), Space Vector Pulse Width Modulation SVPWM, Neutral Voltage Modulation (NVM)

I. INTRODUCTION

MLCIs are used for many applications, such as dynamic voltage restorer, static synchronous compensator (STATCOM), high-voltage energy storage device, photovoltaic inverters, medium-voltage drives, electric vehicle (EV) traction drives, and so on. In MLCI applications, a modulation strategy to generate gating signals is very crucial to achieve high-performance control. To reduce the common-mode voltage, a multilevel SVPWM has been designed. The series SVPWM method has been reported to easily implement SVPWM for the MLCI. An SVPWM is for hybrid inverters consisting of neutral point clamp and H-bridge inverters to improve output voltage quality and efficiency. As with two-level inverters, it is also possible to implement carrier-based SVPWMs which are equivalent to traditional SVPWMs by injecting a common offset voltage to the three-phase references. Some methods to calculate the offset voltages to achieve the optimal space vector switching sequence are addressed. The performances of a carrier-based PWM and an SVPWM are compared, and a PWM scheme is proposed to obtain an optimal output voltage in the multilevel inverter. On the other hand, MLCIs require separated dc links. Therefore, if there is one or more faults present in the dc links in each phase, or if the voltage magnitudes of the dc links are unequal, the output voltage of the MLCI can be unbalanced without proper compensation. Reference explains why the optimum angles and modulation indexes are necessary to obtain maximum balanced load voltages in the MLCI undergoing a fault on switching modules. A neutral voltage shifting technique has been introduced for balancing the state of charge in the MLCI-based battery energy storage system. A duty cycle modification method has been proposed to compensate an output voltage imbalance caused by single-phase power fluctuations. Reference has shown that a zero sequence component helps to obtain the maximum balanced output voltages in a fault condition. An offset voltage injection technique is studied to balance the output voltage of the MLCI, but the use of an integrator in the compensation method may reduce dynamic characteristics in applications such as EV motor drives. Recently, the multilevel multiphase feed forward space vector modulation technique called MFFSVM is to compensate the voltage imbalances in MLCIs. In this paper, a carrier-based PWM strategy to balance line to line output voltages and to maximize the linear modulation range where the

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output voltage can be linearly controlled in the MLCI operating under unbalanced dc-link conditions proposed In unbalanced dc-link conditions, the maximum synthesizable voltage in each phase is not uniform. Consequently, the linear modulation range is reduced, and a significant.

II VOLTAGE VECTOR SPACE ANALYSIS

H-bridge module incorporates voltage and current sensing circuitries, gate drivers, and communication interfaces between the module itself and the main controller. In addition, battery cells can be also included in the H-bridge module. The unipolar modulation technique is applied between two switching legs in the H-bridge module. Consequently, the effective switching frequency in each H-bridge module is twice the carrier frequency. In addition to this, the well-known PS modulation technique is used to implement interleaving and multilevel operation. Therefore, the effective switching frequency f_{sw} in a phase is

$$f_{sw} = 2N \times f_c \quad (1)$$

Where N and f_c represent the number of the H-bridge modules in each phase and the carrier frequency of PWM, respectively. As an example, Fig. 2 shows the carriers for each module, the duty cycles in unipolar modulation, and the output voltage when $N = 2$.

VOLTAGE VECTOR SPACE ANALYSIS:

When the dc-link voltage of a single H-bridge module is V_{dc} , the output voltage v_{pn} has three states, i.e., V_{dc} , 0, and $-V_{dc}$,

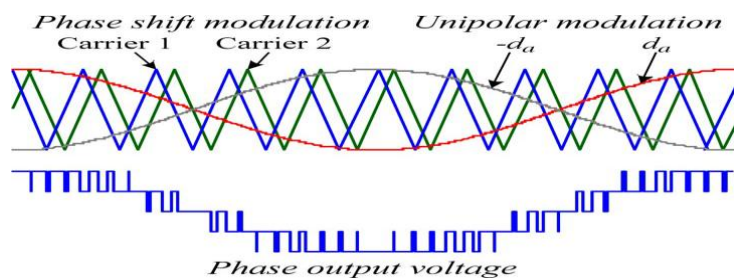


Figure1: Unipolar and phase shift modulation for single H-bridge module.

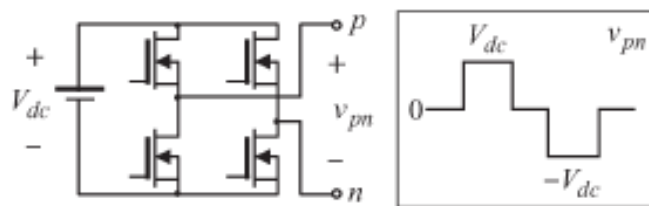


Figure2: Output voltage of a single H-bridge module.

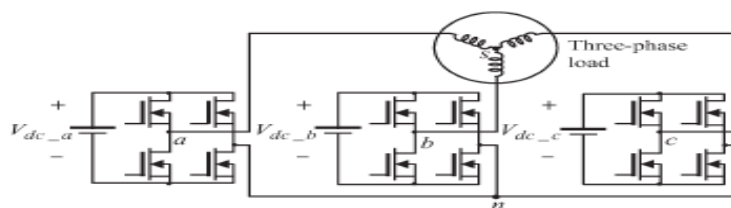


Figure3: One-by-three configuration MLCI.

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As shown in Fig2. By adopting the concept of a switching function, it can be represented as

$$v_{pn} = S_p V_{dc}$$

$$S_p \in \{-1,0,1\} p = a, b, c \quad (2)$$

Where S_p is a switching function and p can be replaced with $a, b,$ or $c,$ which represent the phases. Fig.3 shows a simple one-by-three configuration MLCI. For voltage vector space analysis, the main concept is derived from this simple topology, and then, it is expanded to more levels. The voltage between the output point of each phase and the load side neutral point s is specified as the phase voltage. The phase voltages include $v_{as}, v_{bs},$ and $v_{cs}.$ By using this concept, the voltage between the two neutral points is defined as v_{sn} and can be written as

$$v_{sn} = -v_{an} + v_{sn} = -v_{bs} + v_{bn} = -v_{cs} + v_{cn} \quad (3)$$

By using the condition that the sum of all phase voltages is zero because the load does not have a neutral line, v_{sn} is rewritten as

$$v_{sn} = \frac{1}{3} (v_{an} + v_{bn} + v_{cn}) \quad (4)$$

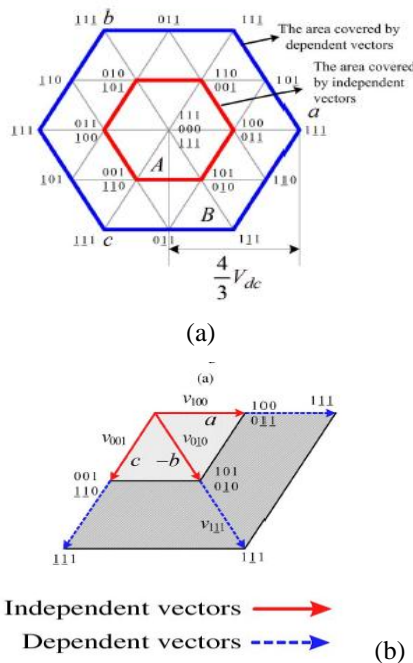


Figure 4. Voltage vector space of one-by-three configuration MLCI.

By substituting (4) into (3), the phase voltage of each phase is represented as follows by using the relationship defined in (2)

$$\begin{aligned} v_{as} &= \frac{2}{3} S_a V_{dc_a} - \frac{1}{3} S_b V_{dc_b} - \frac{1}{3} S_c V_{dc_c} \\ v_{bs} &= -\frac{1}{3} S_a V_{dc_a} + \frac{2}{3} S_b V_{dc_b} - \frac{1}{3} S_c V_{dc_c} \\ v_{cs} &= -\frac{1}{3} S_a V_{dc_a} - \frac{1}{3} S_b V_{dc_b} + \frac{2}{3} S_c V_{dc_c} \end{aligned} \quad (5)$$

If the magnitudes of three dc links are balanced so that $V_{dc_a}, V_{dc_b},$ and V_{dc_c} have the same value $V_{dc},$ the voltage vector space in $\alpha-\beta$ coordinates is defined in Fig. 4(a) by using (5). In the figure, underbars indicate that the switching function has the value of $-1.$ A part of the hexagon in Fig. 5.4(a) is shown in Fig. 4(b). In this figure, the vectors v_{010} and v_{111} are placed at the same reference axis, phase $b.$

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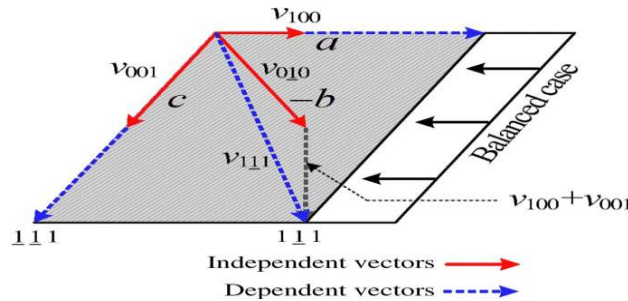


Figure 5. Voltage vector space in an unbalanced dc-link condition.

However, the constituents of those vectors are different. For v_{010} , this vector can be synthesized without the other two phases' assistance. However, v_{111} cannot be produced without other vectors according to (5). From this, let the vectors which do not require other two phases' assistance to be defined as "the independent vectors." Similarly, the vectors which require other phases' support are defined as "the dependent vectors." According to these definitions, v_{100} , v_{001} , and v_{010} are the independent vectors, while v_{111} , v_{111} , and v_{111} are the dependent vectors in Fig. 4(b). Fig. 4(a) also compares the regions that can be composed by the independent

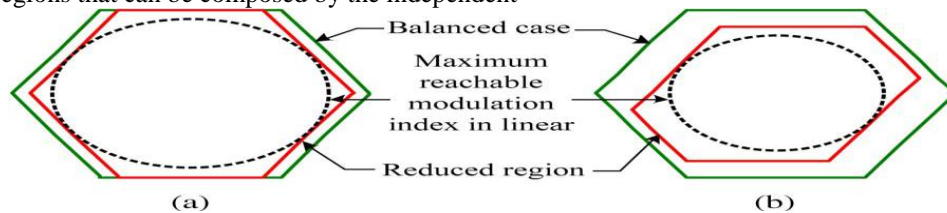


Figure 6. Comparison of the voltage vector space under different dc-link ratios.

(a) $V_{dc_a} < V_{dc_b} = V_{dc_c}$. (b) $V_{dc_b} < V_{dc_a} < V_{dc_c}$.

(b)

and the dependent vectors. Unlike traditional three-phase half bridge inverters, the independent vectors can be fully applied in a switching period because the dc links in each of the three phases are separated in the given system. It should be noted that the maximum voltage is decided by the dependent vectors in the entire voltage vector space. Now, let us consider the case when a three-phase load is supplied by unequal dc links. V_{dc_a} has a lower value than the others. In Fig. 5.6(b), all three dc links have different voltages. As it can be seen in Fig. 5.6, the original shape of the hexagon is distorted in both cases. As shown in Fig. 5.6, the radius is changed as the hexagon distorts, and the achievable linear modulation range is also altered. Here, the maximum amplitude of the phase voltage V_{ph_max} in the linear modulation range is defined as

$$V_{ph_max} = V_m (V_{dc_max} \sqrt{3}/2)$$

$$V_m = \left(\frac{4}{3} - \frac{2V_{dc_max} - V_{dc_mid}}{3V_{dc_max}} - \frac{2V_{dc_max} - V_{dc_max}}{3V_{dc_max}} \right) \quad (6)$$

Where V_{dc_max} , V_{dc_mid} , and V_{dc_min} represent the maximum, medium, and minimum voltages among the dc links. In fact, (6) can be simplified as

$$V_{ph_max} = \frac{V_{dc_mid} + V_{dc_min}}{\sqrt{3}} \quad (7)$$

III. NVM METHOD

TRADITIONAL OFFSET VOLTAGE INJECTION METHOD:

The offset voltage injection scheme is a popular technique in three-phase half-bridge inverter applications. The theory behind this is that an offset voltage is incorporated with phase voltage

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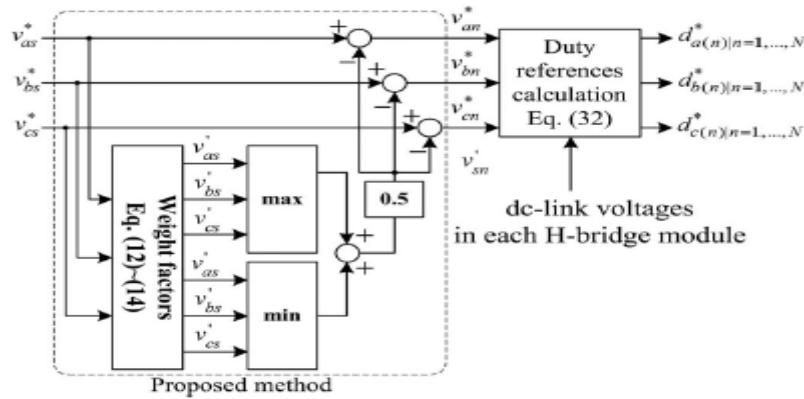


Figure6. Implementation of the NVM method.

References to implement various PWM schemes in carrier-based PWM by using the fact that line-to-line voltages are applied to a three-phase load. For example, the offset voltage v_{sn}^* is injected to the phase voltage references v_{as}^* , v_{bs}^* , and v_{cs}^* to implement carrier-based SVPWM as in

$$v_{sn}^* = \frac{v_{max}^* + v_{min}^*}{2} v_{max}^* = \max(v_{as}^*, v_{bs}^*, v_{cs}^*)$$

$$v_{min}^* = \max(v_{as}^*, v_{bs}^*, v_{cs}^*)$$

NVM METHOD USED:

If the dc links in an MLCI are unbalanced and the traditional offset voltage injection methods are utilized, the three-phase output voltages may become distorted as the phase voltage. Fig. 8 shows the concept of the proposed NVM technique. Here, a neutral voltage between the two neutral points n and s in Fig. 4 is modulated to compensate the output voltage imbalance caused by unbalanced dc-link conditions. To do this, first, the weight constant K_w is defined as

$$K_w = \frac{V_{dc_min} + V_{dc_min}}{2}$$

It should be noted that, depending on dc-link conditions, the sum of v_{as} , v_{bs} , and v_{cs} may not be zero. By using these components, the injected voltage v_{sn} and the pole voltage references are given as

$$v_{sn}^* = \frac{v_{max}^* + v_{min}^*}{2} \quad \begin{matrix} v_{max}^* = \max(v_{as}^*, v_{bs}^*, v_{cs}^*) \\ v_{min}^* = \max(v_{as}^*, v_{bs}^*, v_{cs}^*) \end{matrix}$$

$$\begin{bmatrix} v_{an}^* \\ v_{bn}^* \\ v_{cn}^* \end{bmatrix} = \begin{bmatrix} v_{an}^* - v_{sn}^* \\ v_{bn}^* - v_{sn}^* \\ v_{cn}^* - v_{sn}^* \end{bmatrix}$$

From (15), the line-to-line voltages across each phase of the load are represented as

$$\begin{bmatrix} v_{an}^* \\ v_{bn}^* \\ v_{cn}^* \end{bmatrix} = \begin{bmatrix} v_{an}^* - v_{bn}^* \\ v_{bn}^* - v_{cn}^* \\ v_{cn}^* - v_{an}^* \end{bmatrix} = \begin{bmatrix} v_{an}^* - v_{sn}^* - v_{bs}^* + v_{sn}^* \\ v_{bn}^* - v_{sn}^* - v_{cs}^* + v_{sn}^* \\ v_{cn}^* - v_{sn}^* - v_{as}^* + v_{sn}^* \end{bmatrix}$$

$$= \begin{bmatrix} v_{as}^* - v_{bs}^* \\ v_{bs}^* - v_{cs}^* \\ v_{cs}^* - v_{as}^* \end{bmatrix}$$

As it can be seen, v_{sn} does not appear in the line-to-line voltages, and it is still considered as a hidden freedom of voltage modulation. Now, let us consider the role of the weight factors K_{w_a} , K_{w_b} , and K_{w_c} , which are inversely

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proportional to the corresponding dc-link voltage. For convenience, let us assume that the magnitudes of the dc-link voltage are under the following relationship:

$$V_{dc\ a} < V_{dc\ b} < V_{dc\ c}$$

Then,

$$K_{w\ a} > K_{w\ b} > K_{w\ c} \quad K_{w\ a} > 1$$

$$K_{w\ b}, K_{w\ c} < 1$$

Equation 9 gives

$$|v'_{as}| > |v^*_{as}| \quad |v'_{as}| < |v^*_{bs}| \quad |v'_{cs}| < |v^*_{cs}|$$

It can be recognized that, if v'_{as} , whose dc-link voltage is less than the others, is corresponding to v'_{max} or v'_{min} , the absolute value of v'_{sn} is greater than v^*_{sn} . On the other hand, the final pole voltage references v^*_{an} , v^*_{bn} , and v^*_{cn} are calculated by subtracting v'_{sn} from the original phase voltage references v^*_{as} , v^*_{bs} , and v^*_{cs} . From this reasoning, in this example, it is supposed that, if v'_{as} is corresponding to v'_{max} , then the final pole voltage references v^*_{an} , v^*_{bn} , and v^*_{cn} are less than the original pole voltage references

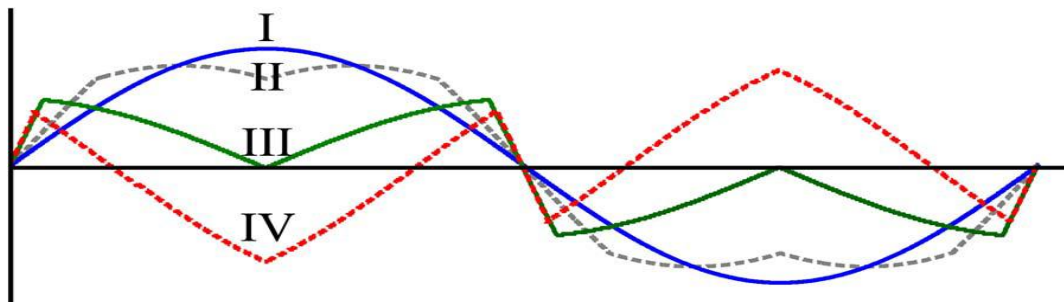


Figure7: Comparison of modulated waveforms. (I) Without v^*_{sn} . (II) Traditional carrier-based SVPWM. (III) NVM with $V_{dc\ a} = 0.275 V_{dc}$, $V_{dc\ b} = V_{dc}$, and $V_{dc\ c} = V_{dc}$. (IV) NVM with $V_{dc\ a} = 0.2 V_{dc}$, $V_{dc\ b} = V_{dc}$, and $V_{dc\ c} = V_{dc}$.

which are not considering v'_{sn} but v^*_{sn} . On the contrary, if v'_{cs} is v'_{max} , then the final pole voltage references are greater than the original pole voltage references. By using this principle, the used method reduces the portion of the phase whose dc-link voltage is smaller than the others and increases the utilization of the phase in which the dc-link voltage is greater than those of the other phases. However, as it can be seen in(16), v'_{sn} does not affect the line-to-line voltages. Therefore, the line-to-line voltage is the same as the one derived from the original phase voltage reference. From this analysis, the used method enables the maximum synthesizable modulation index in the linear modulation range under the unbalanced dc-link conditions to be achieved. In addition to this, if all of the dc-link voltages are well balanced so that $V_{dc\ a}$, $V_{dc\ b}$, and $V_{dc\ c}$ are equal to V_{dc} .

$$K_w = \frac{V_{dc\ mid} = V_{dc\ min} = V_{dc}}{V_{dc\ min} + V_{dc\ min}} = V_{dc}$$

$$K_{w\ a} = K_{w\ b} = K_{w\ c} = 1$$

$$v'_{as} = v^*_{as} \quad v'_{bs} = v^*_{bs} \quad v'_{cs} = v^*_{cs}$$

Equation shows that the proposed method gives the same voltage references as the traditional method under balanced dc-link conditions.

IV. SIMULATION RESULTS

Simulink Model of NVM technique:

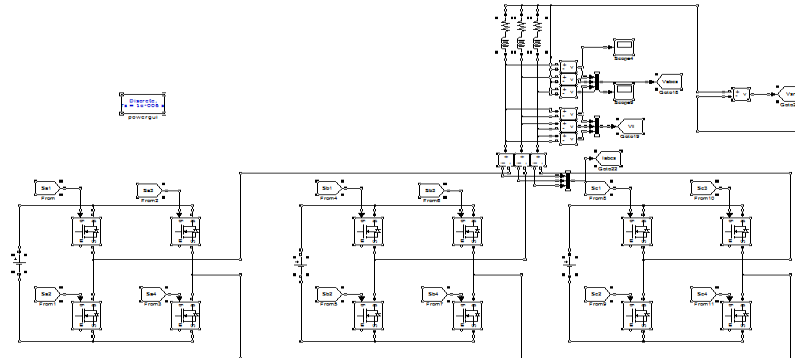


Figure 7: Simulink Model of NVM technique

Control circuit by using svpwm and nvm technique

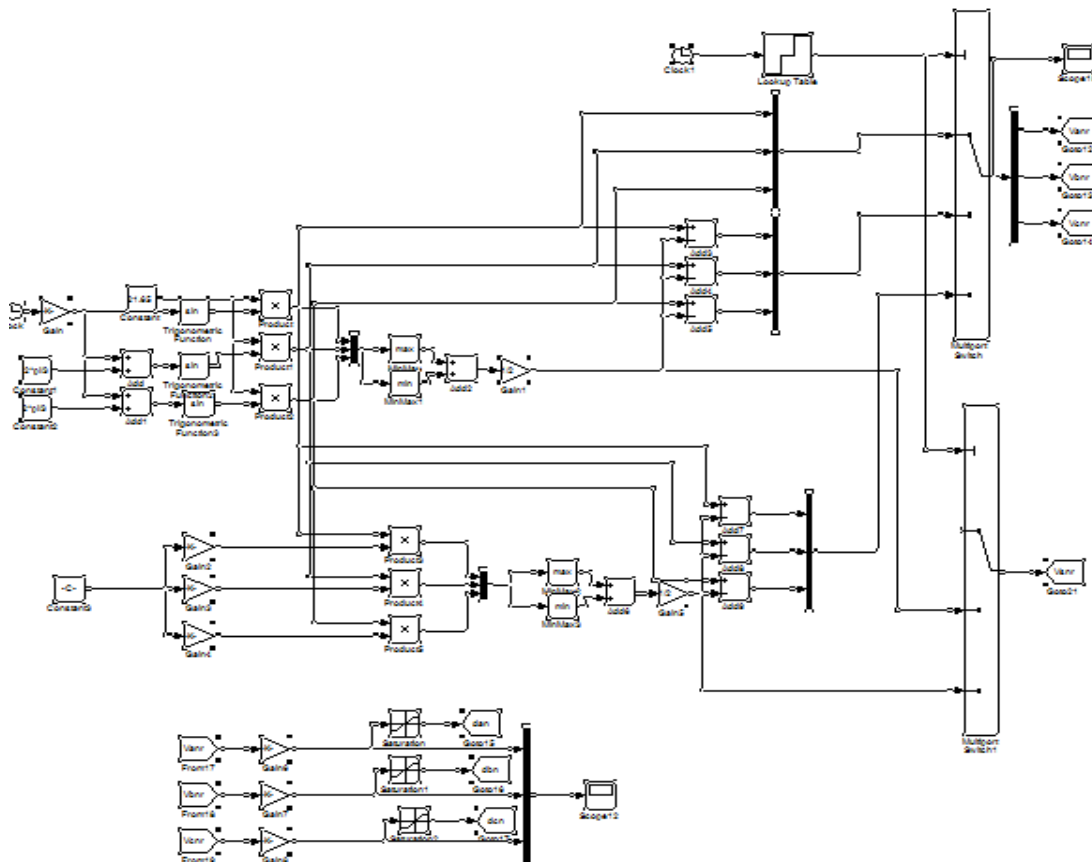


Figure8: Control circuit by using SVPWM and NVM technique

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SIMULATION RESULTS:

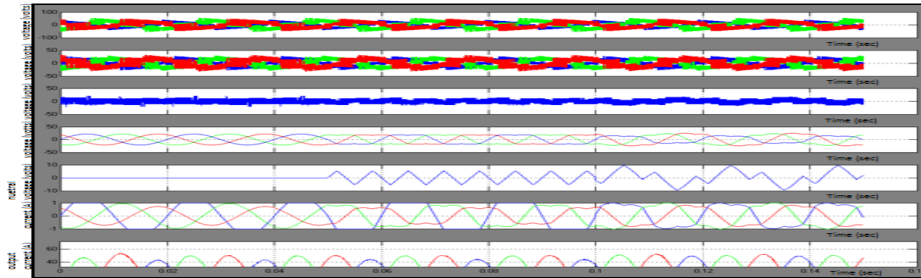


Figure 9: a) phase voltage b) phase to neutral voltage c) load to neutral voltage d) duty ratio e) phase currents
f) balanced output currents

V. CONCLUSION

The NVM technique for MLCIs under unbalanced dc-link conditions has been in this paper. In order to analyze the maximum synthesizable voltage of MLCIs, the voltage vector space has been analyzed using the switching function. From the analysis, the maximum linear modulation range was derived. The NVM technique is applied to achieve the maximum modulation index in the linear modulation range under an unbalanced dc-link condition as well as to balance the output phase voltages. Compared to the previous methods, the proposed technique is easily implemented and improves the output voltage quality under unbalanced dc-link conditions. Both simulations and experimental results based on the IPM motor drive application verify the effectiveness of the method.

REFERENCES

- [1] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.
- [2] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-voltage multilevel converters—State of the art, challenges, and requirements in industrial applications," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2581–2596, Aug. 2010. CHO *et al.*: CARRIER-BASED NVM STRATEGY FOR MLCIs UNDER UNBALANCED DC SOURCES 635
- [3] J.-S. Lai and F. Z. Peng, "Multilevel converters—A new breed of power converters," *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 509–517, [4] M. May/June 1996.
- [4] Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Perez, "A survey on cascaded multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2197–2206, Jul. 2010.
- [5] J. Rodriguez, L. G. Franquelo, S. Kouro, J. I. León, R. C. Portillo, M. A. M. Prats, and M. A. Perez, "Multilevel converters: An enabling technology for high-power applications," *Proc. IEEE*, vol. 97, no. 11, pp. 1786–1817, Nov. 2009.
- [6] G. Bergna, E. Berne, P. Egrot, P. Lefranc, A. Arzande, J.-C. Vannier, and M. Molinas, "An energy-based controller for HVDC modular multilevel converter in decoupled double synchronous reference frame for voltage oscillation reduction," *IEEE Trans. Ind. Electron.*, vol. 60, no. 6, pp. 2360–2371, Jun. 2013. [7] Z. Shu, N. Ding, J. Chen, H. Zhu, and X. He, "Multilevel SVPWM with DC-link capacitor voltage balancing control for diode-clamped multilevel converter based STATCOM," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1884–1896, May 2011.
- [8] J. Chavarria, D. Biel, F. Guinjoan, C. Meza, and J. J. Negroni, "Energy balance control of PV cascaded multilevel grid-connected inverters under level-shifted and phase-shifted PWMs," *IEEE Trans. Ind. Electron.*, vol. 60, no. 1, pp. 98–111, Jan. 2013.
- [9] G. Buticchi, E. Lorenzani, and G. Franceschini, "A five-level single-phase grid-connected converter for renewable distributed systems," *IEEE Trans. Ind. Electron.*, vol. 60, no. 3, pp. 906–918, Mar. 2013.
- [10] J. A. Munoz, J. R. R. Espinosa, C. R. Baier, L. L. Morán, E. E. Espinosa, P. E. Melín, and D. G. Sbarbaro, "Design of a discrete-time linear control strategy for a multicell UPQC," *IEEE Trans. Ind. Electron.*, vol. 59, no. 10, pp. 3797–3807, Oct. 2012.