A Comprehensive Study on Power Reduction Techniques in Deep Submicron Technologies

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ABSTRACT:The use of Very Large Scale Integration (VLSI) technologies in high performance computing, wireless communication and consumer electronics has been growing at a very fast rate.For the most recent CMOS technologies static power dissipation i.e. leakage power dissipation has become a challenging area for VLSI chip designers.A comprehensive study and analysis of various leakage power minimization techniques have been presented in this paper. The present research study and its corresponding analysis are mainly focusing on circuit performance parameters.

KEYWORDS: Sub threshold leakage current,Leakage power consumption,Sub-threshold Leakage, Threshold voltage.

I.INTRODUCTION

Power consumption is one of the top issues of VLSI circuit design, for which CMOS is the primary technology.Today's focus on low power is not only because of the recent growing demands of mobile applications. Even before themobile era, power consumption has been a fundamental problem. To solve the power dissipation problem, manyresearchers have proposed different ideas from the device level to the architectural level and above. However, there is nouniversal way to avoid tradeoffs between power, delay and area and thus, designers are required to choose appropriatetechniques that satisfy application and product needs.With recent advancements in semiconductor technology the density of transistors in Integrated Circuits is still growing,which in turn demands expensive cooling and packaging technologies. Keeping this in view, the supply voltages are scaleddown for reducing the switching power dissipation. Moreover, the threshold voltage is also scaled down for the performancetradeoffs. However, the scaling of threshold voltage has resulted in exponential increase of subthreshold leakage current causingleakage (static) power dissipation. Static power dissipation is now growing considerably proportional to the switching dynamicpower dissipation in deep submicron technologies and battery operated devices. The longer the battery lasts, the better theleakage power savings [2]-[3].

The four main sources of leakage current in a CMOS transistor are i) Reverse-biased junction leakage current ii) Gate induced drain leakage iii) Gate direct-tunnelling leakage and iv) Subthreshold (weak inversion) leakage current.The subthreshold leakage current being the most predominant amongst all the leakage currentsources becomes extremely challenging for research in current and future silicon technologies.In a short channel device, however, the source and drain depletion width in the vertical direction and the source drain potential have a strong effect on the band bending over a significant portion of the device. Therefore, thethreshold voltage and consequently the sub threshold current of short channel devices vary with the drain bias.This effect is referred to as Drain-Induced Barrier Lowering (DIBL)

$$I_{ds} = \mu_0 * C_{ox} * \frac{W}{L} * (m-1) * (V_{th}^2) * e^{\frac{Vgs - Vth}{(m-Vt)}} * (1 - e^{-Vds/Vt})$$

(Where m = 1 + C_{dm}/C_{ox}, m is the sub-threshold swing co-efficient, C_{dm} is capacitance of the depletion layer, C_{ox} isthe capacitance of the oxide layer, μ_0 is the mobility, Vth is the threshold voltage, V_{gs} is the gate to source voltage, V_{ds} isthe drain to source voltage and V_t is the thermal voltage.According to technology trend for the high density the transistor size should be scale down and for highperformance the threshold voltage (V_{th}) scaling down. In the case of sub-threshold leakage if scaling down of V_{th} , theleakage power increase exponentially as Vth decrease and the short channel effect the channel controlled by drain. But incase of gate oxide leakage gate tunneling due to thin oxide and high k-dielectric could be possible solution and anothermotivation leakage power reduction technique can potentially increase the battery life. With application of dual thresholdvoltage (V_{th}) techniques the sleep, zigzag and sleepy stack approaches result in orders of magnitude sub-thresholdleakage power reduction.There areseveral current components which are responsible for theleakage power dissipation in VLSI circuits. The modernisedcooling and packaging strategies are of little help to therapid increase of the power consumption in today's chips. The diagram of leakage current mechanism of deep-submicrometre transistors is depicted below:
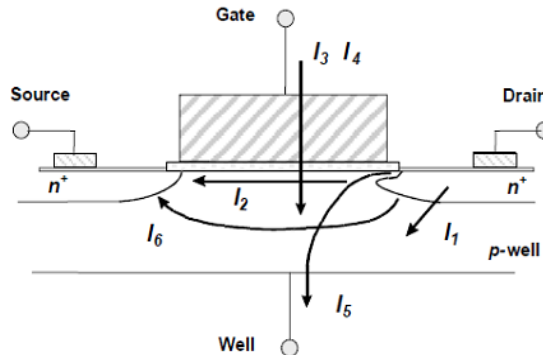
Figure1. Leakage Current Mechanism of deep-submicrontransistor

I1= Reverse-bias p-n junction diode leakage current
I2 = Subthreshold leakage current
I3 = Gate Oxide tunnelling current
I4 = Hot-carrier injection current
I5 =Gate induced drain-leakage current (GIDL)
I6 = Channel punch-through

The dependence of subthreshold current [6] on the transistorparameters are listed in the Table 1.

Table 1: Dependence of sub threshold leakage on device parameters

Parameter	Dependence
Temperature(T)	Exponential increase
Transistor length(L)	Inversely proportional
Transistor width (L)	Directly proportional
Input voltage(V_{gs})	Exponential increase
Transistor Threshold voltage(V_{th})	Increases by an order of magnitude with 100mV decrease

There are various leakage power reduction techniques based on modes of operation of systems. The two operational modesare a) active mode and b) standby (or) idle mode. Most of the techniques aim at power reduction by shutting down the powersupply to the system or circuit during standby mode.

II.LITERATURE SURVEY

In today's VLSI circuits, low power is an important consideration factor along with high performance and high density. There are several techniques to reduce the leakage power but disadvantage of each technique limits its implementation.

A. Dual VT and MTCMOS: This is a basic approach to reduce the leakage power.MTCMOS reduces the leakage by introducing the highthreshold NMOS gating between pull down network andground terminal, in series to low threshold voltage circuitry.As stated in [6] Dual VT technique is a variation inMTCMOS, in which high threshold voltage can be assignedto transistors of non-critical path to reduce leakage currentand low threshold voltage transistors are used in criticalpaths. An additional mask layer is required due to VT(Threshold voltage) variation, thereby making fabricationprocess complicated.This technique suffers from latencyperiod i.e. it need some time to get into normal operatingmode after reactivation. The structure for dual VT andMTCMOS technique is shown as:
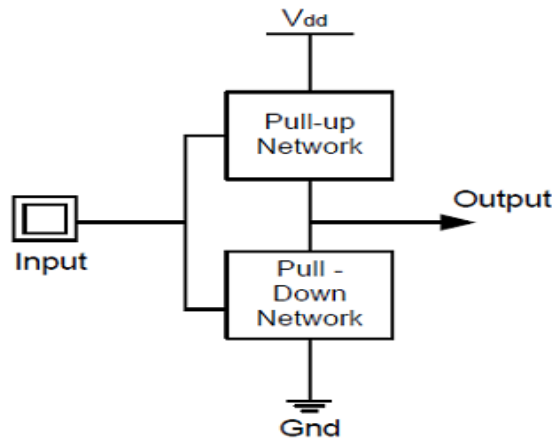
Figure 2: Dual VT and MTCMOS Structure

B. Sleep Transistor Technique: Addition to the MTCMOS technique, high VT sleeptransistor is introduced between VDD (supply voltage) andpull up network, and between pull down network andground for high switching speed, where low VT transistorsare used in circuit [10]. Efficient power management is doneby sleep control mechanism. This modified MTCMOStechnique can only reduce the standby leakage power andthe introduced MOSFETs results increase in area and delay.

During stand-by mode both sleep transistors gets turned off,introducing large resistance in conduction path and thus,leakage current is low. Isolation between VDD and groundpath is necessary for leakage reduction. This technique facesa problem for data retention purpose during sleep mode. TheWakeup time and energy of the sleep technique have asignificant impact on the efficiency of the circuit.
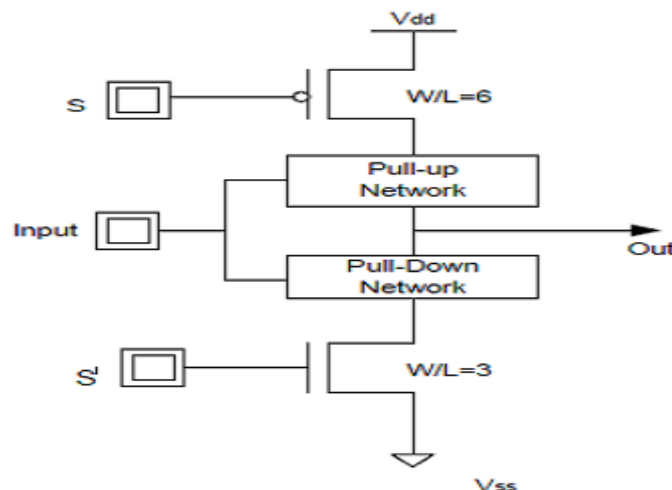

Figure 3: Sleep Transistor Approach

C. Input vector control (IVC): The strong dependence of leakage power values on the input combination is given by Abdollahi et al [11] by citing anexample of 2-input NAND gate to illustrate the concept of transistor stacking. The minimum leakage causing input vector isidentified by an automation process and is applied to the circuit under sleep mode. An algorithm to obtain the minimum leakagevector (MLV) is given by [11].

D. Variable threshold CMOS (VTMOS): This technique involves dynamically modifying the threshold voltage during active mode, which is classically known asstandby power reduction (SPR). In this method the threshold voltage Vth is raised during the standby mode by connecting thesubstrate voltage either lower than (for N transistors) or higher than ground (for P transistors). The major drawback of thistechnique is that it requires an additional power supply, which may not be appropriate in some commercial designs.

III.PROPOSED ALGORITHM

In LECTOR [8], the concept of effective stacking transistors has been introduced between the VDD and GND for the leakage power reduction. In this technique two leakage control transistors i.e. P-type and N-type are insertedbetween the pull up and pull down network of a circuit, inwhich each LCT gate is controlled by the source of other, hence termed as self-controlled stacked transistors. Since itis a self-controlled technique so no external circuit isrequired for controlling purpose. These LCT produces highresistance path between the VDD and GND by turning morethan one transistor OFF, thereby reducing the leakagecurrent. This technique has a very low leakage but there isno provision of sleep mode of operation for state retention.
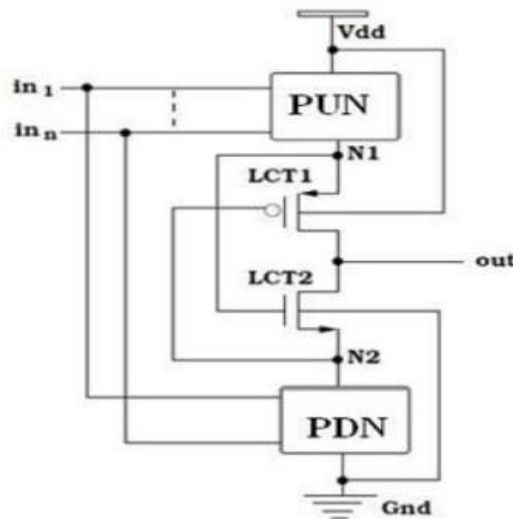

Figure 4: LECTOR Approach

A.   LECTOR Stack State Retention (LSSR)

LECTOR Stack State Retention (LSSR)This technique combines the feature of both, LECTORapproach and the Forced Stack Technique with theadditional feature of state retention in circuit. The circuitconfiguration includes [1], two leakage control transistorsare added between the pull up and pull down network, andthe stack effect is introduced to pull up and pull downnetwork by replacing each existing transistor with two halfsized transistors. It provides the limitation of area because ofusage of extra transistors to preserve the circuit state duringsleep mode. But this technique provides good leakagecurrent reduction without any delay penalty.
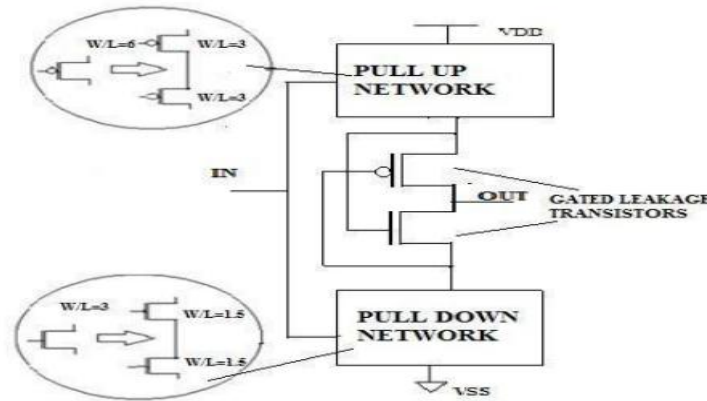
Figure 5: LECTOR Stack State Retention (LSSR)Approach

IV.CONCLUSION

The present study provides an appropriate choice for leakage power minimization technique for aspecific application by a VLSI circuit designer based on sequential analytical approach.To solve the problem,several approaches have been implanted and still work is inprogress on many more. The designers, therefore, have toselect particular technique depending on application andproduct requirements. In this paper, we have presented theseveral leakage power reduction techniques along with theirrespective advantages and disadvantages. We conclude thatLECTOR and the new approach LSSR circuit may lead tomuch large reduction of leakage power than the previouslyintroduced techniques.

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BIOGRAPHY

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