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Low Complexity Filter Bank Architecture for Software Defined Radio Receivers

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ABSTRACT: The ability to support multiple channels of different communication standards, in the available bandwidth, is of importance in modern software defined radio (SDR) receivers. An SDR receiver typically employs a channelizer to extract multiple narrowband channels from the received wideband signal using digital filter banks. Since the filter bank channelizer is placed immediately after the analog-to-digital converter (ADC), it must operate at the highest sampling rate in the digital front-end of the receiver. Therefore, computationally efficient low complexity architectures are required for the implementation of the channelizer. The compatibility of the filter bank with different communication standards requires dynamic reconfigurability. The design and realization of dynamically reconfigurable, low complexity filter banks for SDR receivers is a challenging task. This paper reviews some of the existing digital filter bank designs and investigates the potential of these filter banks for channelization in multi-standard SDR receivers.

KEYWORDS: Channelization , Software defined radio , Digital filter banks , Reconfigurability, Low complexity.

I.INTRODUCTION

Software radios can significantly reduce the cost and complexity of today's cellular radio base stations. Software radios architectures centre on the use of wide band (WB) A/D converters and D/A converters as close to the antenna as possible, with as much radio functionality as possible implemented in the digital domain.The reconfigurable FIR filters are widely used in multiband mobile communication system**.** The most computationally demanding block in the digital front-end of a software defined radio (SDR) receiver is the channelizer which operates at the highest sampling rate. Channelizers are employed in the SDR receivers for extracting individual channels (frequency bands) from the digitized wideband input signal. SDR can be regarded as an ultimate communications solution which can ideally cover any cellular communication standard in a wide frequency spectrum with any modulation and bandwidth. An SDR receiver typically employs a channelizer to extract multiple narrowband channels from the received wideband signal using digital filter banks. Since the filter bank channelizer is placed immediately after the analog-to-digital converter (ADC), it must operate at the highest sampling rate in the digital front-end of the receiver. Therefore, computationally efficient low complexity architectures are required for the implementation of the channelizer. The compatibility of the filter bank with different communication standards requires dynamic reconfigurability [3].

SDR can be regarded as an ultimate communications solution which can ideally cover any cellular communication standard in a wide frequency spectrum with any modulation and bandwidth. FPGA based channelizers are essential components and enable channel selection to be configurable based on the end application. The goal is to obtain maximum use of a single design through software reconfiguration of hardware assets and dynamic configuration and selection of channels, while ensuring highest level of fidelity of signals received at the destination [4].

II. BACKGROUND

The PC approach is a straightforward approach and hence relatively simple. But the main drawback is that, the number of branches of filtering-DDC-SRC is directly proportional to the number of received channels i, e. The complexity of the PC approach is directly proportional to the number of channels. Hence the PC approach is not efficient when the number of received channels is large. The filters used in the PC approach are of a very high order and this results in

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high area complexity and thus increased static power. DFTFBs cannot extract channels with different bandwidths known as non uniform channels, because they are modulated FBs with equal bandwidth forall bandpass filters –the bandwidths are same as that of the prototype LPF. Therefore, for multi-mode receivers, distinct DFTFBs are required for each communication standard. Hence the complexity the channelizer increases linearly with the number of standards. available. A uniform DFTFB can be realized by implementing one low-pass filter (LPF) and a corresponding modulator such as DFT. The limitation of the DFTFB is that the channel filters have fixed equal bandwidths corresponding to the specification of a given standard. The limitations of DFTFBs for SDR receiver applications is that DFTFBs cannot extract channels with different bandwidths known as non uniform channels. Therefore, for multi-mode receivers, distinct DFTFBs are required for each communication standard. Hence the complexity of channelizer increases linearly with the number of standards. The limitations of DFTFBs is that the channel filters have fixed equal bandwidths corresponding to the specification of a given standard.R. MAHESH et.al. in paper [3] entitled "Reconfigurable Low Area Complexity Filter Bank Architecture Based on Frequency Response Masking for Non uniform Channelization in Software Radio Receivers" proposed a new reconfigurable FB based on the FRM approach for extracting multiple channels of non uniform bandwidths. The FRM approach is modified to achieve following advantages: 1) incorporate reconfigurability at the filter level and architectural level, 2) improve the speed of filtering operation, and 3) reduce the complexity.

In reconfigurable FB based on the FRM approach conventional FIR filter designs are used. so, higher order filters are required to obtain sharp transition-band. The complexity of FIR filters increases with the filter order.

III.METHODOLOGY

It is well known that one of the efficient ways to reduce the complexity of multiplication operation is to realize it using shift and add operations. In contrast to conventional shift and add units are used in previously proposed reconfigurable filter architectures. A *programmable shifter* is more complex. Often the speed of multiplication *limits* the performance of the digital processor. So, we can use barrel shifter (a circuit that shifts multiple bits at a time) in proposed architecture instead of programmable shifter. The time required/delay will considerably improve by doing this and the proposed architecture is modified for reducing its complexity.

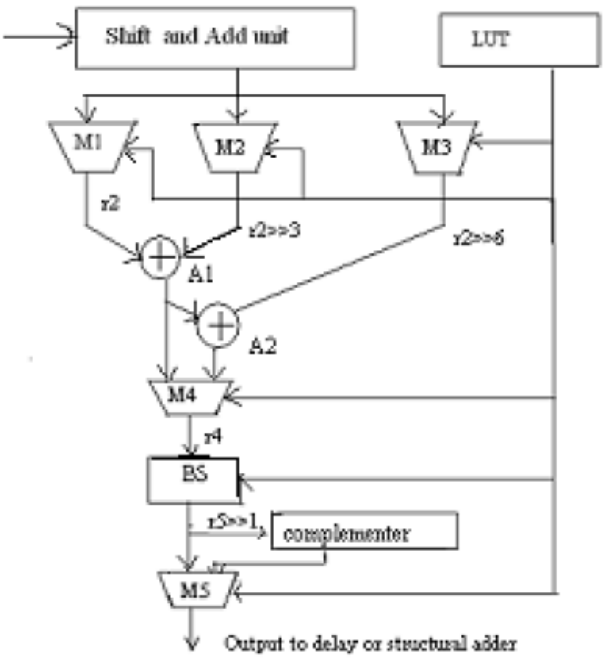

Fig.1 Reconfigurable filter architecture

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Barrel shifters have the ability to shift data words in a single operation over standard shift left or shift right registers that utilize more than one clock cycle. Barrel shifters will continue to be used in smaller devices because it has a speed advantage over software implemented ones. In general, it can be concluded that a barrel-shifter is appropriate for smaller shifters. For large shift values, the log shifter becomes more effective, in terms of area and speed. Also log shifter is more regular and hence can be easily generated automatically.In reconfigurable FIR filter architectures based on a binary sub-expression elimination (BSE) algorithm has been proposed. The architecture is consisted of a shift and add unit which will generate all the 3-bit BCSs using 3 adders. The proposed architecture of the filter for an 8-bit coefficient is shown in figure.4. M1 and M2 are 8:1 multiplexers; M3 is a 4 : 1 multiplexer and M4 and M5 are 2 : 1 multiplexers. The input is given to the shift and add unit whose output is shared among the multiplexers.

IV. EXPERIMENTAL RESULTS

In this section, the synthesis results of the FRM FB, and modified FB architectures are presented and parameters like area and delay are compared. The comparison table states the architecture which has high speed and minimum delay. The Xilinx 9.1i ISE Virtex-II used for synthesizing purposes.

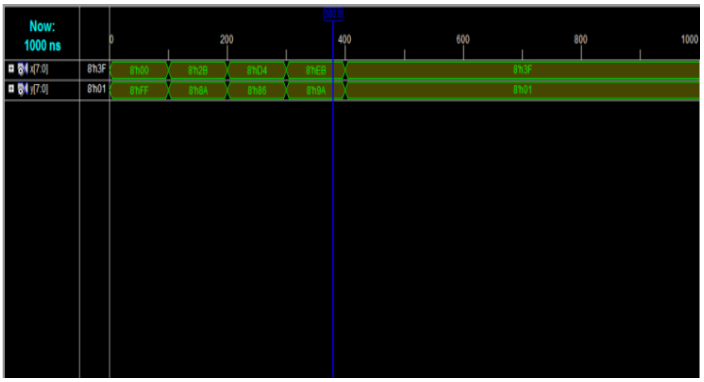

Table 1: The delay Comparison

Parameter	Existing Method From ref.3	Proposed Method
Delay(ns)	38.67	13.65

Table 2: The frequency Comparison between the Existing and Proposed Method

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Parameter	Existing Method From ref.3	Proposed Method
Frequency Of operation(speed MHz)	24	73.26

The comparison table states the architecture which has less area. The Xilinx 9.1i ISE spartan-III used for synthesizing purposes.

Parameter	From reference.4	Proposed Method
Area(slices)	20	14

Table 3: The area Comparison between the Existing and Proposed Method

V. CONCLUSION

The proposed reconfigurable filters architecture results in low area and low delay. The FRM reconfigurable technique is modified to improve the speed and reduce the complexity. Synthesis results show that the proposed FB offers area reduction.

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