ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

*(An ISO 3297: 2007 Certified Organization)*

**Vol. 4, Issue 12, December 2015**

# Switched Capacitor Cascaded Multilevel Inverter for High Frequency AC Power Distribution System

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**ABSTRACT***:* The increase in transmission frequency results in advantages compared to low or medium frequency distribution among various kinds of power applications. High-frequency inverter serves as source side in high-frequency ac (HFAC) power distribution system (PDS). However, it is difficult to obtain a high-frequency inverter with both simple circuit topology and straightforward modulation strategy. A novel switched-capacitor cascaded multilevel inverter is proposed in this paper, which is designed by a switched-capacitor frontend and H-Bridge backend. Through the conversion of series and parallel connections, the switched capacitor frontend increases the number of voltage levels. The output harmonics and the component counter can be significantly mitigated by increasing number of voltage levels.

**KEYWORDS**: Cascaded H-Bridge, high-frequency ac (HFAC), multilevel inverter, switched capacitor (SC), symmetrical phase-shift modulation (PSM).

## I.INTRODUCTION

High-Frequency AC (HFAC) Power Distribution System (PDS) potentially became an alternative to traditional dc distribution due to the reduced components and low cost. They are extensively used for applications such as computer, telecom, electric vehicle, and renewable energy micro grid. However, HFAC PDS has to confront the challenges from large power capacity, high Electromagnetic Interference (EMI), and severe power losses. A traditional HFAC PDS is made up of a high-frequency (HF) inverter, an HF transmission track, and numerous Voltage-Regulation Modules. HF inverter accomplishes the power conversion to accommodate the requirement of Point of Load. In order to increase the power capacity, the most popular method is to connect the inverter output in series or in parallel. However, it is impractical for HF inverter, because it is complicated to simultaneously synchronize both amplitude and phase with HF dynamics. Multilevel inverter is an effective solution to increase power capacity without synchronization consideration, so the higher power capacity can be easily achieved by multilevel inverter with reduced switch stress. Non polluted sinusoidal waveform with the lower Total Harmonic Distortion is critically caused by long track distribution in HFAC PDS. The higher number of voltage levels can effectively decrease total harmonics content of staircase output, thus significantly simplifying the filter design. HF power distribution is applicable for small-scale and internal closed electrical network in Electric vehicle due to moderate size of distribution network and effective weight reduction. The consideration of operation frequency has to make compromise between the ac inductance and resistance, so multilevel inverter with the output frequency of about 20 kHz is a feasible trial to serve as power source for HF EV application.

## II. CIRCUIT CONFIGURATION OF SC-CASCADED INVERTER WITH NINE-LEVEL

The circuit topology of nine-level inverter (N1 =2, N2 = 2), where $S_1$, $S_2$, $S_1^1$, $S_2^1$ as the switching devices of SC circuits (SC1 and SC2) are used to convert the series or parallel connection of $C_1$ and $C_2$ is shown in fig 1. S1a, S1b, S1c, S1d, S2a, S2b, S2c, S2d are the switching devices of cascaded H-Bridge. Vdc1 and Vdc2 are input voltage. D1 and D2 are diode to restrict the current direction. Iout and $v_o$ are the output current and the output voltage, respectively.

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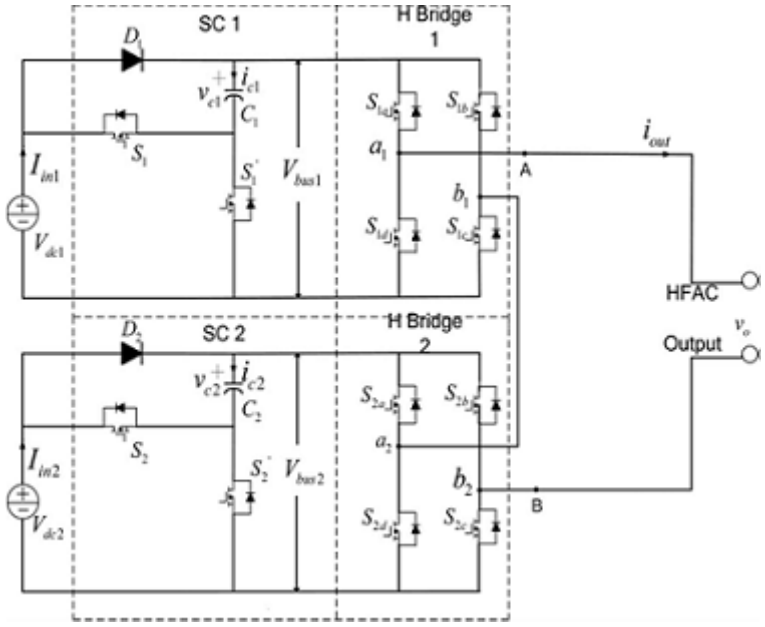


Fig 1 Nine Level Inverter

Fig 1 shows the nine level inverter which consists of two H-bridge inverter connected in cascade the output voltage has nine levels.

Table 1: Relations of on-state switches and output voltage

| Mode 1 | | | Mode 2 | | |
|---|---|---|---|---|---|
| On-state switches | Output voltage | Capacitor State | On-state switches | Output voltage | Capacitor State |
| $S_{1a}$, $S_{1c}$, $S_{2a}$, $S_{2c}$, $S_1$,$S_2$ | $4V_{in}$ | $C_1$, $C_2$ Discharging | $S_{1a}$, $S_{1c}$, $S_{2a}$, $S_{2c}$, $S_1$,$S_2$ | $4V_{in}$ | $C_1$, $C_2$ Discharging |
| $S_{1a}$, $S_{1c}$, $S_{2a}$, $S_{2c}$, $S_1'$, $S_2$ | $3V_{in}$ | $C_2$ Discharging | $S_{1a}$, $S_{1c}$, $S_{2a}$, $S_{2c}$, $S_1'$, $S_2$ | $3V_{in}$ | $C_2$ Discharging |
| $S_{1a}$, $S_{1c}$, $S_{2a}$, $S_{2c}$, $S_1'$ $S_2'$ | $2V_{in}$ | $C_1$, $C_2$ Charging | $S_{1a}$, $S_{1b}$, $S_{2a}$, $S_{2c}$, $S_1'$ $S_2$ | $2V_{in}$ | $C_2$ Discharging |
| $S_{1a}$, $S_{1b}$, $S_{2a}$, $S_{2c}$, $S_1'$ $S_2'$ | $V_{in}$ | $C_1$, $C_2$ Charging | $S_{1a}$, $S_{1b}$, $S_{2a}$, $S_{2c}$, $S_1'$ $S_2'$ | $V_{in}$ | $C_1$, $C_2$ Charging |
| $S_{1a}$, $S_{1b}$, $S_{2a}$, $S_{2b}$, $S_1'$ $S_2'$ or $S_{1c}$, $S_{1d}$, $S_{2c}$, $S_{2d}$ | 0 | $C_1$, $C_2$ Charging | $S_{1a}$, $S_{1b}$, $S_{2a}$, $S_{2b}$, $S_1'$ $S_2'$ or $S_{1c}$, $S_{1d}$, $S_{2c}$, $S_{2d}$ | 0 | $C_1$, $C_2$ Charging |
| $S_{1c}$, $S_{1d}$, $S_{2b}$, $S_{2d}$, $S_1'$ $S_2'$ | $-V_{in}$ | $C_1$, $C_2$ Charging | $S_{1c}$, $S_{1d}$, $S_{2b}$, $S_{2d}$, $S_1'$ $S_2'$ | $-V_{in}$ | $C_1$, $C_2$ Charging |
| $S_{1b}$, $S_{1d}$, $S_{2b}$, $S_{2d}$, $S_1'$ $S_2'$ | $-2V_{in}$ | $C_1$, $C_2$ Charging | $S_{1c}$, $S_{1d}$, $S_{2b}$, $S_{2d}$, $S_1'$ $S_2$ | $-2V_{in}$ | $C_2$ Discharging |
| $S_{1b}$, $S_{1d}$, $S_{2b}$, $S_{2d}$, $S_1'$, $S_2$ | $-3V_{in}$ | $C_2$ Discharging | $S_{1b}$, $S_{1d}$, $S_{2b}$, $S_{2d}$, $S_1'$, $S_2$ | $-3V_{in}$ | $C_2$ Discharging |
| $S_{1b}$, $S_{1d}$, $S_{2b}$, $S_{2d}$, $S_1$,$S_2$ | $-4V_{in}$ | $C_1$, $C_2$ Discharging | $S_{1b}$, $S_{1d}$, $S_{2b}$, $S_{2d}$, $S_1$,$S_2$ | $-4V_{in}$ | $C_1$, $C_2$ Discharging |

From table 1 the switching sequence, capacitor charging and discharging and output voltage levels are given in two modes in operational mode 1**:**

$\delta 1 = Vm\ 2bVpp\pi$, $\alpha 1 = Vm\ 1bVpp\pi$,$\delta 2 = Vm\ 2cVpp\pi$, $\alpha 2 = Vm\ 1cVpp\pi$.

In operation mode 2**:**

$\delta 1 = Vm\ 2bVpp\pi$, $\alpha 1 = Vm\ 2cVpp\pi$,$\delta 2 = Vm\ 1bVpp\pi$, $\alpha 2 = Vm\ 1cVpp\pi$.

The relations of output THD and Pulse widths $\alpha 1$, $\alpha 2$, $\delta 1$, $\delta 2$ , four parameters are predefined

$k1 = \alpha 1\delta 1$, $k2 = \alpha 2\delta 2$, $x1 = \pi - \delta 12$, $x2 = \pi - \delta 22$.

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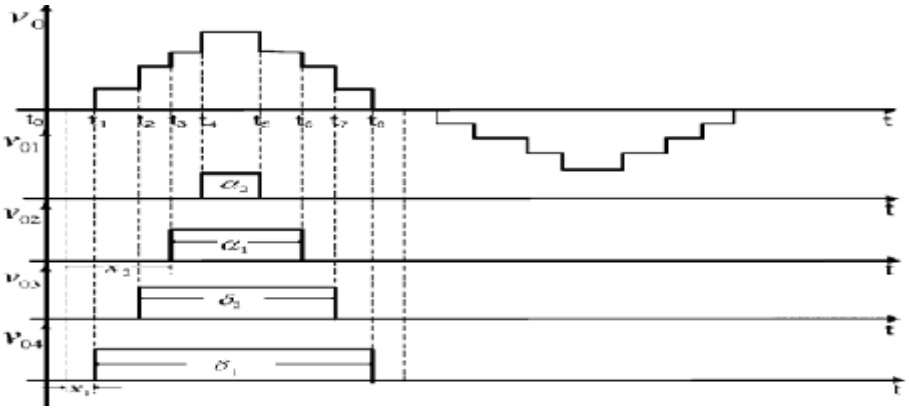

Fig.2 Output voltage decomposition for mode 1.

The output voltage waveforms in fig 2 can be characterized by these four constants. THD of output voltage can be calculated by the harmonic magnitudes THD can be less than 10% within the scope of $0 < x1 < 0.4$ and $0.4 < x2 < 0.6$. Furthermore, THD becomes less along with the increasing number of voltage levels. The output magnitude of multilevel inverter can be regulated by the duration width of voltage levels as well. Two patterns are available to perform the regulations of THD and magnitude simultaneously. One is to regulate $x1$, $x2$ with the fixed $k1$, $k2$ . The other one is to regulate $k1$, $k2$ with the fixed $x1$, $x2$ . The numerical benchmark and THD optimization will be examined in the future study, and a fixed ratio ($k1 = k2 = 0.5$, $x1 = \pi/8$, $x2 = \pi/4$) is adopted to evaluate output harmonics in subsequent simulation.

Table 2: Components Comparison of Proposed Inverter and Cascaded H-Bridge:

| Inverter Type | SC Inverter | Inverter H-Bridge | Cascaded H-Bridge |
|---|---|---|---|
| Switching Device | 2n+8 | 6n | 8n |
| Capacitor | 2n-2 | n | 0 |
| Diode | 4n-6 | n | 0 |
| DC Bus | 2 | n | 2n |
| Power Loss | $(2n-2)loss_{cap}+(4n-6)loss_{diode}$ $+(2n+8)loss_{switch}$ | $n\ loss_{cap}+n\ loss_{diode}+$ $6n\ loss_{switch}$ | $8n\ loss_{switch}$ |

Table 2 gives the comparison of the number of components required to obtain the stepped output voltage with nine levels $4n + 1$ voltage levels. With the same number of voltage levels, the proposed inverter needs less switching devices and inputs than the traditional cascaded H-Bridge.

## III. MULTILEVEL CONVERTER PWM MODULATION STRATEGIES

Pulse width modulation (PWM) strategies used in a conventional inverter can be modified to use in multilevel converters. A symmetrical phase-shift modulation (PSM) is introduced into the proposed multilevel inverter. The symmetrical PSM ensures the output voltage of full bridge is symmetrical to the carrier, so voltage levels can be superimposed symmetrically and carrier frequency is twice as that of the output frequency . The structure of symmetrical PSM is shown in Fig.3.

The logic operations of gate signals are

gate1 = XOR{Q(RS),$Q^1$(D)}

gate2 = XOR{Q(RS),Q(D)}

gate3 = XOR{AND{Q(RS),NOT(PWM)},Q(D)}

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gate4 = XOR{AND{Q(RS),NOT(PWM)},$Q^1$(D)}.

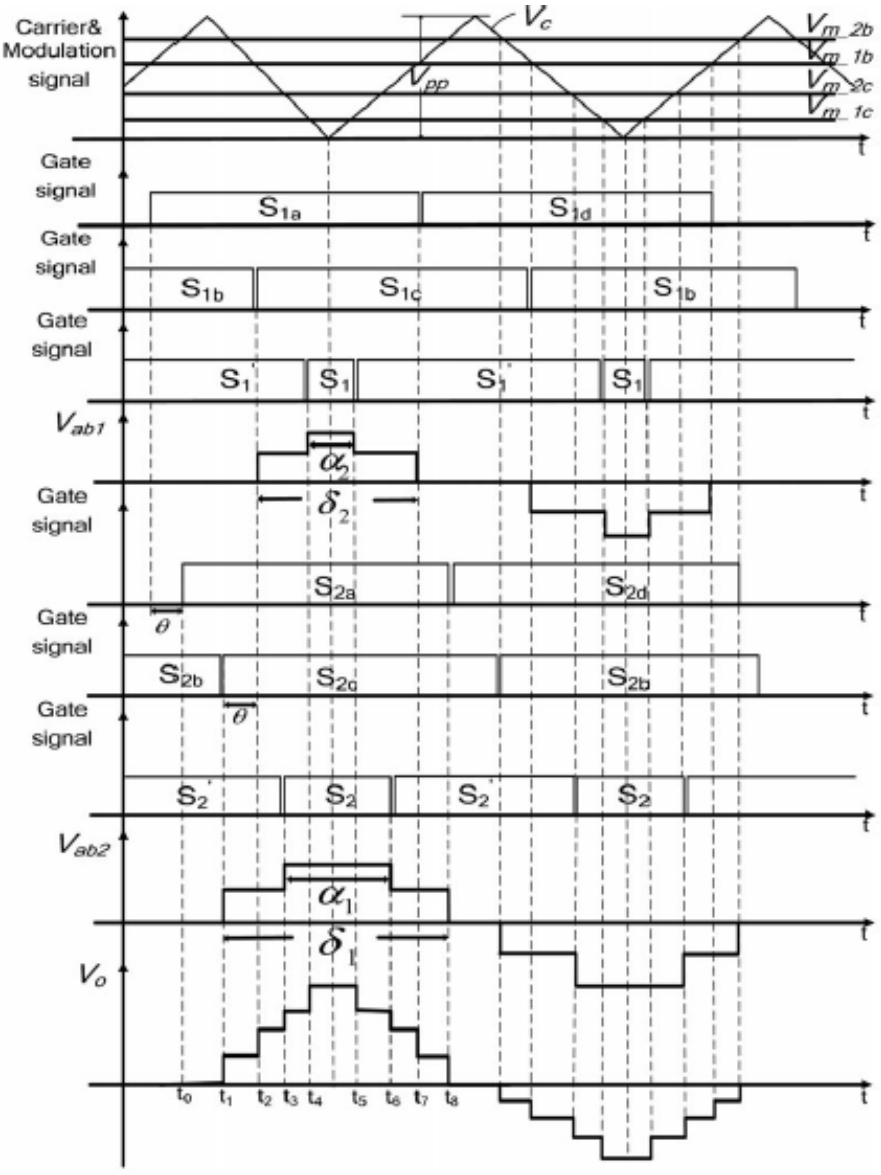


Fig 3 Symmetrical PSM signals with operation mode

Fig. 3 shows waveforms of proposed inverter. Vc is the triangular carrier, and Vpp is the peak value of Vc. The modulation signals of triangular carrier are Vm_1c, Vm _1b, Vm _2c and Vm _2b. Vm _1b and Vm _2b are used to control phase-shift angles of H-Bridge 1 and H-Bridge 2, respectively, and δi is the duration of voltage levels controlled by them. Vm_1c and Vm_2c are used to control the alternative operations of SC1 and SC2, respectively, and αi is the duration of voltage levels controlled by them. Thus, the drive signals of H-Bridge switches
(S1a, S1b, S1c, S1d, S2a, S2b, S2c, S2d) are phase-shifted pulse signals, while the drive signals of SC switches (S1, S2, $S1^1$, $S2^1$ ) are complementary pulse signals.

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## IV. SIMULATION AND RESULTS

The Simulink model is developed for sc-cascaded inverter with nine-level is developed which shows inverter output voltage ,because of increased level of output voltage harmonic content is reduced.

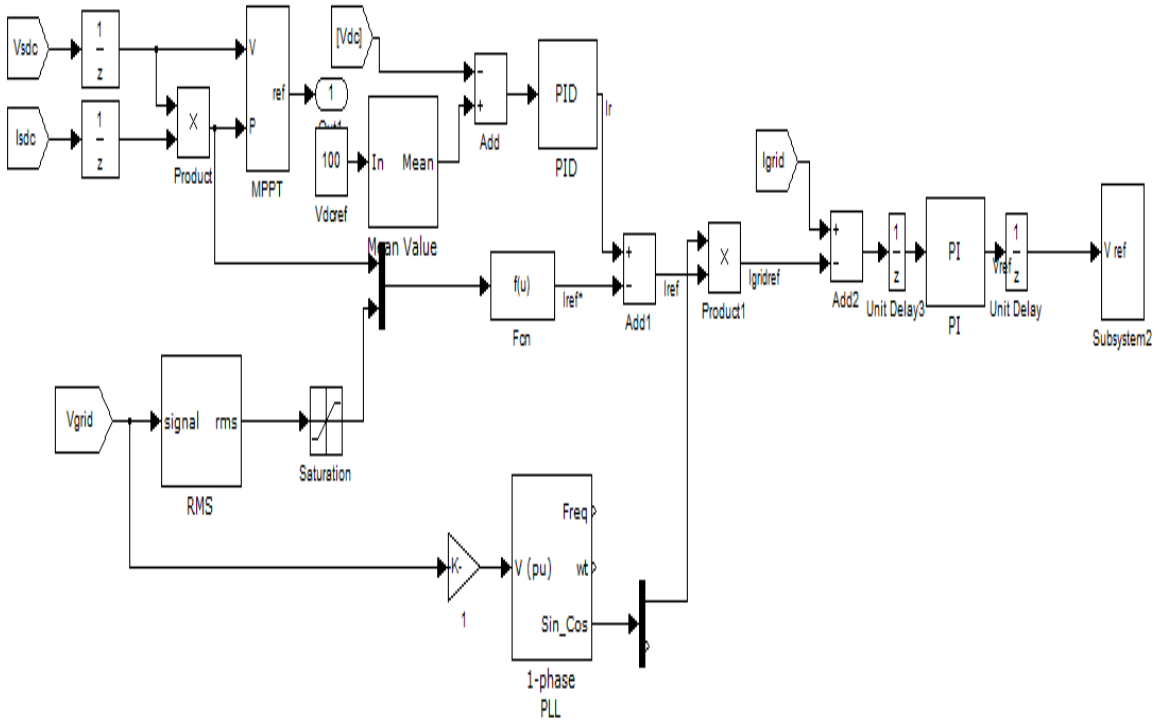


Fig 4 Simulink model of modulation circuit

The simulink model of fig 4 gives the gate drive signals for the switching devices to conduct and obtain the modulation of the system by using controllers.

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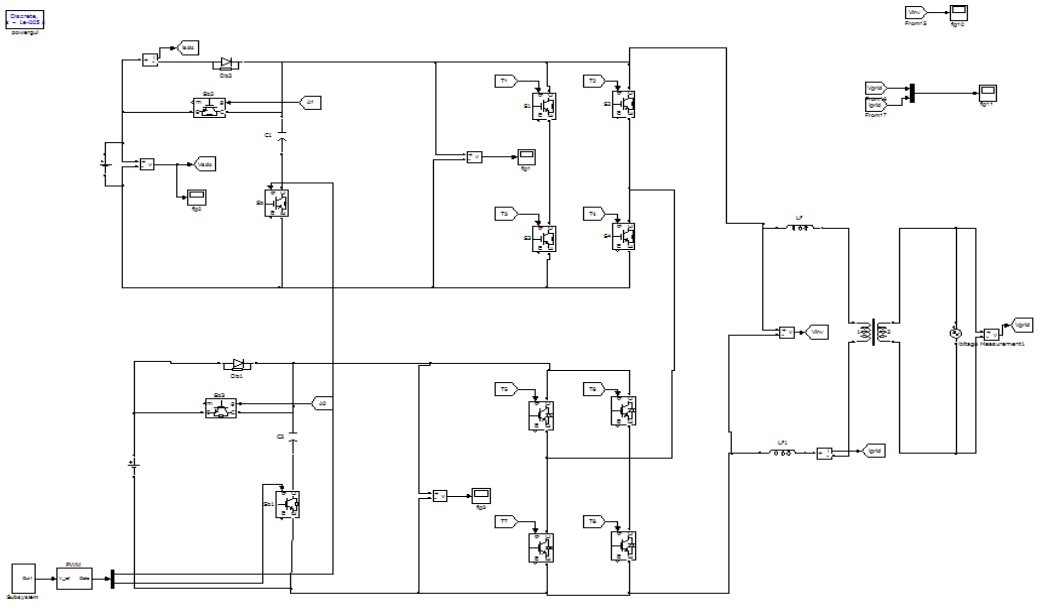

Fig 5 Simulink model of sc-cascaded inverter with nine-level

The Simulink model of fig 5 the proposed system with sc-cascaded inverter is developed by considering the frequency of the fundamental as 50 hz.

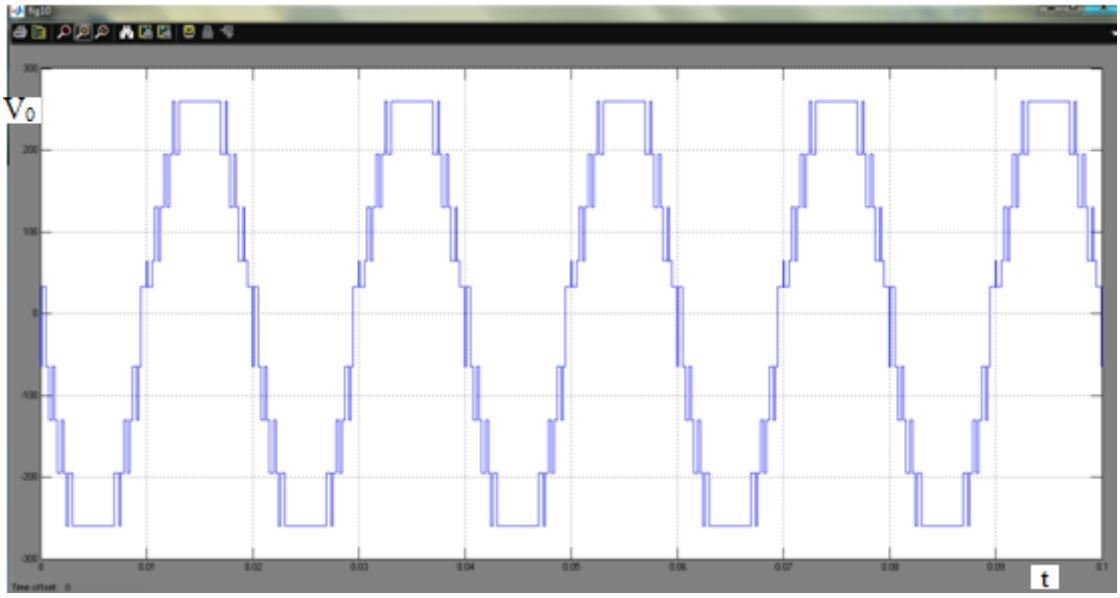


Fig 6 sc-cascaded nine level inverter output voltage waveform

The output voltage waveform shown in fig 6 shows the output voltage in stepped waveform with nine-levels. The magnitude of lower order harmonics is reduced there by increasing the magnitude of higher order harmonics which is easily filtered by external load circuit .The output voltage waveform is nearly sinusoidal by which total harmonic distortion is reduced.

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## V.CONCLUSION

In this paper, a SC-based cascaded multilevel inverter with nine-level circuit topology is examined in depth. Compared with conventional cascaded multilevel inverter, the proposed inverter can greatly decrease the number of switching devices. A single carrier modulation named by symmetrical PSM, was presented with the low switching frequency and simple implementation. The result of simulation gives the feasibility of proposed circuit and modulation method. Comparing with traditional cascade H-bridge, the number of voltage levels can be further increased by SC frontend. The number of voltage levels increases twice in half cycle of 9-level circuit. With the exponential increase in the number of voltage levels, the harmonics are significantly cut down in staircase output, which is particularly remarkable due to simple and flexible circuit topology. Meanwhile, the magnitude control can be accomplished by pulse width regulation of voltage level, so the proposed multilevel inverter can serve as HF power source with controlled magnitude and reduced harmonics. The proposed inverter can be applied to grid-connected photovoltaic system and electrical network of Electric vehicles, because the multiple dc sources are available easily from solar panel, batteries, Ultra capacitors, and fuel cells.

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