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Development of Small Signal Amplifier using BJT-JFET Hybrid Unit in Sziklai Pair Topology

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ABSTRACT: As a novel approach, BJT-JFET hybrid unit in Sziklai pair topology is used to design small-signal amplifier. Proposed amplifier, which can be tuned in 108Hz-505KHz frequency range, may amplify audio range signal excursions swinging in 0.1-12mV range at 1KHz. High voltage gain (105.552), current gain greater than unity (1.5574), wider bandwidth (505.356KHz) and low order harmonic distortion (0.89%) makes this amplifier superior than small-signal PNP Sziklai pair amplifier, announced by the author in 2012. Addition of biasing resistance R_A in the circuit is essential to maintain amplification property. The investigation deals with qualitative analysis, small signal analysis, temperature dependency and tuning performance of the proposed circuit. Proposed amplifier design may be suitably used in cascade stages of Radio-TV receivers and 108Hz-505KHz frequency range power sources whereas the hybrid device may be tested for designing power supplies, power amplifiers, general purpose high current switches and other linear applications.

KEYWORDS: Small-signal amplifiers, Sziklai pair, Circuit simulation, Circuit analysis.

I.INTRODUCTION

Similar to Darlington pairs, Sziklai pairs are also one of the frequently used devices for designing push-pull power amplifiers but converse is not true for the small signal amplifier designs [1]-[2]. Small signal amplifiers with Sziklai pairs are still under the developmental phase. Despite of having dissimilar configuration, both the paired units compete with each other in many applications due to almost identical range of current gain, input resistance, output resistance and voltage gain [1]-[3]. This becomes more relevant in case of amplifiers using paired unit transistors with $\beta>100$. The current gain factor β of Sziklai pair ($\beta_1\beta_2+\beta_1$) is slightly less than Darlington pair ($\beta_1\beta_2+\beta_1+\beta_2$) due to small amount of in-built negative feedback, but for $\beta>100$ both are approximated as $\beta\approx\beta_1\beta_2$ [1]-[3]. However, Sziklai pair holds better linearity (less distortion, if used in audio range amplifiers) with half base-turn-on voltage than Darlington pair [1]-[3].

Present investigation is focused around the development and analysis of a small signal amplifier that uses a hybrid unit of PNP transistor (driver) and N-channel JFET in Sziklai pair topology.

II. CIRCUIT DETAILS

Proposed small-signal amplifier (Fig.1) uses a PNP driver transistor (Q2N2907A with $\beta=231.7$) and N Channel JFET (J2N4393 with $V_T=-1.422$) at follower position in Sziklai pair topology [1]. Required DC biasing is established with an additional biasing resistance R_A and other suitable passive biasing components using RC coupled potential divider biasing methodology [3]. PSpice simulation is done to carry present investigations [4]. AC input signal source of 1V, 1KHz is used to feed the circuit. Observations are listed for 1mV, 1KHz input signal but the proposed amplifier produces useful results for 0.1-12mV range AC input at 1KHz.

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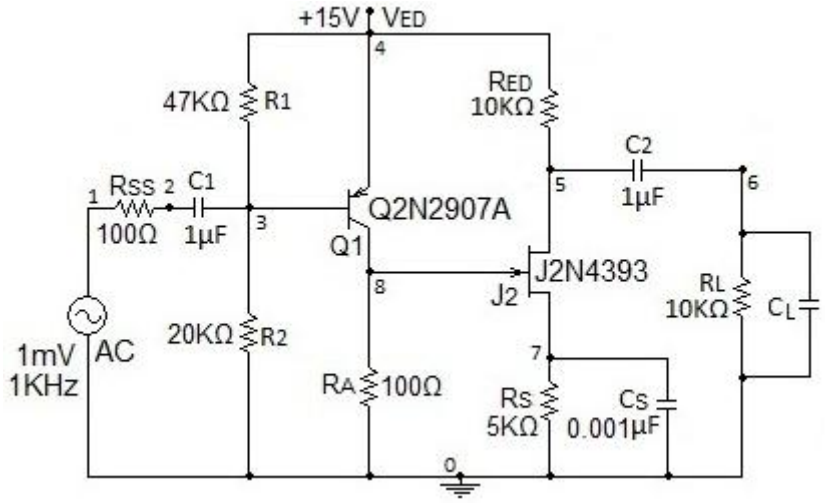

Fig.1. Proposed amplifier with BJT-JFET hybrid unit in Sziklai pair topology

III. RESULTS AND DISCUSSIONS

A. Qualitative Analysis

TABLE-I depicts the observed values of various performance parameters of the proposed circuit. It also describes a quick qualitative comparison of proposed circuit with small signal PNP Sziklai pair amplifier [3].

TABLE-I: Performance parameters at room temperature 27°C

Performance Parameters	PNP Sziklai pair amplifier	Proposed amplifier
Maximum voltage gain (A_{VG})	102.309	105.552
Maximum current gain (A_{IG})	7.345	1.5574
Band width (B_W)	4.80KHz	505.247KHz
Lower cut-off frequency (f_L)	224.453Hz	108.177Hz
Higher cut-off frequency (f_H)	5.0556 KHz	505.356KHz
Peak output voltage (V_{RL})	1.106V	106.956mV
Input signal used for present observations at 1KHz (V_I)	10mV	1mV
Input signal range for faithful amplification at 1KHz	10mV - 30mV	0.1mV - 12mV
Peak output current (I_{RL})	109.434 µA	11.162 µA
Input current across R_{SS}	13.574 µA	6.06 µA
Output phase difference θ°	180°	180°
Total harmonic distortion (THD)	1.72%	0.89%

Proposed circuit holds enhanced voltage gain, wider bandwidth, reduced THD and suppressed current gain than small signal Darlington pair and PNP Sziklai pair amplifier [3]. Inclusion of biasing resistance R_A in the proposed circuit design is essential to retain the observed performance. Absense of R_A causes voltage and current gains of the amplifier to dip below unity at any baising combination. Moreover, the permissible range of R_A to obtain faithful response is $37\Omega<R_A<100\Omega$. In addition, the circuit is found free from poor-response-problem of small-signal Darlington's amplifier [5] at higher frequencies and narrow bandwidth restrictions of PNP driven Sziklai pair amplifier [3].

Proposed amplifier circuit shows considerable response for variations in biasing resistances and DC biasing supply. Refer input biasing resistance R_{SS}. Voltage gain A_{VG} of the amplifier receives its maximum (270.621) at $R_{SS}=10\Omega$ and minimum (1.55) at $R_{SS}=10K\Omega$ with a faithful amplification in $10\Omega<R_{SS}<10K\Omega$ range. Similarly, A_{VG} rises almost linearly with increasing values of drain-emitter resistance R_{ED} up to 20KΩ and beyond this critical limit it gradually acquires a saturation tendency. However, A_{VG} increases non-linearly with source resistance R_S, reaches maximum

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(A_{VG}=106.021) at R_S=10KΩ, thereafter starts decreasing but the amplifier shows purposeful response in 100Ω <R_S<75KΩ range.

Moreover, the hybrid unit of BJT-JFET in Sziklai pair topology unit switches-ON at 3V. A 3-30V range of V_{CC} is observed for the faithful response of the circuit. Correspondingly, A_{VG} rises almost exponentially with increasing values of V_{CC} up to a critical limit of 15V and thereafter falls almost linearly.

Qualitative features suggest the possible use of the proposed circuit in designing cascadable gain blocks for receivers and 108Hz-505KHz frequency range power sources (with A_{VG} and A_{IG} both are greater than unity). However, the hybrid device used in the proposed circuit design may also be tested in power supplies, power amplifiers, general purpose high current switches and other linear applications.

B. Small Signal AC Analysis

Small-signal AC equivalent circuit of proposed amplifier is drawn in Fig.2

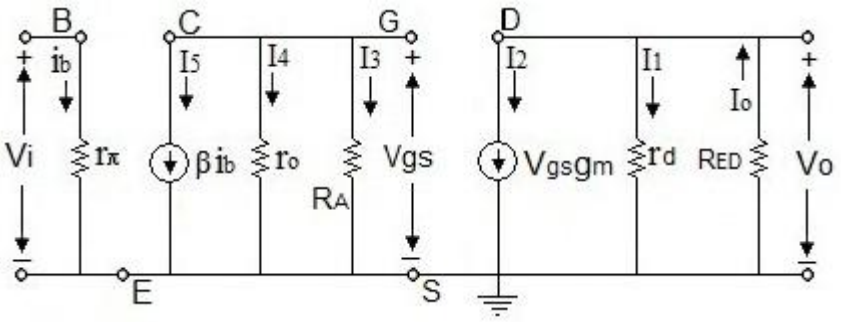

Fig.2. Small-signal AC equivalent of the Proposed amplifier

Based on simulation results, BJT of the Sziklai unit consists base-emitter resistance r_π=37.7Ω, collector-emitter resistance r_o=825Ω, AC current gain factor β=184 whereas JFET consists g_m=1.33x10^{-4}mho, drain-source resistance r_d=0.30x10^{3}Ω. Also, I_b is the base current of BJT and R_B=R_1||R_2. Small-signal AC voltage gain of the proposed amplifier (Fig.2) is deduced as –

$$A_V = \frac{-\beta g_m}{r_\pi\left(\frac{1}{R_{ED}}+\frac{1}{r_d}\right)\left(\frac{1}{R_A}+\frac{1}{r_o}\right)} \approx \frac{-\beta g_m R_A}{r_\pi\left(\frac{1}{R_{ED}}+\frac{1}{r_d}\right)}$$

However, small-signal AC current gain can be deduced as-

$$A_I = \frac{-\beta g_m}{R_{ED} r_\pi\left(\frac{1}{R_B}+\frac{1}{r_\pi}\right)\left(\frac{1}{R_{ED}}+\frac{1}{r_d}\right)\left(\frac{1}{R_A}+\frac{1}{r_o}\right)} \approx \frac{-\beta g_m R_A}{\left(1+\frac{R_{ED}}{r_d}\right)}$$

Negative sign in respective expressions shows the reversal of phase in output waveforms [5]. Equations also verfies the strong dependency of AC voltage and current gains (A_V and A_I) on the additional biasing resistance R_A.

C. Temperature Analysis

Both A_{VG} and A_{IG} simultaneously go high but bandwidth goes down with rising temperature up to a critical temperature limit 38°C. Values of various parameters at –30°C are reported to be- A_{VG}=89.64, A_{IG}=1.26, B_W= 812.11KHz, THD=0.905%, β_{ac}=145 r_π=30.7Ω, r_o=1.11KΩ, g_m=1.76x10^{-4} and r_d=105.34Ω whereas at critical temperature 38°C these are observed to be A_{VG}=108.08, A_{IG}=1.60, B_W=358.17KHz, THD=0.855%, β_{ac}=191 r_π=39Ω, r_o=0.785KΩ, g_m=1.26x10^{-4} and r_d=472.80Ω. However beyond critical temperature both variety of gains gradually fall and make the amplifier purposeless after 45°C.

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Refer temperature dependency of the proposed circuit. Rising temperature affects h_{fe} of the transistor in proposed design in a usual way [3] whereas it accelerates the majority carrier generation in semiconductor channel of JFET up to a critical temperature limit. This causes simultaneous enhancement in A_{VG} and A_{IG}. Beyond critical temperature, rate of collision of majority carriers with the ions in semiconductor channel enhances and affect their mobility [6]. This decreases the drain current of the JFET based Sziklai pair system and therefore the effective voltage and current gain of the proposed amplifier.

D. Noise Analysis

Both Input and output noises for the proposed circuit are found considerably low and within the permissible range for small-signal amplifiers [4]. Output noise (approx range 10^{-7} V/Hz) is observed to be higher than input noise (approx range 10^{-9} V/Hz) at various operating frequencies between 100Hz to 1MHz. Moreover, the output noise significantly reduces at elevated temperatures (e.g. 20^{o}C rise in temperature forces output noise to reduce from approximately 10^{-7} V/Hz to 10^{-8} V/Hz range).

E. Tuning Performance

Voltage gain A_{VG} and bandwidth B_W of the proposed amplifier remains almost unaltered whereas A_{IG} shows a slow pace rising tendency in the permissible range of coupling capacitors C_1 (500nF< C_1<500μF) and C_2 (22nF< C_2<10μF). However, proposed amplifier shows significant variations in upper-cut-off frequency f_H for different values of source capacitor C_S and load capacitor C_L in a variation range of 22nF–0.0001μF whereas A_{VG}, A_{IG} and lower-cut-off frequency f_L remains almost unaltered. Thus the bandwidth B_W varies with C_S between 622.41KHz (at C_S=.0001uF) to 69.50KHz (at C_S=22nF) whereas it varies with C_L from 490.035KHz (at C_L=0.0001μF) to 51.14KHz (at C_L=22nF). Variations in C_S and C_L control only to the upper cut-off-frequency f_H of the amplifier. Thus, the proper adjustment of C_S and C_L may be used to tune the proposed amplifier at a desired frequency in the permissible response range [7].

IV. CONCLUSIONS

A small signal amplifier using hybrid unit of PNP transistor (driver) and N-channel JFET in Sziklai pair topology is proposed and analyzed for the first time in present investigation. Proposed circuit holds enhanced voltage gain, wider bandwidth, reduced THD and suppressed current gain than small signal Darlington pair and PNP Sziklai pair amplifiers. The proposed circuit design is found free from poor-response-problem of small-signal Darlington's amplifier at higher frequencies and narrow bandwidth restrictions of PNP driven Sziklai pair amplifier. Biasing resistance R_A in the proposed design is to be essentially present for reported performance. Proper adjustment of C_S and C_L may provide facility to tune the proposed amplifier at a desired frequency in the permissible response range.

Qualitative analysis of proposed amplifier circuit suggests possibility of using the circuit in designing cascadable gain blocks for receivers and 108Hz-505KHz frequency range power sources. However, hybrid device used in the proposed circuit design may also be tested in power supplies, power amplifiers, general purpose high current switches and other linear applications.

V. ACKNOWLEDGMENT

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BIOGRAPHY

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