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Review on Low Voltage Current Conveyor

Kaushani H.Shah[1], Bhoomi P.Patel[2], Mohammed G. Vayada[3]

PG Student [VLSI], Dept. of ECE, Silver Oak Engineering College, Ahmedabad, Gujarat, India[1]

PG Student [VLSI], Dept. of ECE, Silver Oak Engineering College, Ahmedabad, Gujarat, India[2]

Assistant Professor, Dept. of ECE, Silver Oak Engineering College, Ahmedabad, Gujarat, India[3]

ABSTRACT:Now a day current mode circuits have been receiving significant attention in analog signal processing. For high frequency current mode applications is a current conveyor. In many cases the conveyor-based implementation offers improved performance to the voltage op-amp-based implementation in terms of accuracy, bandwidth and convenience.Current mode circuits do not have the limitation of dynamic range. Various topologies are used to implement current conveyor circuit. In this paper two topologies are used which are current mirror based topology and differential pair based topology. Major applications are available based on current conveyor which are capacitance multiplier, negative impedance conveyor and V to I converters. This paper gives the comparison of both topologies in terms of gain, bandwidth, linearity, power consumption. In the end results of different simulations are compared to conclude that differential pair based topology gives better results.

KEYWORDS: Bandwidth, CCII, CMOS, Current Conveyor, Gain, Linearity, VLSI.

I. INTRODUCTION

The current conveyor is a three terminal device performing many useful analog signal processing functions when the device is connected with other electronic elements in specific circuit configurations. The current conveyor has evolved from first generation to third generation. the first generation current conveyor (CCI) was proposed by Smith and Sedra in 1968 [1] and the more versatile second generation current conveyor (CCII) was introduced by the same authors in 1970 [2] as an extension of their first generation conveyor.

There has been substantial emphasis on the development of current mode signal processing circuits such as filters and oscillators. This is due to increased bandwidth, simple circuitry, better linearity, dynamic range performances and lower power consumption as compared to their voltage mode circuitry. A variety of current mode building blocks are developed with current mode circuits. The current conveyor (CCII) is one among such blocks which has received significant attention. It is hybrid block and has basic construction containing a voltage follower (VF) interconnected with either current mirror or current follower. Two topologies of the current conveyor are used. The first is based on current mirror and the second is based on differential pair.

II.LITERATURE REVIEW

(1) This paper gives the comparison between two topologies. The first method is inverter based current conveyor and the second method is current mirror based current conveyor. Second generation current conveyor is used for both the methods. Table gives the comparison of both topologies. [5]

Table 1: comparison of Topologies

Sr No.	Parameters	Inverter based CCII	Current mirror based CCII
1	Bandwidth	Twice than Translinear loop based CCII+	Half of the Inverter based CCII+
2	Third Harmonic Distortion	Less	More
3	Output Noise	Less than Inverter based CCII+	More than Inverter based CCII+
4	Area of silicon required	Half	Twice
5	Synthesized by	Analog and Digital	Only Analog

Even through inverter base topology performs better for certain performance measure, it may fail at input voltage dynamic range. The input voltage dynamic range for the CMOS inverter for using in linear application is very narrow; this may lead very small dynamic range. Current mirror based topology has very high input voltage dynamic range.

(2)This paper is based on the second method which is differential pair based CCII. This paper represents that NMOS differential pair is works, when voltage is greater than 2_{vdsat} and PMOS differential pair is works, when voltage is less than 2_{vdsat}. So using both type of MOSFET, increase in voltage dynamic range is possible. If CCII use only NMOS pair then necessary voltage required is 2_{vdat} to run the circuit. If CCII use only PMOS pair then necessary voltage required, which is less than 2_{vdat} to run the circuit.In this paper, a new circuit is proposed low-voltage low power CMOS rail-to-rail second generation current conveyor. [3]

Drawback: No of transistors increases so power consumption is increases.Power consumption are not compared, however the power consumption for the proposed design seems to be higher because there are two differential pairs and thus requirement of two separate current sources.

III.CIRCUIT DISCRIPTION

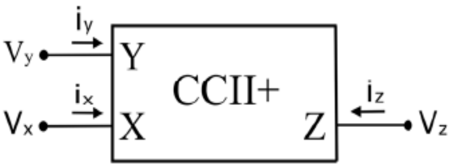

Fig1: Basic CCII+ current conveyor voltages and currents

If a voltage is applied to terminal Y, an equipotential will appear on the input terminal X. An input current I being forced into terminal X will result an equal amount of current flowing into terminal Y. The current I will be conveyed to output terminal such that terminal Z has the characteristics of a current source, of value I with high output impedance. Potential of X being set by that of Y, is independent of the current being forced into port X. Current through port Y being fixed by X is independent of the voltage applied to Y. Terminal Y exhibits an infinite input Impedance.

It is a three port device. Three terminals X, Y, Z are used to satisfy all the conditions which CCII needed. Fig2 shows the all conditions which are required for CCII.

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix}$$

Fig 2: Matrix Representation of CCII

$$\boldsymbol{Vx = Vy,}$$

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$$Iy = 0,$$
$$Iz = Ix$$

IV.CURRENT MIRROR BASED TOPOLOGY

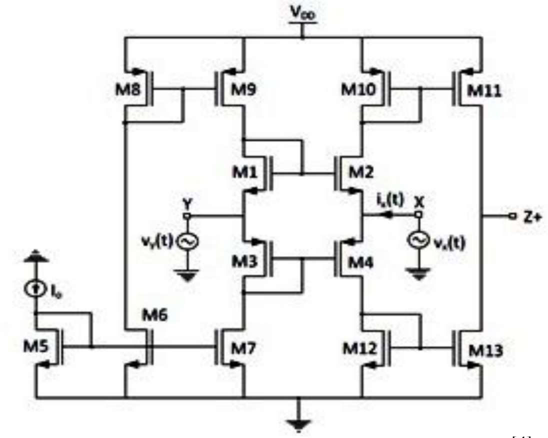

Fig 3: Current mirror based current conveyor [4]

CCII has a mixed translinear loop comprised of two PNP and two NPN transistors. For the positive CCII circuit illustrated in Fig. 3, transistors M1–M4 form the input translinear mixed loop. The current relationship in the loop is characterized by $I1I3 = I2I4$. The circuit is dc biased by $I0$, which is proportional to the current flowing through transistor M1 and M3 ($Io \approx I1 = I3$). When no load is connected to terminal X, the terminal can be considered as low impedance output port. The input port Y is considered to be the high impedance node.

V. DIFFERENTIAL PAIR BASED TOPOLOGY

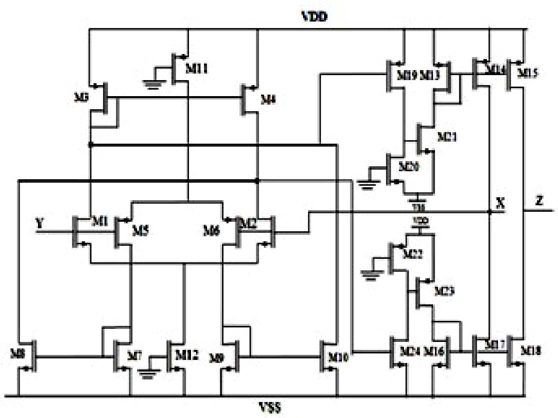

Fig 4: Differential pair based current conveyor [3]

In the input stage, we assembled a NMOS differential pair in parallel with a PMOS differential pair to get a good tracking throughout the supply area. We also duplicated the output stage to minimize the parasitic resistor at X. The operation of this stage can be divided into three regions shown in fig. l. In the positive rail region, only NMOS pair is active. In the mid-rail region both NMOS and PMOS are active, however in the negative rail region only PMOS pair is active.

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The input stage is the important part of second generation current conveyor (CCII) to obtain a large dynamic range. This can be achieved by using N-MOS matched differential pair (MI, M2) and another P-MOS matched differential pair (M5, M6) connected parallel to implement the voltage follower between the X and Y terminals. Transistors (M22, M12) provide the necessary biasing currents for each differential pair separately.

VI. SIMULATION RESULTS

1. NGSPICE Simulation Results of Current Mirror Based Topology

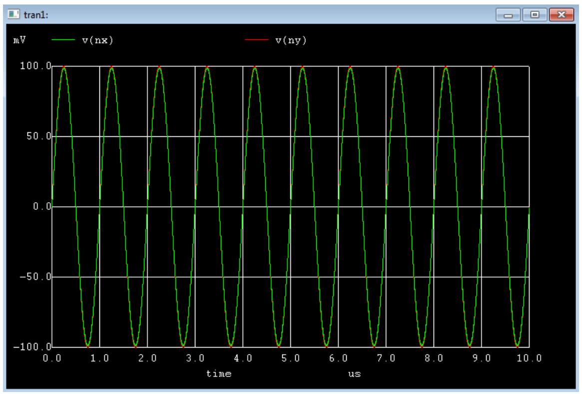

Fig 5: Variation of output voltage as a function of input voltage

Fig 5 shows the relation between the input voltage and output voltage. As per CCII matrix we need Vx=Vy that is satisfied in this graph.

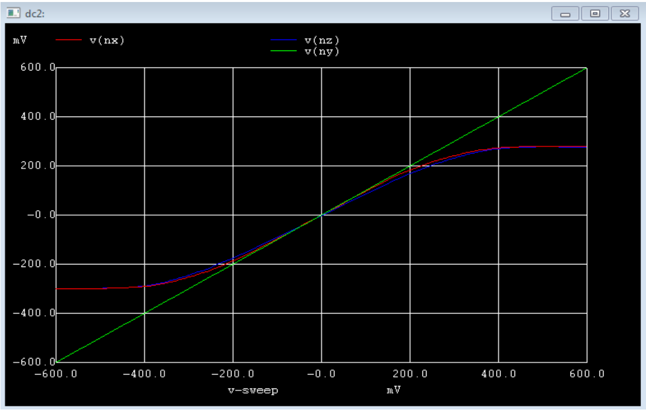

Fig 6: Dynamic Range Representation of Voltage

Fig 6 shows dynamic representation of voltage in which gives the vdd to -0.6V to +0.6V but get linear response between -0.2V to +0.2V. Current mirror based topology has a problem of nonlinearity; it will overcome in the second method differential pair base topology.

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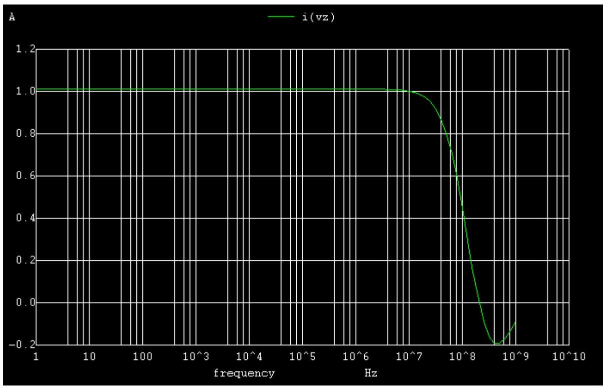

Fig 7: Current gain according to the frequency

Fig 7 represents the gain of current which will not reduce if we increasebandwidth because current mode circuits do not have the limitation of gain bandwidth product (UGB).

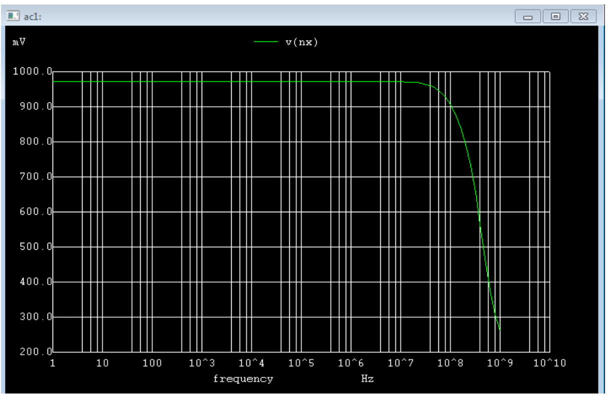

Fig 8: Voltage gain according to the frequency

Fig 8 shows the bandwidth of voltage. Current mirror based topology has large voltage bandwidth than differential pair based topology

2. Simulation results of Differential Pair Based Topology

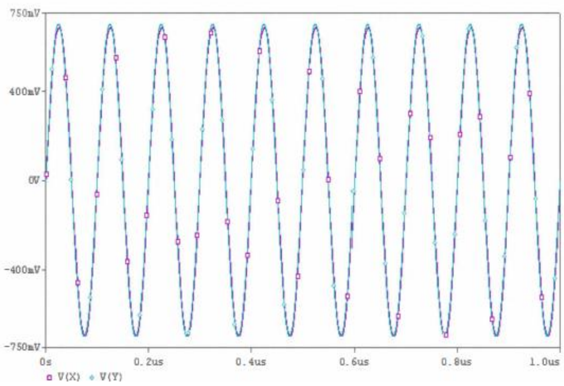

Fig 9: Variation of output voltage as a function of input voltage [4]

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Fig 9 shows the relation between the input voltage and output voltage. As per CCII matrix we need Vx=Vy that is satisfied in this graph. This graph is better than Fig 5.

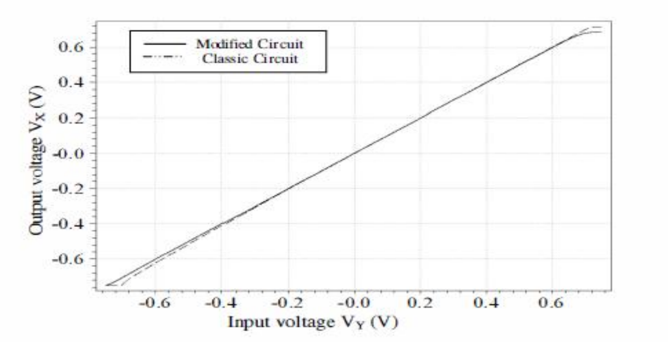

Fig 10: Voltage gain according to the frequency [3]

Fig 10 shows dynamic representation of voltage in which gives the vdd to -0.6V to +0.6V but get linear response between -0.5V to +0.5V.the problem of non-linearity is overcome using differential pair based topology.

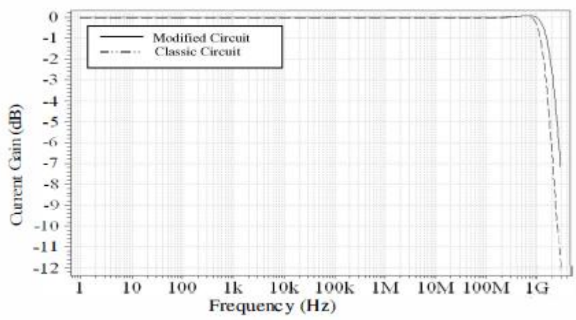

Fig 11: Current gain according to the frequency [3]

Fig 11 represents the gain of current which will not reduce if we increase bandwidth because current mode circuits do not have the limitation of gain bandwidth product (UGB).This topology has higher gain than current mirror based topology.

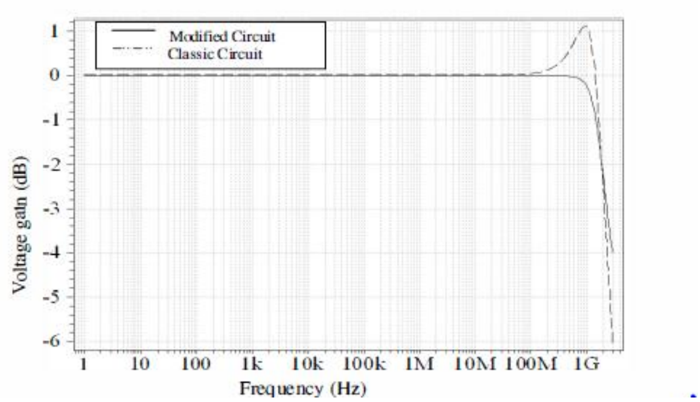

Fig 12: Variation of output voltage as a function of input voltage [3]

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Fig 12 shows the bandwidth of voltage. Current mirror based topology has large voltage bandwidth than differential pair based topology.

VII.CONCLUSION

The effect of CCII topologies performance is evaluated on the basis of gain, bandwidth and linear characteristics. Bandwidth response for voltage transfer is found to be higher in current mirror based topology than differential pair based topology. But in case of linearity and dynamic range differential pair based topology gives better performance than current mirror based topology. Simulations results are compared for both topologies.

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