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Low Power and High Speed 4-Bit Flash Analog to Digital Converter Using Dynamic Latch Comparator Technique

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ABSTRACT: As VLSI technology gaining more popular power consumption and high speed are the major constraints. In Mixed signal IC's it is a necessity of minimum power dissipation in order to limit energy in a reasonable size batteries. Analog to digital converter is the key to mixed signal IC's. Analog to digital converters are the basic component in modern communications, handheld wireless computers and signal processing systems. In this paper most preferred and high speed flash ADC using CMOS latch comparator is presented. Normally Flash Adc takes large number of comparators as size of ADC increases. In this comparator count will be decreased by using multiplexing of reference signal and reduce power dissipation using dynamic latch comparator. This design is simulated and results are presented. The presented flash ADC consumes 212.47uwatts power at a frequency of 1000 MHz with an operating voltage of 1.8v.

KEYWORDS: Analog to digital converter (ADC), Flash ADC, Dynamic latch comparator, Power dissipation.

I.INTRODUCTION

With the technology development the devices requires more accuracy, high speed and low power consumption. World is moving faster by means of wireless media and high speed communication that ultimately increases the use of high frequency analog signals. Generally high speed processing is done by using processors, digital computers, etc. In the real world signals are analog in nature for example video, sound, light. To get digital signal from this we use analog to digital converter for converting analog type of signal to digital nature. If we need to get back analog signal digital to analog converter is required. Analog to digital converters plays a major role in many modern systems to link analog signals with digital systems. Digital system applications can be range from audio to communication applications and to medical applications. These analog to digital converters are implemented using different types of architectures, sizes and speeds. The demand of the comparators are mostly depends on area, speed, and power of the converters.

At present, there are so many types of ADCs with different architectures, sampling rates, resolutions, power consumption. These ADCs are useful in mobile communication devices and measure equipment. Since the performance of ADC including sampling rate, resolution and power consumption may vary based on its architecture, one single ADC cannot cover all the applications which are needed. Therefore, it is important to select proper ADC for particular application.

In this most popular and high speed flash ADC is designed with an operating voltage of 1.8v. In designing ADC comparators are one of the important components. This comparator was designed using a dynamic latch comparator with CMOS technology in order to getting low power dissipation. Here, the flash ADC with minimum number of comparators is designed to decrease power consumption. The minimization of comparators can be achieved by multiplexing of reference signals with different scaling.

II. THEORY OF ADC

Analog to digital converters (ADCs) are used to convert analog type of signals into digital form of those signals. In modern time based on applications ADCs are available in different forms. ADCs are defined mainly in three categories depending on their high speed of operation. The three types of ADCs are a high speed ADC, medium speed ADC and

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low speed ADC. ADC has a different type of architectures in which first one is Pipeline ADC. Its operating speed is high as compared to flash it is slow and medium resolution. Second architecture is SAR ADC. It is more suitable for medium to high resolution and low power applications with moderate speed. Third type of architecture is Sigma-delta ADC. It is used in low speed and high resolution applications. Forth Type of ADC architecture is Flash ADC. It is operating at high speed and low resolution. So we conclude that flash ADC is the fastest ADC among all other types of ADC architectures. So the flash ADC is the best option for high speed low resolution applications. The important features that are available in flash ADC includes different diagrams, sampling rates, resolutions, power consumptions and a range operating temperature. Because of flash ADC with parallel design, It easily converts on e cycle with many comparators. This flash ADC converts analog to digital are so fast in case of analog to digital type of signal conversion. The flash ADC is designed to reduce power consumption that means it provide better output signals but require a less amount of power. Now a day's flash ADC with CMOS technology is also available. The flash ADC is widely used in digital oscilloscopes, high speed instrumentation, radar, high data rate links and optical communications. As flash ADCs are operating in a method of parallel conversion, maximum operating frequency in the range of gigahertz is possible.

III.TYPES OF COMPARATORS

After operational amplifiers Comparators are the one of the most popular and widely used electronic components in the world. Comparators are also called as 1-bit analog to digital converter and for that reason they are mostly used in analog to digital converter. The comparator is a circuit that compares an analog voltage with the reference voltage and gives the binary signal output based on comparison. In the analog to digital conversion process, first it is need to sample the input signal. After that the sampled signal is given to a combination of comparators in order to get binary equivalent of the analog input signal. Comparators are found in many other applications like pear detector, switching power regulators, zero-crossing detectors, and data transmission. CMOS comparator is used to find out whether a signal is greater than or smaller than zero or to compare analog input signal with a reference signal and gives a binary signal output based on comparison. Basically comparators are classified into two types they are Amplifier chain type and Latch type comparators. Amplifier chain type comparators generates digital signal output through a set of cascode amplifier stages in response of small difference between input analog signal and reference signal. It is better to use high gain stages as compared to low gain stages. Latch type comparators are most popular for design ADCs. It offers high speed, low static power consumption and more flexible power management.

IV.DYNAMIC LATCH COMPARATOR

CMOS technology based dynamic latch comparators are suitable for designing a analog to digital converters with high speed, low power dissipation and immune to noise. Basically dynamic latch comparator will operates in two modes, they are Active mode and Standby mode or precharge mode. The schematic diagram for dynamic latch comparator is shown in fig.1. When the Lth signal is low then the comparator will works under Standby mode and when it is high then it works in Active mode. In the active mode of operation both NMOS and PMOS logic are connected with Mth transistors are in operation mode. In this mode based on Lth signal the input signal is sampled and compares the input signal with the reference signal. In this circuit we have two paths to discharging those are M3 to ground and M4 to ground. In the case of standby mode Lth signal is low and the both NMOS logic and PMOS logic are separated each other and during this stage it is in hold mode and will gives the output. Since, due to cross coupled connection comparator stage gives the positive output on one side and negative output on other side. But, here consider positive output for simplicity. To get stabilized output use inverter buffers at the output of comparator. In this mode of operation only upper half of the comparator is worked and resulting in the reduction of power.

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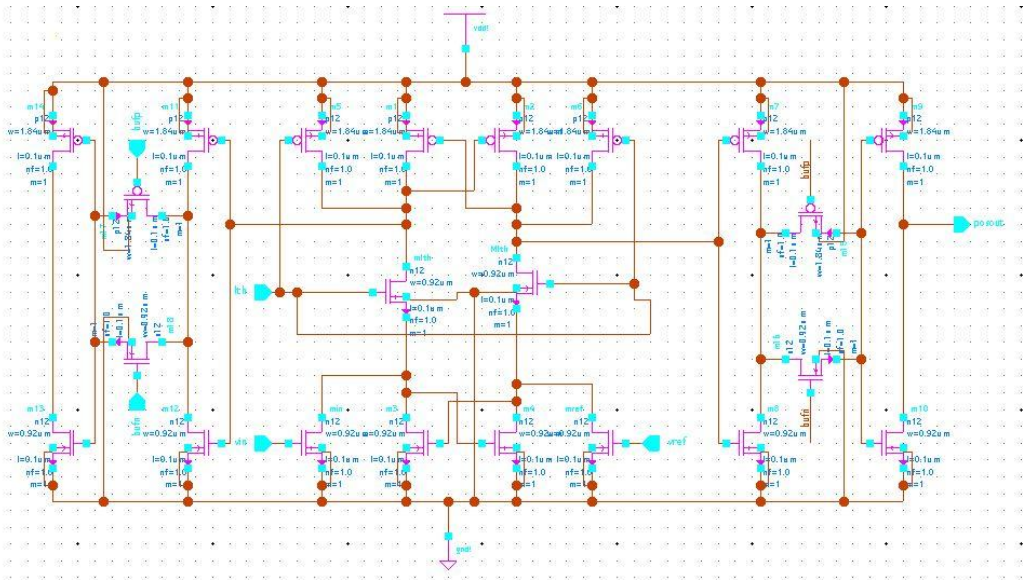

Fig. 1. Schematic diagram for Dynamic latch comparator

V.FLASH ADC STRUCTURE

Flash ADC's are also known as parallel ADC's. Due to the parallel architecture it has high speed conversion compared to other types and is used for high bandwidth applications. As presence of 2^N resistor it dissipates lot of power, has low resolution, and needs a large number of comparators for high resolution. In high frequency applications it is more useful. It has few applications those are high-density disk drivers and satellite communication. A typical flash ADC structure is shown in fig.2.

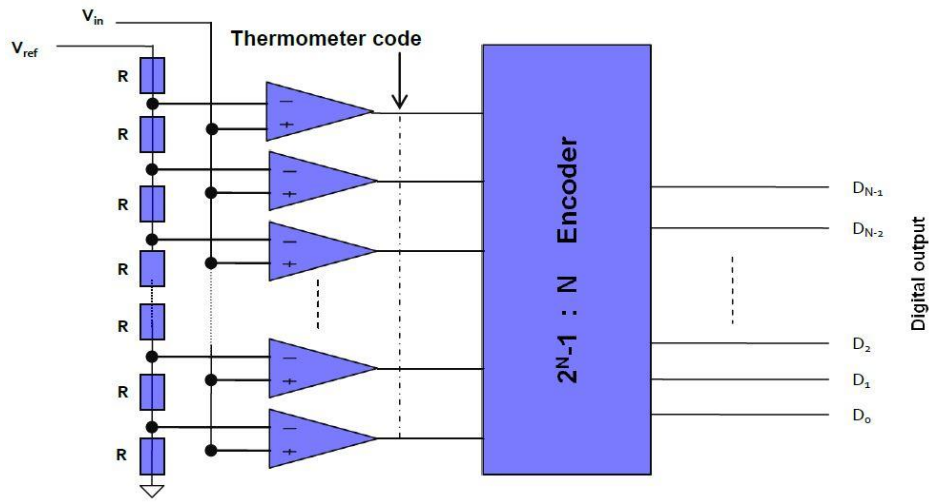

Fig. 2. Typical flash ADC block diagram

As shown in fig.2. It requires 2^N-1 comparators for an N bit converter. This much of comparators complex the design as resolution increases, requires larger die area and a large amount of power consumption. The resistor ladder network is formed by 2^N resistors, and which provide reference voltage to the comparator. These reference voltages are spaced equally by V_{LSB}. An analog input is connected to all comparators and compares with reference voltage, so that each comparator output is produced in one cycle. When the input voltage (positive terminal) is more than the reference voltage (negative voltage) it generates logic 1 as output, otherwise, output is zero. The set of comparators produce digital output called thermometer code and is changed into a binary code through the encoder.

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VI. MODIFIED FLASH ADC

In this modified flash ADC with dynamic latch comparator is proposed. The traditional flash analog to digital converter requires 2^N-1 comparators for designing N-bit flash ADC. For 4-bit flash ADC it requires 15 comparators. As number of bits increases it is very complex and count of comparators also more. And these comparators are working in each clock cycle causes more and more power consumption.

In order to prevent this, flash ADC with multiplexing scheme is proposed. The flash ADC with modified structure has reference voltages to comparators, these reference signals are provided through multiplexers. This type of scheme can reduce the number of comparators that are required to design ADC. By this scheme only 2^{N-2}+2 comparators are required to design N-bit ADC instead of using 2^N-1, that is for 4-bit ADC 6 comparators are sufficient. As the number of comparators is reduced power consumption also reduced. This flash ADC with dynamic latch comparators technique will limit to enough power consumption because dynamic latch comparator has an advantage of low power dissipation. The basic schematic diagram for modified flash ADC is as shown in fig.3.

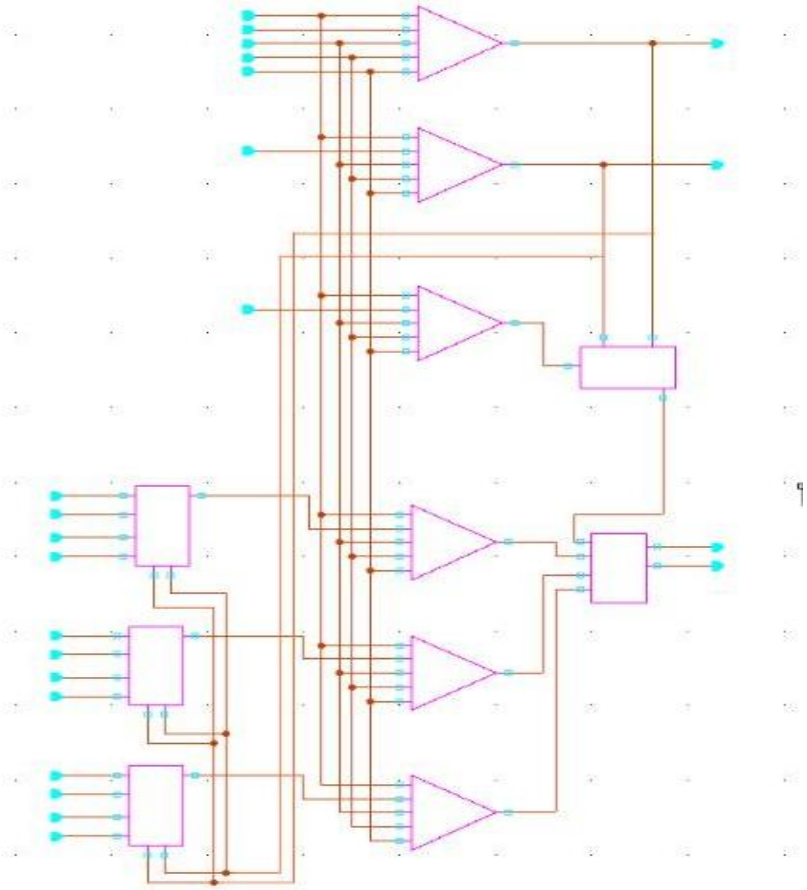

Fig. 3. Schematic diagram for proposed flash ADC

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VII. RESULT AND DISCUSSION

The simulated results for a Dynamic latch comparator with different timing waveforms are as shown in below fig.4.

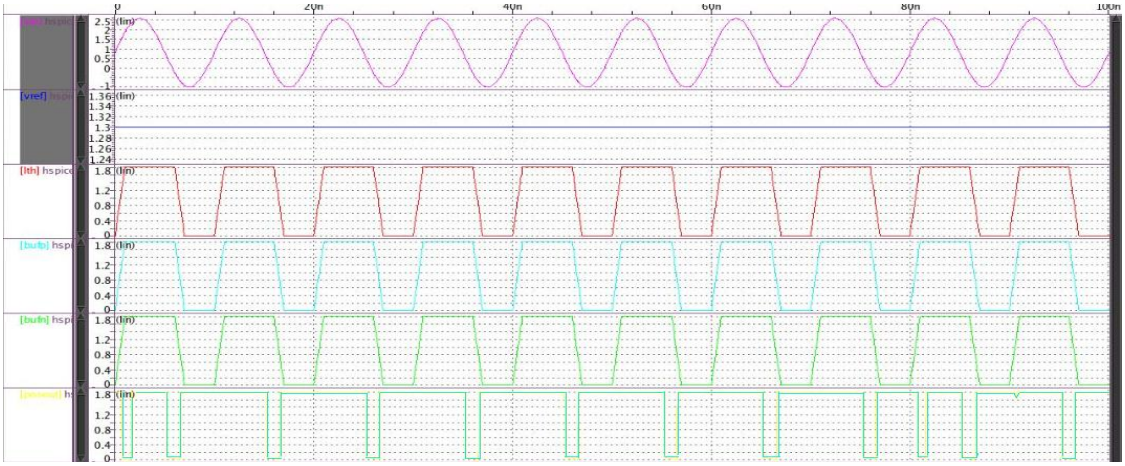

Fig. 4. Simulated results for Dynamic latch comparator

Simulated results for this proposed flash analog to digital converter using dynamic latch comparator is shown in fig.5 with different times are shown in simulated waveform.

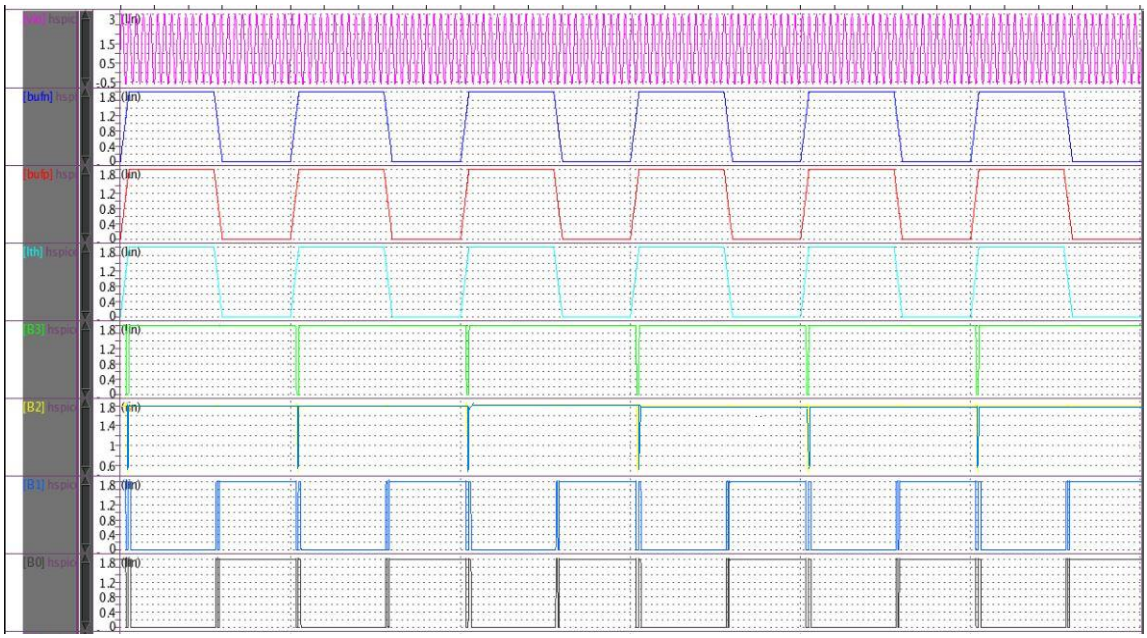

Fig. 5. Simulated results

Specifications and results for this modified flash analog to digital converter using dynamic latch comparators are presented in Table.1.

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TABLE 1
Specifications and Results for Modified Design

Resolution	4bit
Technology	0.1um
Power supply	1.8v
Reference voltage	1.3v
Input range	0-1.8v
Sample rate	1000MHZ
Power consumption	212.47uwatts

VIII.CONCLUSION

A low power and high speed modified new design for 4-bit flash analog to digital converter is presented. By this power consumption is going to be reduced than traditional flash analog to digital converter because reduction in comparators counts. The traditional flash analog to digital converter requires 82mw where as our modified design has only 212.47uw.

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