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An Efficient HPF LED Driver with Zero Voltage Switching

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ABSTRACT: Lighting is an important aspect of energy consumption. It consumes about 25% of the world's total electric energy production. Light Emitting Diode (LED) technology has now emerged promising technology to replace conventional lighting devices. LEDs are highly efficient, energy conserving and eco-friendly. The applications of LEDs include in mobile products, and back lighting of Liquid Crystal Display(LCD) panels. LED drivers utilize an AC input source; Power Factor Correction (PFC) control must be imposed in the driver to achieve a high Power Factor (PF). This is a novel two stage LED driver. It consists of a buck-boost converter and a buck converter. The buck-boost converter which serves as a PFC converter to achieve a High Power Factor and low current ripples. The buck converter step down the dc-link voltage to drive high power white LEDs. Operating the active switches at Zero Voltage Switching(ZVS) can effectively reduce the power losses. To achieve the PFC function, it should be designed to operate at Discontinuous-Conduction Mode (DCM). The buck converter can be designed to operate at either Continuous-Conduction Mode (CCM) or DCM. Operating a buck converter at CCM has the advantage of small current ripple but, it requires using an inductor of higher value than that at DCM. This High Power Factor(HPF) LED driver topology will reduce the switching losses by using soft switching technique and improves power factor to almost unity.A prototype of the topology with 25 V input voltage and four 12 V, 10 W high power LEDs is tested and it works properly. Dimming is automatically adjusted by using a Light Dependent Resistor(LDR) of diameter 5mm. Simulation is done in MATLAB. dsPIC30F2010 and ATMEGA 328P are used in control schemes.

KEYWORDS: Buck boost converter,Buck converter,Light Emitting Diode(LED),Power Factor Correction(PFC),Zero Voltage Switching(ZVS).

I.INTRODUCTION

LEDs are the fast emerging technology and have a wide range of applications. Due to the increased popularity of LEDs, the LED driver design should be simple [1]. The LED driver may be a single stage driver or a two stage driver. The single-stage approaches are derived by integrating the PFC converter and the DC/DC converter. By sharing one active switch and the control circuit, the single-stage converters have the advantages of less component count and are cost effective solutions. They are less expensive. The two-stage approach includes a PFC semi-stage to shape the input current into a sinusoidal waveform and a DC/DC semi-stage to regulate the output voltage. These two-stage approaches have the advantages of good performance, fast output dynamic response, and easy control. They require two power-conversion processes and are energy inefficient [2-8]. There are many topologies using single stage and two stage converters based on different applications. In both single stage and two stage converters, the active switches are operated in hard switching mode. Hard switching increases the switching losses.

Hence the objectives are to improve the power factor of the LED driver system for economical operation and to reduce switching losses by using a suitable technique. To reduce the switching losses soft switching techniques can be employed. By using zero voltage switching, i.e, the voltage across the device is reduced to zero before the current increases, along with the help of phase shift full bridge PWM converter switching losses can be reduced. Therefore, a new two stage topology can be introduced which will improve the PF and reduces the switching losses. A buck converter can be used to drive the LEDs with required voltage [9-11].The circuit configuration and operation of the proposed topology is given in section II. Section III deals with detail circuit analysis. An illustrative design example

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and MATLAB simulation results are given in section IV. Section V is the hardware implementation and obtained waveforms. Section VI gives the conclusion of this paper.

II.CIRCUIT CONFIGURATION AND OPERATION

Fig. 1 shows the block diagram of the proposed topology. It consists of a diode bridge rectifier, buck-boost converter and a buck converter.

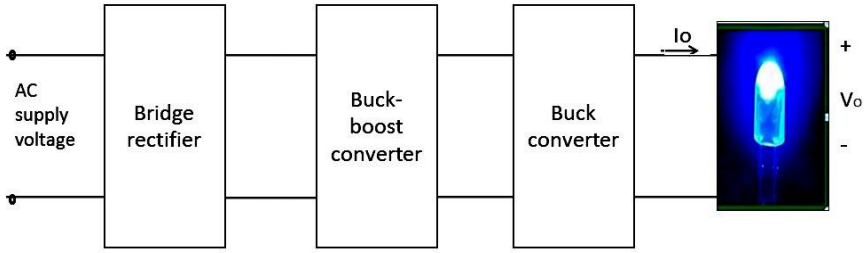

Fig.1. Block Diagram

The diode bridge rectifier converts the input AC voltage to DC. The buck-boost converter performs the function of PFC, and the buck converter steps down the dc-link voltageto drive LEDs. Both active switches can operate at Zero-VoltageSwitching-on (ZVS) to effectively reduce the switching losses.To achieve the PFC function, it should be designed to operate at Discontinuous-Conduction Mode (DCM). The buck converter can be designed to operate either in Continuous-Conduction Mode (CCM) or in Dis-continuous Conduction Mode (DCM).Continuous-Conduction Mode (CCM)has the advantage of small current ripple. At the same time an inductor of higher value is required for operation. Hence the latter method is preferred. The circuit diagram for the proposed topology is shown in Fig. 2.

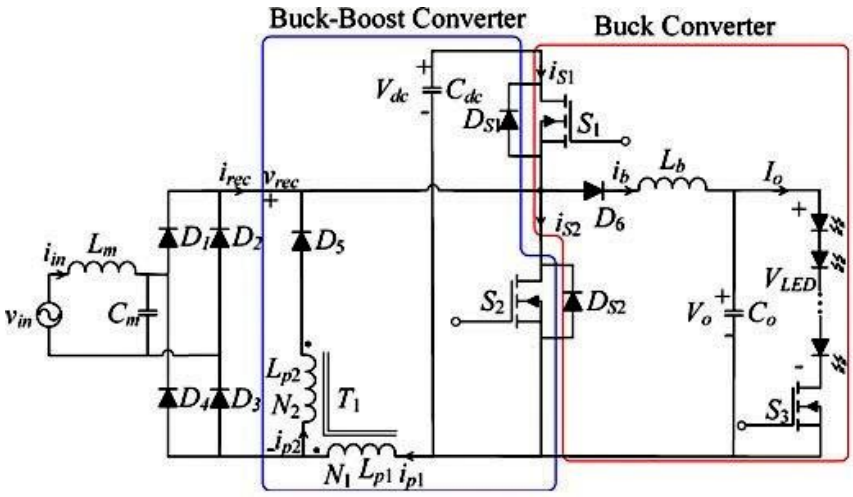

Fig.2. Circuit Diagram

The first stage is a buck-boost converter consists of diodes D_5 and D_{S1}, an active switch S_2, two coupled inductor L_{p1} and L_{p2}, and a dc-link capacitor C_{dc}. It serves as the PFC circuit by wave shaping the input current to be sinusoidal and in phase with the input line voltage. The second stage is a buck converter consisting of diodes D_6 and D_{s2}, an active switch S_1, an inductor L_b, and a capacitor C_0. Diode D_6 is used to block the reverse current of buck inductor and can be removed when the buck converter is operated at CCM. Instead of using a single inductor, two coupled inductors along with a blocking diode (D_3) are used to accomplish buckbuck-boost conversion. The turnsratioof the two coupled inductors is designed to induce voltage on L_{p2} to block the current from the line source.A small low-pass filter, Lm and C_m, is used to remove the highfrequency current harmonics at the input line. MOSFETs S_1 and S_2 are the bidirectional switches. Each switch is composed of a transistor and an anti-parallel diode. The MOSFET's intrinsic body diodes D_1

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and D_2 are used as the anti-parallel diodes. For dimming operation, the active S_3 is placed in series with the LED string. Switch $S_3$is controlled by the scheme of low-frequency pulse-width modulation. The active switches $S_1$and S_2 are alternately driven by two gated signals, v_{GS1} and v_{GS2}. They are non-overlapping and complementary rectangular-wave voltages with a short dead time at the high switching frequency f_s. The dead time is the time interval when v_{GS1} and v_{GS2} are both zero. Neglecting the short dead time, the duty cycle of v_{GS1} and v_{GS2} is 0.5. For simplifying the circuit analysis, the following assumptionsare made:

- All the circuit components are ideal.
- V_{dc} and V_o can be regarded as constant voltage sources.

The input low-pass filter formed by L_m and C_m and the diode bridge rectifier can be replaced with the voltage V_{rec}. The output LED string can be replaced with its equivalent resistance $R_{LED.}$ At steady state, the circuit operation can be divided into six modes in each high-frequency cycle. For simplifying the circuit analysis, the low-pass filter and the diode rectifier (D_1- D_4) is represented by the rectified voltage V_{rec} and the LED string is represented by its equivalent resistance R_{LED}. Fig. 3 shows the six modes of operation. The circuit operation is described as follows.

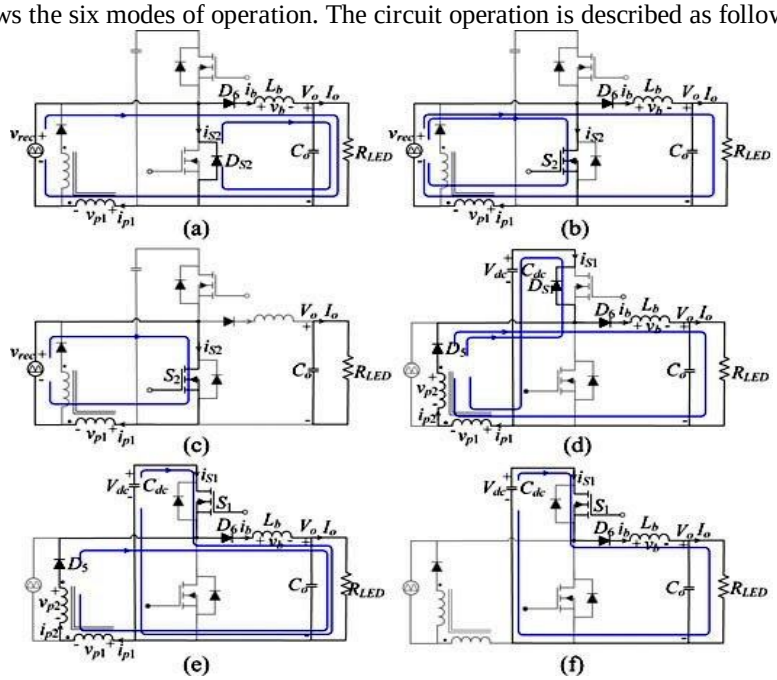

Fig.3. Modes of Operation

A. Mode I (t_0<t<t_1)

This mode begins as soon as S_1 is turned OFF. The current i_b diverts from S_1 to D_{S2}. The voltage across the buck inductor is equal to V_0 and i_b starts to decrease from a peak value. At the same time, the voltage across the buck-boost inductor L_{p1} is equal to the rectified input voltage V_{rec}Since the buck-boostconverter is designed to operate at DCM, the buck-boost current ip1 increases linearly from zero with a rising slope thatis proportional to V_{rec}. The theoretical waveforms of buck converter are shown in Fig. 4. In the initial stage of this mode, i_b is higher than ip1. Parts of i_b flow through D_{S2}, while the rest of i_b is equal to i_{p1} and flows through L_{p1}, diode bridge rectifier and the line-voltage source. Since D_{S2} is on, the voltage across $S_1$is clamped at -0.7 V. After the short dead time, v_{GS2} becomes a high level.Switch S_2 does not conduct current until the rising current i_{p1} becomes higher than the decreasing current i_b and then, thecircuit operation enters Mode II.

B. Mode II (t_1<t<t_2)

In this mode, S_2 is on and i_{p1} is higher than i_b. There are two current loops. Parts of $i_{p1}$are equal toi_b and flows through D_6, L_b, C_o, L_{p1} and the line-voltage source, while the rest flows throughL_{p1} and the line-voltage source.The voltage equations for v_b and v_{p1} are the same as those in Mode I. The current i_b keeps decreasing. Now i_{p1} keeps increasing.

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Ifthe buck converter operates at DCM, the circuit operation entersMode III as soon as i_b decreases to zero. If it operates atCCM, the circuit operation enters Mode IV at the instant timeof turning OFF S_2. The current i_b is zero. S_2 is kept at on stage and i_{p1} keeps increasing. This mode ends at the instant time of turning OFF S_2 and the circuit operation enters Mode IV.

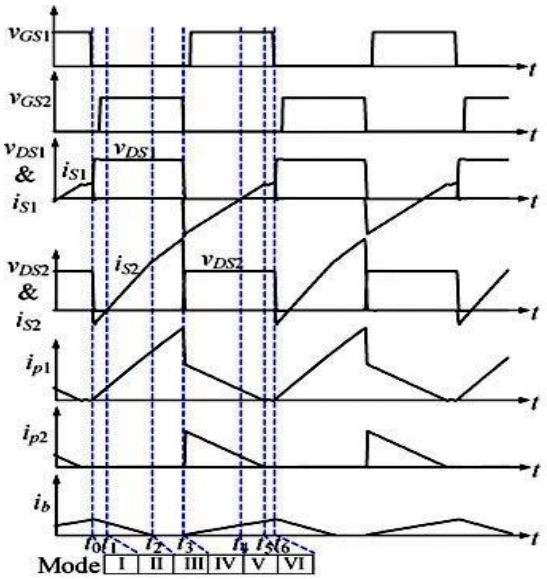

Fig.4. Waveforms

C. Mode III ($t_2<t<t_3$)

The current i_b is zero. $S_2$is kept at on stage and i_{p1} keepsincreasing. This mode ends at the instant time of turning off S_2,and the circuit operation enters Mode IV.

D. Mode IV ($t_3<t<t_4$)

At the beginning of this mode, i_{p1} reaches a peak value. Inorder to ensure the buck-boost converts i_{p1} on operation, i_{p1}should be diverted from S_2 and flows through L_{p1}, L_{p2}, D_5, and $D_{S1}$to charge the dc-link capacitor $C_{dc}$when S_2 is turned OFF. For this, the voltage across the inductor L_{p2} must be higher than the amplitude of the input voltage to block the current from the ac line source. By this way, the diode-bridge rectifier is reverse-biased. Currents $i_{p1}$and i_{p2} will be equal and flow through diode D_5 Current i_{p1}drops and i_{p2} rises dramatically at the switching-off instant. The negative dc-link voltage is imposed on the coupled inductors, and both $i_{p1}$and i_{p2} decrease linearly. Regarding operation of the buck converter, since D_{s1} is on,the voltage across L_b is equal to V_{dc}-V_O and, i_b rises linearly. In the initial stage of this mode, i_{p1} (i_{p2}) is higher than i_b. Parts of i_{p1}flow through D_{s1} to charge C_{dc}, while the rest of $i_{p1}$is equal to i_b and flow into the buck converter. Since $D_{s1}$is on, the voltage across $S_1$is clamped at -0.7 V. After the short dead timev_{GS1} becomes a high level. S_1does not conduct current until the rising current i_b becomes higher than the decreasing current i_{p1}, and then the circuit operation entersMode V.

E. Mode V ($t_4<t<t_5$)

In this mode, $S_1$is on and i_b is higher than i_{p1}. There are twocurrent loops. Parts of i_b are supplied from the dc-link voltage and the rest of i_b is equal to $i_{p1}$and flow through L_{p1}, L_{p2}, and D_5. Both the currents $i_{p1}$and i_{p2}keep decreasing. The circuit operation enters Mode VI when $i_{p1}$and i_{p2} decrease to zero.

F. Mode VI ($t_5<t<t_6$)

In this mode, $S_1$is remained at on stage and i_b keeps increasinglinearly. This mode ends at the time when v_{GS1} becomes to a low level to turn OFF S1, and the circuit operation returns to Mode I of the next cycle.

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III. Design and Analysis

The anti-paralleldiode of the active switch of one converter serves as the freewheeling diode of the other converter, the features of the buck-boost and the buck converter can be retained. Therefore, the two converters can be analyzed separately. An LED driver for 4, 10 W white LEDs is illustrated as a design example. Table 1 shows the circuit specifications and are obtained by using the below equations.

Table 1: Circuit Specifications

Input voltage	25 V
High switching frequency	50 kHz
Low switching frequency	200 Hz
Output power	40 W
Output voltage	48 V
Output current	0.8 A
LED voltage	12 V
LED current	0.8 A
LED equivalent resistance	3200 Ω

The input voltage is 25 V. The forward voltage drop for 1 LED is 12 V. Hence the output voltage for 4 LEDs is 48 V. From output power and output voltage, the output current can be calculated. The equivalent LED resistance can be obtained from output voltage and output current.Table 2 gives the circuit parameters.

Table 2: Circuit Parameters

Filter inductor	2 mH
Filter capacitor	0.47 µF
Switches	IRFP250
Buck inductor	1.94 mH
Coupled inductors(buck boost inductor)	0.46 mH
DC link capacitor	100 µF
Buck capacitor	100 µF

A. *Buck- boost converter*

In the operation from Mode I to Mode III, either S_2 or D_{S2} is on, the rectified voltagev_{rec} supplies energy to raise the current i_{p1}. Since the buck-boostconverter is operated at DCM, ip1raises from zero at the beginning of Mode I and reaches a peak value at the end of Mode III. The input voltage is given by,

$$V_{in}(t) = V_m \sin \omega t \quad (1)$$

The input current can be calculated by integrating the current i_{rec} over one cycle. It is given by,

$$I_{in}(t) = \frac{T_s V_m}{8 L_{p1}} \sin\omega t \quad (2)$$

From the above two equations, it is clear that input currentis a sinusoidal waveform and it is in phase with input voltage. Hence a HPF is achieved.The input power is given as:

$$P_{in}(t) = \frac{T_s {V_m}^2}{16 L_{p1}} \quad (3)$$

The output power is given by

$$P_{out}(t) = \frac{T_s {V_m}^2}{16 L_{p1}} \times efficiency \quad (4)$$

With a 92% efficiency, the value of L_{p1} can be obtained. The value of L_{p2} and L_{p1} are equal.

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B. *Buck converter*

The on time of the buck converter is the interval from the beginning of operation Mode IV to the end of Mode VI. During this interval, either S_1 or D_{S1} is on. Hence, the duty ratio of the buck converter is also 0.5. At steady-state operation, the average value of i_b is equal to LED current. For fulfilling DCM operation, V_{dc} should be less than or equal to $2V_o$. The buck inductor L_b can be designed by using the equation:

$$L(b) = \frac{V_{dc}T_s R_{LED}(V_{dc}-V_o)}{8{V_O}^2} \quad (5)$$

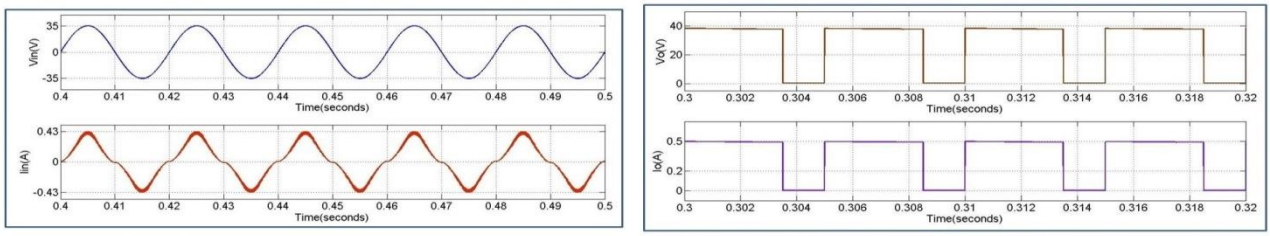
By diverting the current in one active switch to the anti-parallel diode of the other one is what enables the active switches to achieve ZVS operation. By this way, the anti-parallel diode conducts current prior to the transistor in each MOSFET. The voltage across the transistor is maintained at about -0.7 V when its anti-parallel is on. This small voltage is negligible and the transistor can be turned ON at zero voltage. It means that the turn-on switching loss is effectively eliminated.

IV. SIMULATION AND HARDWARE DEVELOPMENT

This section deals with the simulation waveforms and hardware details of the LED driver topology.

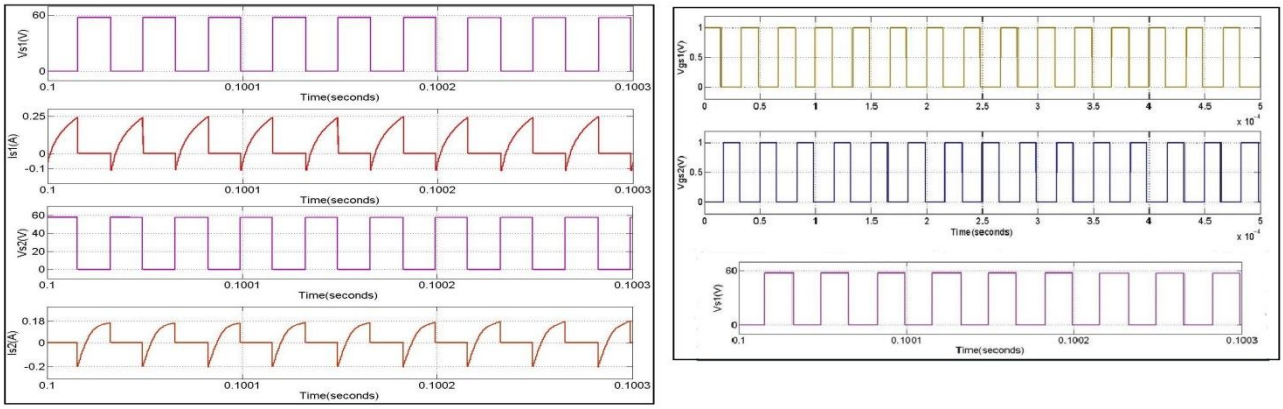
A. Simulation Waveforms

Fig. 8 shows the input voltage and current waveforms.From the figure the input voltage is 25 V. The input voltage and input current are inphase. Magnitude of input current is less than 1A. Current and voltage waveforms for the switch $S_1$and S_2 are shown in the Fig. 9 and gate pulses for the three switches are also shown in the same figure.



Input voltage, input current **Output voltage, output current**

Fig. 8 Input and Output Waveforms



Voltage and current waveforms of switch 1 and 2 **gate pulses for switches 1, 2 and 3**

Fig. 9 Waveforms of switches and their gate pulses

The gate pulses shows that switches are operated complementary. Duty cycle is 46% and it is same for both the two switches and the switching frequency is 50 kHz. A short dead time is provided. The voltage across the DC- link capacitor C_{dc} is given in Fig. 10 and current through the primary and secondary winding of coupled inductor is also given in the same figure. According to design criteria magnitude of capacitor voltage should be less than $2V_o$ and

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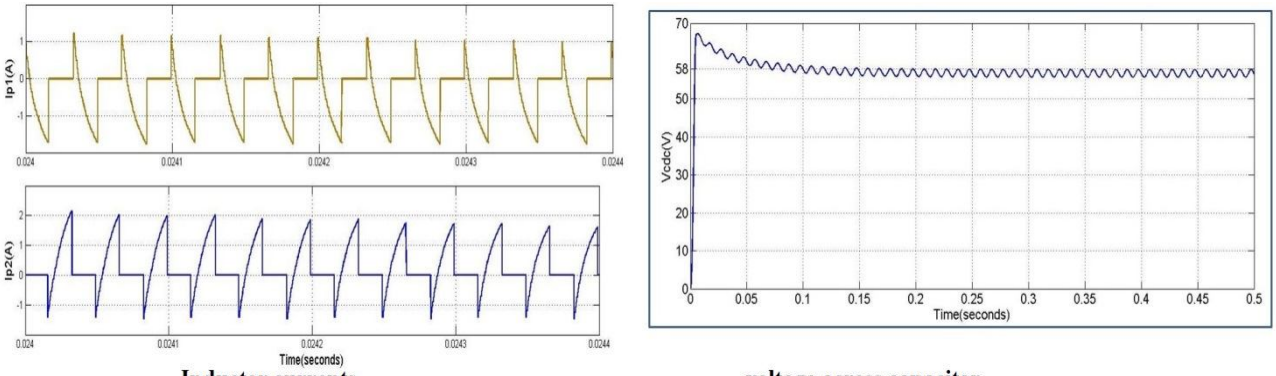
greater than V_o. Here the magnitude is 58 V. Gating pulses for switch S_3 is shown in Fig. 9.Dimming is done in the output by using the switch S_3 and dimming can be controlled with respect to the intensity oflight in the room.



Inductor currents **voltage across capacitor**

Fig. 10 Inductor currents and DC- link capacitor voltage

Voltage corresponding to the light intensity in room is scaled by using a factor 20.The output voltage and current waveforms for 20% dimming is shown in Fig. 8. The output voltage and current contains less ripples.

B. Hardware Development

This section deals with the experimental results of the prototype having four 12 V, 10 W LEDs and an input voltage of 25 V. The prototype is shown in Fig. 11. Three MOSFET switches are used here.

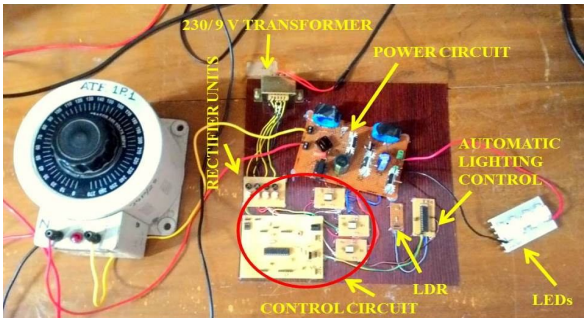
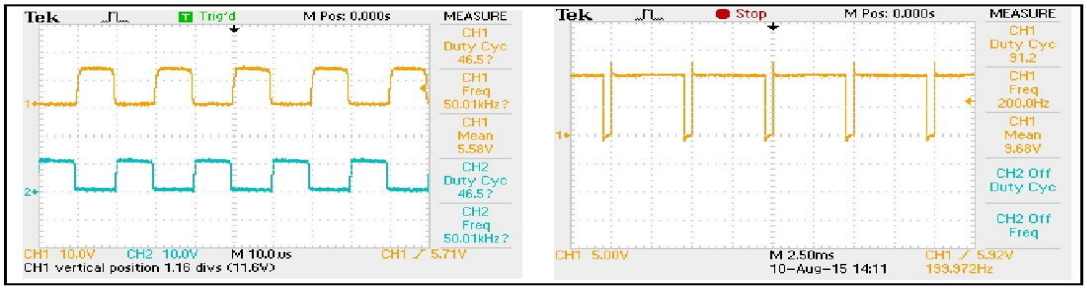


Fig. 11 Prototype Test Circuit

The input to the prototype is 25 V AC and is connected to the mains through a single phase auto transformer.A single phase step down transformer of rating 230/ 9 V is used for giving supply to the control circuits.The transformer has 4 isolated secondary windings and they are connected to 4 rectifier units. There are three switches in the topology.



Pulses for switches 1 and 2 **Pulses for switch 3 at 91% duty cycle**

Fig. 12 Input Waveforms

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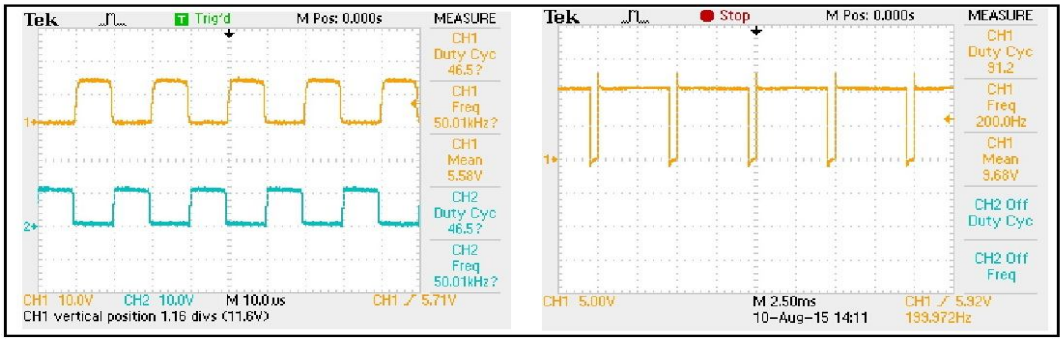
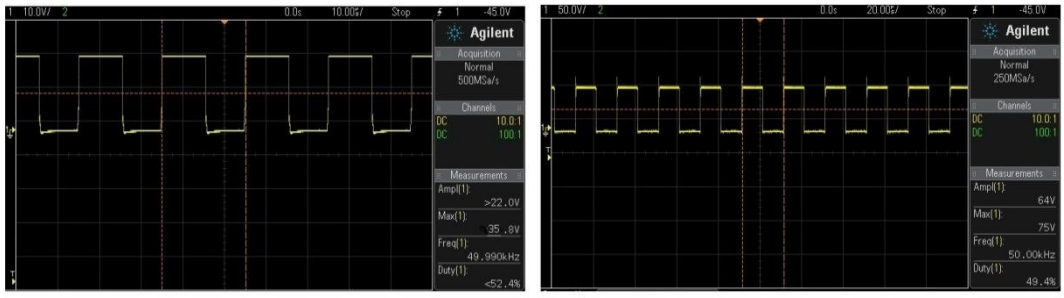


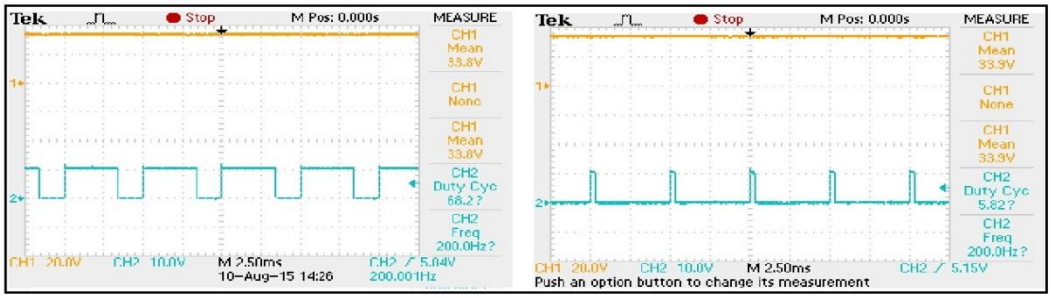
Pulses for switches 1 and 2 **Pulses for switch 3 at 91% duty cycle**

Fig. 13 Gate pulses for the three switches



Voltage across switch1 **Voltage across switch 2**

Fig. 14 Voltage across switches 1 and 2



Output voltage at 68% duty cycle **Output voltage at 5% duty cycle**

Fig. 15 Outputvoltage at different duty cycles

Two of them ($S_1$and S_2) are complementary switches. The digital signal controller dsPIC30F2010 is used for controlling these switches. Gating pulses are generated according to the program written in MPLAB. Working voltage of dsPIC is only 3 V and it is insufficient for driving the switches. Hence an optically isolated gate driver TLP250 is used for this purpose.Three gate driver IC's are required for three active switches. A voltage regulator LM317 is used to drive dsPIC which reduces the 12 V to 3 V. The 4 secondary windings of single phase transformer are connected to three gate driver IC's and to LM317. The input voltage and current waveforms are given in Fig. 12. Gate pulses for the two switches are shown in Fig. 13. Voltage across the switches 1 and 2 are given in Fig.14. The light intensity at the output is varied with the help of a LDR. Therefore the experiment is conducted in absence and presence of day light. Pulses for switch S_3 with 91% is shown in Fig. 12. In a dark room brightness of the LED array is more and is shown in Fig. 15. Output voltage in the day light is given in same figure. Comparing these experimental results with the theoretical waveforms, we can see the shape of all the waveforms are identical to the theoretical waveforms.

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V. RESULTS AND DISCUSSIONS

By comparing the input voltage and current waveforms as shown in Fig. 8, it is clear that they are inphase and there by power factor is improved. FFT analysis for input current is given in Fig. 16. There is only 21% of third harmonics in input current and higher order harmonics are less than 3%.

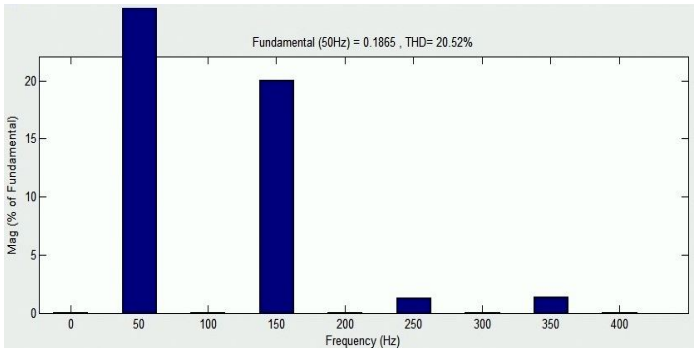

Fig. 16 FFT Analysis for Input Current

For getting better results, dsPIC control can be replaced by fuzzy logic or FPGAaccording to the needs and improvement in the circuit. Based on the application, the LED array can be arranged in different manner [13-16]. For indoor lighting applications only a few numbers of LEDs are required. The same topology can be used for outdoor lighting with more number of high power LEDs.

VI.CONCLUSION

This is a novel two stage LED driver. It consists of a buck-boost converter and abuck converter. The buck-boost converter which serves as a PFC converter is operated at DCM toachieve a high power factor and low current THD. The buck convertersteps down the dc-link voltage to drive high power whiteLEDs. The circuit operation is described, and design equationsare derived. For achieving the design goals of high power factorand ZVS operation, the output voltage cannot be lower than theamplitude of input voltage. Both active switches can achieve ZVS. Automatic dimming operation is achieved by controlling the duty ratioof the active switch S_3 with the help of a LDR. A prototype of 48 V, 40 W is tested and simulation results are obtained by using MATLAB. THD is 22%.

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