An Improved Inverter Based Double-Tail Comparator for Ultra Low-Voltage Circuits

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ABSTRACT: Comparators are most commonly use and basic blocks of analog-to-digital converters. For the purpose of increasing speed and also for lesser power and delay circuits needed high-speed comparators. It is very difficult and challenging to design high-speed comparators when the smaller of supply voltages. In this paper, a new double-tail comparator i.e inverter based double-tail comparator is implemented with lesser power, high speed and low-voltages based on the results of conventional double-tail and proposed double-tail comparators. When compared to the results of conventional and proposed double-tail comparators, a new inverter based double-tail comparator gives better performance in terms of delay and power. this project is done with tanner tools in 180nm technology. output waveforms will be shown in w-edit.

KEYWORDS: Double-tail comparator, low power, High Speed, Analog-to-Digital Converter.

I.INTRODUCTION

After op-amp's, we mostly use comparators as the electronic components. Comparators are mostly used in analog-to-digital converters. Basically comparators are well defined as 1-bit analog-to-digital converters. By using comparators, analog signal is converted into digital signal. The comparators conversion speed is optimized by the response time of decision making phase. Comparator is one of the process of optimization of the convertion speed. In today's market, there is demand for low-power and high speed portable devices and mobiles in smaller chip area.

Analog circuits have negatives of lesser power supply voltages. Threshold voltage is not decreased when the supply voltage is smaller. So, designing of comparator with smaller supply voltage is more challenging it leads to increase chip area and power. In ADC, clocked regenerative comparators are used for the purpose of low-power, low-delay and high speed for the reduction of delay and power.

Due to the strong positive feedback in the regeneration of latch, the clocked regenerative comparators are used for making fast decision (Positive feedback is nothing but regenerative feedback). In this project, by using different types of comparators for the reduction of delay and power in order to increases the speed.

II. PREVIOUS WORK

It includes the description of previous structure conventional comparator and conventional double-tail comparator .The structure of conventional comparator and conventional double-tail comparator is shown in below figure.

A. CONVENTIONAL SINGLE-TAIL COMPARATOR:

Conventional single-tail comparator is shown in below figure. Coming to operation, during pre-charge mode clock is applied with 'zero'. Tail transistor Mtail is off, the transistors M7 and M8 are on. Then charge the output nodes(outn & outp) to Vdd. During evaluation mode, clock is applied with 'Vdd'. Mtail is on and transistors M7&M8 are off. Then the output nodes have starts their discharging rates with various values. If the voltages one of the input is higher than that specified output is discharges faster to ground. If VINP>VINN it shows the voltage of INP is higher

than INN then automatically corresponding output i.e outp discharges to ground, outn pulls to Vdd. If VINN>VINP then circuit works in opposite.
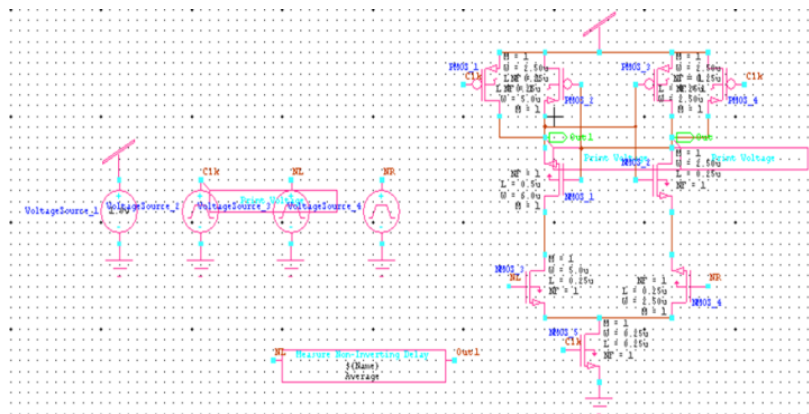

Fig.1: Schematic of conventional single-tail comparator

Drawbacks of single-tail comparator is, there is one current path via single tail for both latch and differential amplifier it may leads to reduce the speed of latch regeneration then also power is increased. To overcome this drawback we go for double-tail comparator.

B.CONVENTIONAL DOUBLE-TAIL COMPARATOR:

Conventional double-tail comparator shows below figure. By using double-tail , it can supply required amount current to both latch and difference amplifier. It may leads to increase the speed of latch regeneration. Here we use additionally two intermediate stage transistors MR1 and MR2 these are pases the ΔVf(np) to the latch stage. During pre-charge phase, clock is applied with 'zero' then both Mtail1 & Mtail2 are off. The transistors M3 & M4 are on these are pre-charge the fn & fp nodes to Vdd. During evaluation mode, when clock is applied with 'Vdd'. Both Mtail1 & Mtail2 are on. M3 & M4 are off.the voltages near fn and fp nodes have drops with various values. For the purpose of increasing speed we go for another technique in the double-tail comparator.
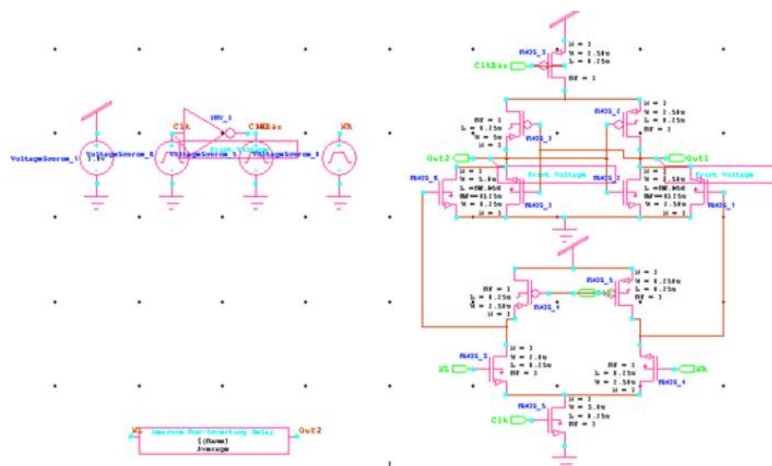

Fig.2: schematic of conventional double-tail dynamic comparator

In this comparator both MR1 & MR2 are in cut off. Due to this reason they cannot play any role for increasing speed of latch. To overcome this we can go for another technique based on double-tail comparator.

III. IMPLEMENTATION OF CONVENTIONAL DOUBLE-TAIL COMPARATOR

Implemented double-tail comparator is shown below. For better performance, modified double-tail comparator is implemented. The main idea of the modified one is increased the speed of latch regeneration in low-voltage applications. We connect two MC1 and MC2 control transistors in a cross coupled type for the increase of latch regeneration speed to the conventional double-tail comparator. During reset mode, clock is applied with 'zero'. Both Mtail1 and Mtail2 are in off, M3 and M4 are on. Both control transistors MC1 & MC2 are in cut off. The intermediate transistors MR1 & MR2 discharges the output nodes of latch to ground. During evaluation mode, clock is applied with 'Vdd'. Both Mtail1 & Mtail2 are on, M3 & M4 are off. At the beginning position of this mode the both control transistors MC1 & MC2 are in cut off mode. Then output nodes i.e fn and fp slowly precharge to vdd.
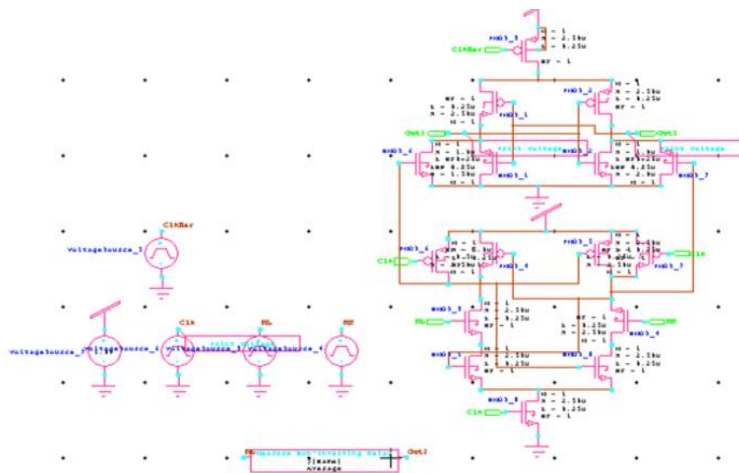

Fig.3: Implemented double-tail dynamic comparator

The output nodes fn and fp start to drop with their various values. If VINP>VINN then the VINP corresponding node of fn is faster discharges then the VINN corresponding node of fp. Thus, the corresponding transistor of fn i.e M2 provides larger amount of current then M1. As long as fn continuous falling, then that related PMOS transistor MC1 starts to turn on, pulling fp node back to Vdd. Thus fp is at Vdd. When the control transistor MC1 is on, the current drawn path from Vdd to ground is via MC1, M1, & Mtail1 results static power consumption. To reduce this problem, connect two NMOS switches below input M1 & M2 transistors i.e Msw1 & Msw2. If fp node is discharges to ground then that corresponding switch Msw2 in the current drawn path is closed then the other switch Msw1 will be open for the prevent of current. In this technique speed of latch is increased when compared to the previous conventional double-tail comparator. For the purpose of increasing latch regeneration another implementation is below.

IV.INVERTER BASED DOUBLE-TAIL COMPARATOR DESIGN

Inverter based double-tail comparator is shown below. During reset mode, clock is applied with 'zero'. Both Mtail1 and Mtail2 are in off, M3 and M4 are on. Both control transistors MC1 & MC2 are in cut off. The intermediate transistors MR1 & MR2 discharges the output nodes of latch to ground. During evaluation mode, clock is applied with 'Vdd'. Both Mtail1 & Mtail2 are on, M3 & M4 are off. At the beginning position of this mode the both control transistors MC1 & MC2 are in cut off mode. Then output nodes i.e fn and fp slowly precharge to vdd. The output nodes fn and fp start to drop with their various values.

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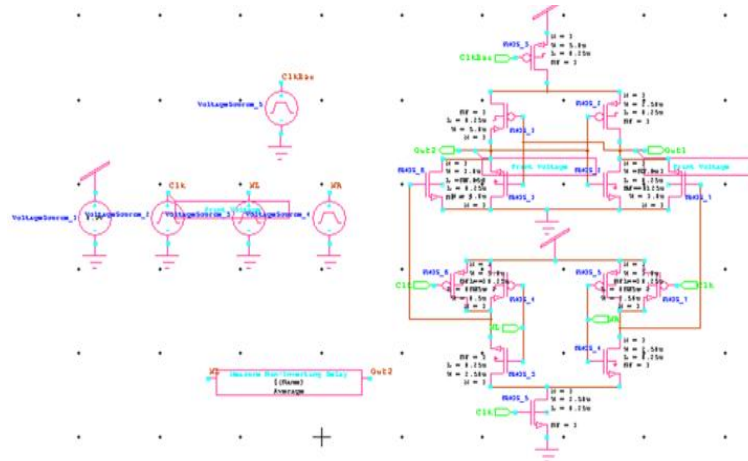
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Fig.4: schematic of inverter based double-tail comparator

If VINP>VINN then the VINP corresponding node of fn is faster discharges then the VINN corresponding node of fp. Thus, the corresponding transistor of fn i.e M2 provides larger amount of current then M1. As long as fn continuous falling, then that related PMOS transistor MC1 starts to turn on, pulling fp node back to Vdd. Thus fp is at Vdd. So, the corresponding intermediate stage transistor MR1 turns on and it will caused to regenerate the latch by using back to back inverters in the latch stage so that the output node outn completely discharges to ground and another output node outp is charges to Vdd.

V. SIMULATION RESULTS

The simulation of all above designs is carried out by using Tanner EDA tool v13.0 with 180nm technology. The simulated waveforms of conventional single-tail, conventional double-tail, proposed double-tail and inverter based double-tail comparators.
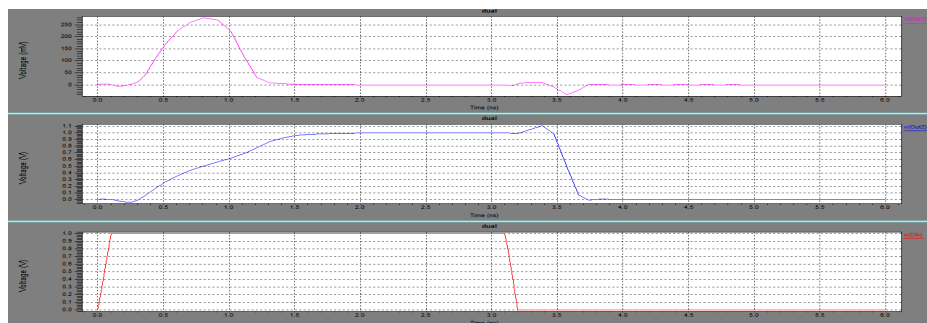

Fig.5: Simulated waveforms of conventional single-tail comparator

In simulation result of conventional single-tail comparator shows VINN>VINP i.e supply voltage is 1v and applied input voltages are VINN is 1v and VINP is 0.8v then the output of corresponding VINN i.e out n will be discharged to ground i.e 0, and out p will be high i.e 1. This will be shown in the above simulation result

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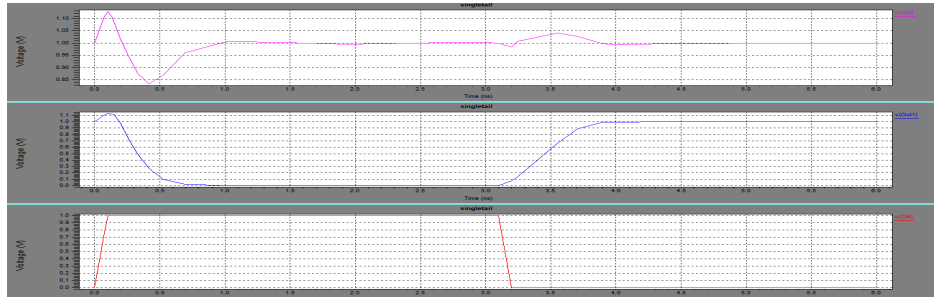*(An ISO 3297: 2007 Certified Organization)*

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Fig.6: Simulated waveforms of conventional double-tail comparator

In simulation result of conventional double-tail comparator shows VINN>VINP i.e the output node of the VINN is greater when compared to VINP then the corresponding node of VINN is pull to Vdd means output will be 1. then the another node of corresponding VINP will be discharged to ground i.e zero.This will be shown in the above simulation result.
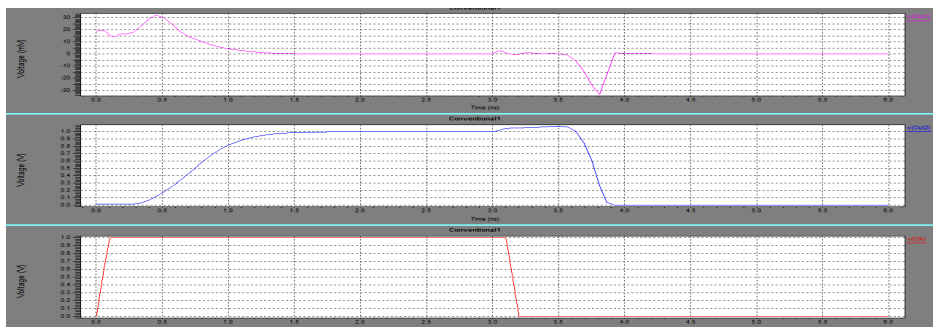

Fig.7: Simulated waveforms of implemented double-tail comparator

In simulation result of implemented double-tail comparator shows VINN>VINP means applied voltage of VINN is higher than VINP. then the corresponding output node of higher input voltage i.e out n will be pull to Vdd i.e output will be shown 1. the another output node out p will be discharged to ground completely mens it's zero. the result will be shown in the above simulation figure.
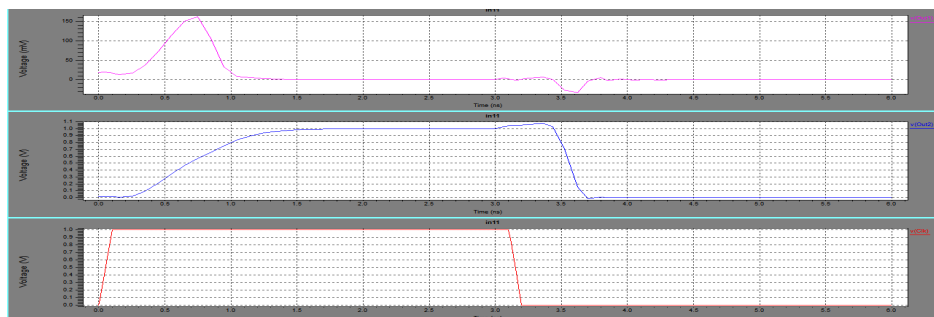

Fig.8: Simulated waveforms of inverter based double-tail dynamic comparator

In simulation result of inverter based double-tail comparator shows VINN>VINP means given input voltage of VINN is greater than the VINP. then the corresponding output node of higher input i.e out n will be pull to Vdd i.e the output will be shown 1. then the other output node out p will be discharged to ground completely i.e the output will be shown zero. the output results will be shown in the above simulation results.

PERFORMANCE COMPARISION

Table.1: Performance comparison for different designs

	Single-tail	Double-tail	Conventional double-tail	Inverter based
Power dissipation (w)	2.961 μw	936.1 n w	865.0 n w	800.0 n w
Delay(sec)	2.5930 ns	2.1448 ns	2.1346 ns	2.0522 ns
Gain (db)	-	-	-59.812	-53.801

VI. CONCLUSION

Inverter based double-tail comparator was designed that works with high speed and low power consumption when compared to double-tail comparator and implemented double-tail comparator. For comparison we provide analog input to the comparator and the output will be digital. The simulation results show that the inverter based double-tail comparator circuit can operate at higher speed with low power dissipation than the other double-tail comparators. This project is done by using tanner tools with 180nm technology. Waveforms will be shown in w-edit.

REFERENCES

[1] Samaneh Babayan-Mashhadi, "Analysis and design of a low-voltage low- power Double-tail comparator", IEEE Trans. Feb-2014.
[2] B. Goll and H. Zimmermann, "A comparator with reduced delay time in 65-nm CMOS for supply voltages down to 0.65," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 56, no. 11, pp. 810–814, Nov. 2009.
[3] M. Maymandi-Nejad and M. Sachdev, "1-bit quantiser with rail to rail input range for sub-1V __ modulators," IEEE Electron. Lett., vol. 39,no. 12, pp. 894–895, Jan. 2003.
[4] P. Nuzzo, F. D. Bernardinis, P. Terreni, and G. Vander Plus, "Noise analysis of regenerative comparators for reconfigurable ADC architectures," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 55, no. 6, pp. 1441–1454, Jul. 2008.