ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 8, August 2015

Optimization of Power in C-MOS Circuit

M.Kanmani[1], Dr.T.V.U.Kiran Kumar*[2]

Assistant Professor, Dept. of ECE, Jerusalem College of Engineering, Chennai, Tamil Nadu, India[1]

Assistant Professor, Dept. of ECE, Bharath University, Chennai, Tamil Nadu, India[2]

* Corresponding Author

ABSTRACT: A generalized power tracking algorithm that minimizes power consumption of digital circuits by dynamic control of supply voltage and the body bias is proposed. A direct power monitoring scheme is proposed that does not need any replica and hence can sense total power consumed by load circuit across process, voltage, and temperature corners. Design details and performance of power monitor and tracking algorithm are examined by a simulation framework developed using UMC 90-nm CMOS triple well process. The proposed algorithm with direct power monitor achieves a power savings of 46.2% for activity of 0.02 and 25.4% for activity of 0.04. Experimental results from test chip fabricated in AMS 70 nm process shows power savings of 46.3% and 90% for load circuit operating in super threshold and near sub-threshold region, respectively.

KEYWORDS: Dynamic voltage and threshold scaling (DVTS), leakage current control, sleep transistor, variable body bias, and variable supply voltage

1. INTRODUCTION

Dynamic power management (DPM) is employed at operating system level to adjust the supply voltage for each power state. The supply voltage is conservatively margined to account for process and temperature variations. These voltage margin increases with technology scaling due to larger process variations, rendering DPM less efficient. On the other hand, the hardware approach like dynamic voltage scaling (DVS) allows voltage to be scaled such that the actual delay of the chip instead of worst case delay meets the target performance. This enables more power savings as minimum possible voltage for target performance can be attained. In

DVS the supply voltage is adjusted to meet the target delay using an on-chip delay monitor in a hardware feedback loop. Performance degradation is a direct consequence of supply voltage reduction. In order to maintain the required throughout, dynamic voltage scaling (DVS) systems are used to adjust the supply voltage according to throughput requirements.

Though DVS very well manages the dynamic switching power, with shrinking feature size the static (leakage) power has increased exponentially which it cannot control. Particularly, at low activity levels, leakage power is dominant. We present a Dynamic VTH Scaling (DVTS) scheme to save the leakage power during active mode of the circuit. Dynamic voltage and threshold scaling (DVTS) manages both dynamic and leakage power by adjusting supplies voltage and body bias voltage. The power saving strategy of DVTS is similar to that of the Dynamic VDD Scaling (DVS) scheme, which adaptively changes the supply voltage depending on the current workload of the system. Instead of adjusting the supply voltage, DVTS controls the threshold voltage by means of body bias control, in order to reduce the leakage power. The power saving potential of DVTS and its impact on dynamic and leakage power when applied to future technologies are discussed. Finally, a feedback loop hardware for the DVTS which tracks the optimal VTH for a given clock frequency, is proposed. Simulation results show that 92% energy savings can be achieved with DVTS for 70nm circuits.

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II. EXISTING SYSTEM

Dynamic voltage scaling (DVS) has become a standard approach for reducing power when performance requirements vary.

A. DVS SYSTEM INTRODUCTION:

Dynamic voltage scaling is a power management technique in computer architecture, where the voltage used in a component is increased or decreased, depending upon circumstances [1-2]. Dynamic voltage scaling to increase voltage is known as Overvolting; dynamic voltage scaling to decrease voltage is known as Undervolting. Undervolting is done in order to conserve power, particularly in laptops and other mobile devices, where energy comes from a battery and thus is limited. Overvolting is done in order to increase computer performance, or in rare cases, to increase reliability. The term "overvolting" is also used to refer to increasing static operating voltage of computer components to allow operation at higher speed.

III. PROPOSED METHODOLOGY

A. DYNAMIC VOLTAGE AND THERSHOLD SCALING (DVTS):

DVS very well manages the dynamic switching power, with shrinking feature size the static (leakage) power has increased exponentially which it cannot control. Particularly, at low activity levels, leakage power is dominant. Dynamic voltage and threshold scaling (DVTS) manages both dynamic and leakage powers by adjusting supply voltage and body bias voltage. In digital circuits designed below 0.1 m, total power at any given performance can be optimized by DVTS.DVTS has been successfully proven on silicon for low power high speed applications. The optimum power point varies strongly with activity and temperature hence, it is necessary to locate optimum automatically [3]. To locate the optimum point, unlike in DVS, DVTS needs information about total power consumption of the circuit. In a DVTS closed-loop system is designed, where a feedback loop is used to maintain the ratio of for which power is optimum.

BLOCK DIAGRAM

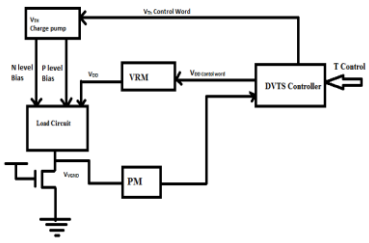

Fig. 1 Closed loop DVTS system

PM-power monitor
Vth-threshold value
VRM-voltage regulator module
T Cntrl-fixed control clock

Fig. 1 shows block diagram of closed loop DVTS system with *in-situ* power monitor [4]. DVTS controller implements the pro- posed DVTS algorithm and controls the supply voltage regulator and well bias charge pump. The drain of sleep transistor acts as a virtual ground node for the load circuit.The power monitor processes virtual ground voltage to generate a 2 bit output that gives information on total power consumed by the load. Control signal generator (CSG) generates control signals for power monitor when START signal is asserted. The delay monitor measures whether performance of load circuit meets the target performance within tolerance limit. Delay monitor is implemented with a critical path replica circuit [10]. The proposed DVTS system is suited for load circuits where the rate of change in activity is gradual.

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Reducing the clock frequency will proportionally reduce the total power. However, simply reducing the clock rate does not affect the energy consumed per operation [5]. The DVTS hardware tracks the optimal VTH for the given clock frequency by dynamically adjusting the VBB.

DVTS versus DVS

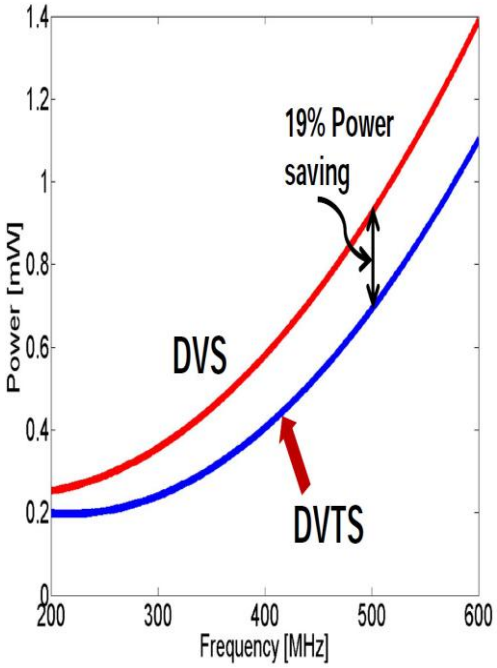

Fig. 2 70 nm technology (nominal VDD = 0.9 V, nominal VTH = 0.15 V) Power versus clock frequency for DVS and DVTS systems in different technology Generations.

The leakage power consists 52% of the total power, when the operating temperature was set as 125C°. By simply reducing the clock frequency, only the dynamic power can be reduced, leaving the leakage power virtually unchanged [6]. Since the leakage power is so high for scaled CMOS technologies, DVTS appears to be comparable to DVS in saving total power. From fig.2, 92% total energy savings can be achieved using DVTS for 70nm process technology.

Another merit that DVTS has for future technologies such as 70nm is the wide control of the power and delay just by adjusting the VTH. Fig. 3 shows that the VTH can be adjusted to its optimal value for a wide range of given clock frequency. Additionally, DVTS can substantially reduce the standby leakage power. Both the dynamic power and leakage power are lowered by either using DVS or DVTS. DVS will help reduce leakage power since the sub-threshold leakage and the leakage due to Drain Induced Barrier Lowering (DIBL), will decrease as the supply voltage is scaled down. Vice versa, DVTS can reduce the dynamic power by suppressing the short circuit current [7-8].

Nevertheless, DVS mainly reduces the dynamic power, and DVTS, the leakage power. DVS is not able to suppress the leakage power as much as the DVTS. Thus DVTS is more effective in reducing active and standby leakage power for future technology generations.

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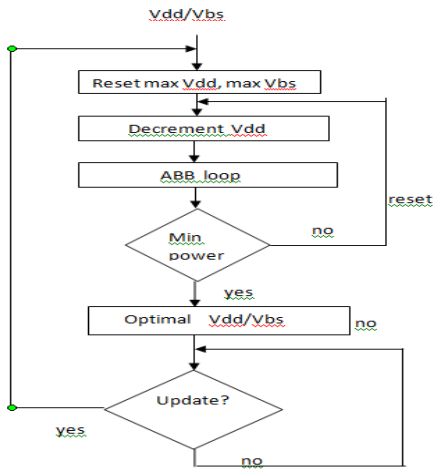
IV. DVTS SCHEME

A. DVTS Controller

DVTS controller implements the proposed DVTS algorithm and controls the supply voltage regulator and well bias charge pump [9]. Control signal generator (CSG) generates control signals for power monitor when START signal is asserted. The proposed DVTS system is suited for load circuits where the rate of change in activity is gradual.

B.DVTS Algorithm



The algorithm first sets the supply voltage to meet target performance, and then adjust well potential to achieve minimum power. NWell bias and PWell bias are always tuned by same amount and hence DVTS control loop is essentially a 2-D control loop. To avoid oscillations, loop and loop are decoupled by tuning them independently [12]. Initially maximum supply voltages and maximum forward bias are applied and the supply voltages are slowly lowered. At each step, the body bias is reset to maximum forward bias and locks to the target frequency to ensure that the chip stays functional. Once the minimum power point is detected, the bias values can be held in a register and the controller turned off. The loop can be reactivated whenever the workload changes, or periodically updated to reflect changes in temperature or operating conditions. Because the ASB loop does not have to be constantly running, the overhead power consumption, which is already amortized across the whole chip, can be reduced even further [11]. This ASB control loop is completely self-contained and should lock to the true minimum power configuration taking into account all possible current paths. This minimum will result in the physically lowest power consumption achievable by tweaking both and subject to the constraint that the chips satisfy a target frequency. Even for technologies where the theoretical limit is not yet achievable using body biasing techniques or in cases where excessive forward bias at low degrades performance, it is still possible to use this architecture to find the minimum physical power condition.

Advantages of DVTS OVER DVS

No voltage level converters:
DVS or multiple VDD systems require a voltage level shifter whenever a low VDD signal is driving a high VDD receiver.

Improvement in noise immunity:
Signal integrity has become an important issue for deep sub micron devices as crosstalk noise becomes considerable. Increasing VTH for low workload periods in DVTS will help improve noise immunity, especially for noise-susceptible circuits such as domino logic and pulsed flip-flops.

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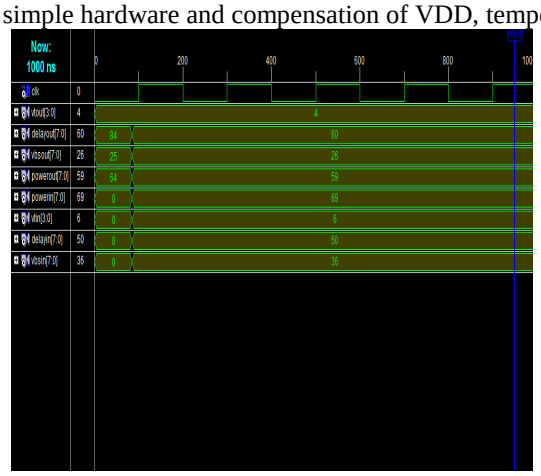
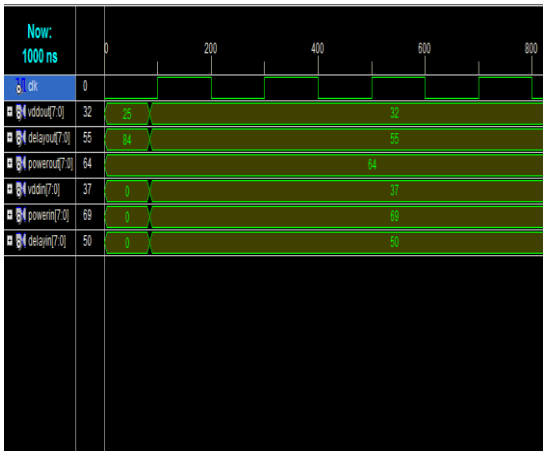
V. RESULT AND DISCUSSION

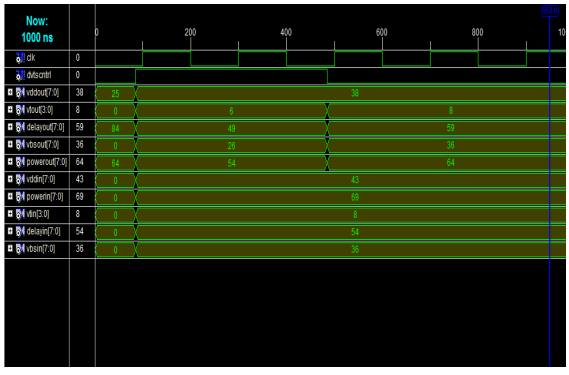
Dynamic VTH Scaling (DVTS) scheme is presented. The DVTS will become comparable to Dynamic VDD Scaling (DVS) in saving total power for future technologies such as 70nm.The DVTS has additional merits such as dramatic savings in standby leakage power, simple hardware and compensation of VDD, temperature variations.



V_{bs} Controller Result



V_{dd} Controller Result



DVTS Controller Result

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VI. CONCLUSION

A DVTS algorithm that can locate with varying activity is studied under simulation framework and validated with a test chip. Timing overhead of DVTS system and size of load circuit is analyzed as they limit the application of DVTS. Tracking performance of the algorithm can be improved by reducing the timing overhead. It can be inferred that for technology node with larger leakage currents, DVTS is more beneficial over DVS. To improve the accuracy, techniques to cancel the input offset voltage of difference amplifier can be employed. Also, with technology scaling the design of integrator can become challenging and hence, alternate integrator topologies (e.g., VCO) has to be researched.

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