ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 4, April 2015

A Review: Reconfigurable Processor for Binary Image Processing

Nikita S.Sakhare[1], R. K. Kulkarni[2]

PG Student, Dept. of E&TC, SKNCOE, Vadgaon (Bk), Pune, Maharashtra, India [1]

Assistant Professor, Dept. of E&TC, SKNCOE, Vadgaon (Bk), Pune, Maharashtra, India [2]

ABSTRACT: In many image and video vision applications, Binary image processor is very important processing operation. Binary image processor architecture contains input control logic, reconfigurable processing module, processor control unit and register group. The functional blocks of reconfigurable processing module, one is a binary compute unit which is mixed grained architecture, it provides high flexibility, efficiency, performances, less reconfigurable time and another is output control logic. This can perform basic binary morphological operations such as dilation, erosion, opening, closing. This paper illustrates the binary mathematical morphology operation and algorithm for edge detection by applying image difference technique, which indicates that processor, is suitable for binary image processing specially for mathematical morphological operation. This processor can be efficiently implement and synthesis using Spartan 3.

KEYWORDS: Field programmable gate array (FPGA), binary image processing, mathematical morphology, mixed grained, reconfigurable.

I.INTRODUCTION

Binary image processing system is very useful in many applications such as, motion detection, edge detection, object recognitions, shape recognitions, computer application, image analysis etc. Many researchers have been interested in vision a chip which provides properties such as compact size, high speed and low power consumption for performing parallel image processing. In today's life binary image processing system has been implemented using processor such as CPU or DSP but these processors are inefficient and difficult for complex mathematical operation or algorithm of binary image processing. Therefore to achieve high speed implementation of binary image processing operations, reconfigurable chips are used for binary image processing. In various image processing application, application-specific-chip (ASIP) and hardware have been proposed. This conventional chip with high resolution cellular logic processing array was developed to verify and enhanced fingerprint images.

ASIP provides more performance because they are optimized for a particular application and required instructions for a particular application can build on chip but it does not provide good flexibility.

A programmable single instruction multiple data (SIMD) vision chips removed the drawbacks of early general-purpose vision chip. This SIMD chip was presented for improving the parallel processing performances and real time applications. Many chips such as ASIP chip which has limited range and general purpose chips have its own problems, all these chips made of an analog circuit or digital circuit or both, when comprised these two parts which shows less accuracy, scalability and robustness.

Thus, a reconfigurable chip can be design with high performance, small size, and wide range application, which perform morphological operation. The processor chip used for wide application range which is compatible for binary image processing like motion detections, object tracking. Motion detections plays an important role in any surveillance system, it uses image differencing technique. All complicated binary algorithm and morphological operations can be easily implement on reconfigurable processor chip. In this paper using FPGA as a reconfigurable processor.
The rest of the paper is organized as follow; the section II describes literature survey in short. Section III illustrates the reconfigurable processing operations. Section IV describes morphological operation.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 4, April 2015

II.LITERATURE SURVEY

Many researchers have been implemented binary image processing on different types of processor such as DSP, CPU these processors are inefficient and difficult for complex mathematical operation or algorithm of binary Image processing [1,2,3].However for high speed implementation of binary image processing a application specific chip is realized. This chip is only used for a particular application. One application is to verify fingerprint images by implanting cellular-logic processing array [4], another application of a specific chip is motions detection using ModPod algorithm for simple operations [5]. The disadvantage of application specific chip is less flexibility. Due to the lacks of problems, these chips are made of analog circuit, and some are made of an analog part or digital part[6,7], while implementing analog part that result shows low robustness, accuracy, small area and low power consumptions. The general purpose processor chips have digital processor array architecture, in which each processor handles only one pixel. If large sized images are used, the chip becomes larger. Therefore to designs a chip with high speed, high performance, small size, A reconfigurable processor is presenting for binary image processing using morphological operations [8]

III. RECONFIGURABLR PROCESSING OPERATONS

As per pervious studied there various methods for binary image processing, this paper present one method for image processing using FPGA as reconfigurable processor. Reconfigurable processor is a microprocessor which has erasable hardware that can rewire itself dynamically. A processor which has erasable hardware such type of processor is called reconfigurable processor, due to this approach this processor is chooses for binary image processing.

The binary image processor architecture contains input control logic, reconfigurable processing module, processor control unit and register group. The functional blocks of reconfigurable processing module, one is a binary compute unit which is mixed grained architecture, which provides high performances, less time and another is output control logic. The core processor also has two bus interfaces, process control unit and register group.

The structure of reconfigurable binary processing module has been classified into two parts. These two parts of basic binary operations, first is output control logic which is used for selecting particular output from all binary compute unit outputs as per the input parameter and it also converts series binary images data into parallel data. Another part of processing module is binary compute unit which has mixed grained architecture that provides high flexibility, efficiency. Binary compute unit can easily solve the binary logic and binary image operations at very high speedily. In structure of binary compute unit, binary logic element plays important role which performs all logic gate operations like AND, OR NOT, NAND, NOR, XOR, XNOR. Structure of Binary compute unit has coarse grained architecture.

Input and Output control logic units are the blocks reconfigurable processing. In different image processing synchronizations is difficult task, due to this in reconfigurable processing input control logic is used for providing synchronizations between pixels in different images. Synchronizations is important before giving the input to the reconfigurable processing module. Output control logic unit is used to writes data parallel images into SDRAM. This unit writes data from reconfigurable processing module.

Process control unit is one of the main blocks of reconfigurable processing architecture. It is used for controlling the operation process of processing module, during the data access it also controls input and output control logic units, bus interfaces.

IV. MARPHOLOGICAL OPERATIONS

Binary morphological operation is one of the useful techniques used for binary-image analysis in computer vision. This type of binary image analysis is based upon binary Boolean operations like addition, subtraction and energetic set of system called mathematical morphology. The concept of mathematical morphology was coming from algebra and geometry.

The morphological concept is first started from the work of Matheron and sirra. Morphological concept was mostly used in binary image processing applications like motion detection, image feature extraction. Several binary image

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 4, April 2015

processing applications uses morphological operations and algorithms, motion detection, image feature extraction, such type techniques' are mostly used for wide range of applications in image processing and analysis. Mathematical morphology has two basic methods, which are dilation and erosion. This technique is used to despites set mathematical theoretic operations, like union, interaction by morphological operations. Dilation and erosion operation has two operands: first one is an image which is input signal and structuring element which represents image shape, size, and central location. Second operand of morphological operation like opening, closing. Hit-and-miss operation is one of the basic morphological operations; it is used for enhancing images by using basic operations, dilation and erosion.

Erosion – Suppose that X is the set of Euclidean coordinates corresponding to the input binary image and K is the set of coordinates for the structuring element. The erosion is defined by,

$$X \ominus K = \{ x \mid [(K)_x \subseteq X \} \quad 1$$

Where, K_x describes the translation of K so that its origin is at x and then the erosion of X by K is the set of all points x such that K_x is a subset of X. Erosion operation is used to remove salt noise in image. Erosion operation is mainly used for edge detection of an image and then subtracting it away from the original image , hence it highlights only those pixels at the edge of object that were removed by the erosion.

Dilation - Suppose that X is the set of Euclidean coordinates corresponding to the input binary image and K is the set of coordinates for the structuring element. The dilation is defined by,

$$X \oplus K = \{ x \mid [(K^{\wedge})_x \cap X \} \quad 2$$

Where, K_x describes the translation of K so that its origin is at x and then the dilation of X by K is the set of all points x such that the interaction of K_x with X is non-empty. Dilation operation is the dual of erosion. Dilation operation method is also used for edge detection by taking dilation of an image and then subtracting the original image , hence it highlights only those pixels at the edge of object that were added by the dilation. The hit-and-miss operation denoted by

$$X \otimes K = (X \ominus K_1) \cap (X^c \odot K_2) \quad 3$$

The noise filtering and bounty extraction both are simple binary morphological algorithms The noise filtering is defined by,

$$\{[(X \ominus K) \oplus K] \oplus K \} \ominus K = (X \circ K) \bullet K \quad 4$$

Opening – an opening binary morphological operation is defined as the an erosion followed by dilation using the same structuring element for both operations. Therefore, it requires two input, an image which is to be opened and structure element. Opening operation can be defined by,

$$X \circ K = (X \odot K) \oplus K \quad 5$$

Closing –The reverse operation of opening is nothing but the closing operation. It is defined simply as dilation followed by erosion using the same element for both operations, therefore it requires two inputs: an image to be closed and a structure element. This can be defined by,

$$X \bullet K = (X \oplus K) \ominus K \quad 6$$

Median filtering – In binary image processing there are several methods for removing noise such as salt and paper noise from images. Median filtering is effectively used in binary image processing, this filter works by removing through the image pixel by pixel, replacing one by one value with the median value of neighboring pixels.

VI. CONCLUSION

The binary reconfigurable processing architecture uses dynamics reconfiguration which increases performance of processor. The basic methods of mathematical morphological operation and algorithm can easily implement on field programmable gate array (FPGA). Thus using morphological operation like dilation, erosion, median filtering, it is simple and easy to implement edge detection morphological application on hardware Spartan 3.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 4, April 2015

REFERENCES

1. W. Miao, Q. Lin, W. Zhang *et al.*, "A programmable SIMD vision chip for real-time vision applications," *IEEE J.Solid-State Circuits*, vol. 43, no. 6, pp. 1470–1479, Jun. 2008.
2. A. Lopich and P. Dudek, "A SIMD cellular processor array vision chip with asynchronous processing capabilities," *IEEE Trans. Circuits Syst.I*, vol. 58, no. 10, pp. 2420–2431, Oct. 2011.
3. K. M. Shaaban, S. A. Ali, and Y. B. Mahdy, "A chip design for binary and binary morphological operations," in *Proc. Int. Conf. Inform. Intell. Syst.*, 1999, pp. 554–559.
4. K. Fujii, M. Nakanishi, S. Shigematsu *et al.*, "A 500-dpi cellular-logic processing array for fingerprint-image enhancement and verification," in *Proc. IEEE Custom Integr. Circuits Conf.*,May 2002, pp. 261–264.
5. H. J. Park, K. B. Kim, J. H. Kim *et al.*, "A novel motion detection pointing device using a binary CMOS image sensor," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2007, pp. 837–840.
6. R. Dominguez-Castro, S. Espejo,A. Rodriguez-Vazquez *et al.*, "A 0.8-μm CMOS 2-D programmable mixed-signal focal-plane array processor With on-chip binary imaging and instructions storage," *IEEE J. Solid- State Circuits*, vol. 32, no. 7, pp.1013–1026, Jul. 1997.
7. A. Zarandy, A. Stoffels, T. Roska *et al.*, "Implementation Of binary and gray-scale mathematical morphology on the CNN universal machine," *IEEE Trans. Circuits Syst. I*, vol. 45, no. 2, pp.163–168, Feb. 1998.
8. Bin Zhang, Kuizhi Mei," Reconfigurable Processor for Binary Image Processing", *IEEE Transactions OnCircuits And Systems For Video Technology, Vol. 23, No.5, May 2013*