Power Factor Correction of Fluorescent Lamp with Electronic Ballast Topology

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ABSTRACT: This paper focuses on the idea of a comparative study for different topologies of electronic ballast for power factor correction. The circuits presented are supposed to be high power factor single stage conversion electronic ballast to drive 36W fluorescent lamp. The work comprises of a half bridge inverter-LCC filter topology, a Class DE low dv/dt topology and Class DE current source driven rectifier. The circuits are designed and simulated using MATLAB/Simulink. The results were analyzed.

KEYWORDS: Power Factor Correction (PFC), Electronic ballast Class-DE low dv/dt rectifier, Class-D resonant inverter, dc side Class-DE resonant rectifier

I.INTRODUCTION

Electric lamps have now become the primary source of artificial illumination. They are preferred to other sources of illumination due to cleanliness, convenience, steady state light output and reliability. There are different types of lamps available and each type has special properties which make them suitable for specific application. In these days lighting adds up to a very big part of building maintenance rate. The energy consumption of domestic purpose amount to be more than 50% of lighting devices. So there lays the importance to focus on the efficiency of these lighting equipments. To obtain the maximum efficiency highest power factor correction is to be maintained in the lighting device

In order to achieve the high PF, the additional circuit named as ballast circuit is added between the supply line and discharge lamp. Magnetic ballast and Electronic ballast are the types of ballast circuitry. The disadvantage of magnetic core ballast is that the quality of light output is poor. In spite of that these ballast scheme does not enhance life of lamp. So the result is always flickering of lamp with short lamp life duration.Whereas electronic ballast offers full controllability of output.

This paper focuses on the idea of a comparative study for different topologies of electronic ballast for power factor correction. The power factor correction results in better efficiency of the discharge lamp and better quality output. The studied single stage structure comprises of a half bridge inverter in association with a LCC filter is directly connected to a half bridge rectifier. The numbers of components used in the circuit were less. [2].The use of bridge rectifier is discussed in the second topology. The input and output were analyzed [4].The current driving rectifier which is supposed to correct the power factor of the circuit is focused in the next topology [1].The ripple suppression of the current using LCC filter is taken for the first stage of analysis [3].The bridge rectifier function at the output side of the circuit is referred later [5].
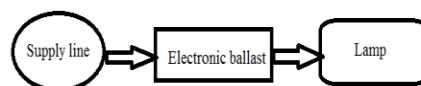

Fig.1 General Block diagram of electronic ballast

 The main function of the ballast is to guarantee lamp ignition and current regulation. It gets the supply from the line and ignites the lamp which is shown in Fig 1. It provides high voltage pulses between the lamp electrodes and limits the current that will circulate through the lamp.
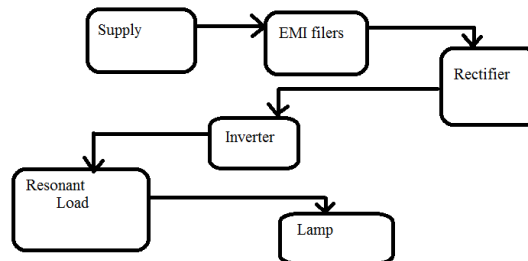
Fig.2 Block diagram of electronic ballast

The main problem of the two power processing circuits is the increasing number of components which results in high cost. In this comparative study single stage power conversion method is proposed. The single stage techniques are attractive for commercial applications. The electronic ballast circuitry usually consists of an EMI filter, power factor corrector, high frequency dc/ac converter and control circuitry and the operation sequence of the ballast is presented in Fig.2.

Fig.3 Output rectified lamp voltage as a function of load resistance

The lamp resistance is almost inversely proportional to its current. The general characteristic of the lamp is shown in Fig.3 Since the lamp exhibits a negative dynamic resistance, it should be driven by an ac source with a high output reactance to limit the lamp current and prevent lamp destruction from excessive current. Gas discharge lamps are normally operated from ac sources to equalize electrode wear, achieving longer life. The paper is structured as different section with introduction in section I. Section II is the analysis of different circuit and section III discusses design .The section IV shows the simulation results and discussion. Finally, section V presents the conclusion.

II.ANALYSIS OF CIRCUITS

The section comprises of a half bridge inverter-LCC filter topology, a Class DE low dv/dt topology and Class DE current source driven rectifier. The working principle operation is discussed for each topology with circuit diagram

A. Class D resonant inverter

The studied single stage structure comprises of a half bridge inverter in association with a LCC filter is directly connected to a half bridge rectifier. To analyze the feasibility of the idea LCC electronic ballast was designed for a 36w fluorescent lamp.
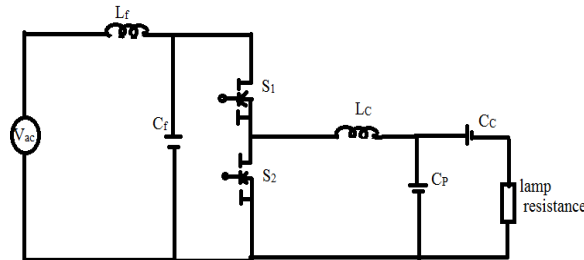
Fig 4.Half bridge inverter with LCC circuit

The analysis is simplified by assuming sinusoidal currents in L_c, C_P and R_p. The shape of the waveform is determined by the quality factor. The resistance R_p represents a load to which the ac power is to be delivered. A high capacitance dc blocking capacitor C_C prevents dc current flow through the R_P. The two bidirectional two quadrant switches S_1 and S_2 drives the resonant circuit L, C_P and R_p. The switches are turned on at nearly zero voltage reducing the turn on switching loss to a negligible value

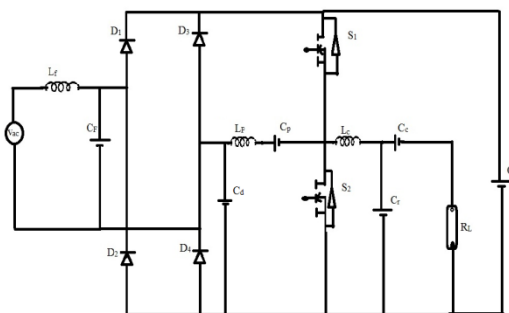### B. Class DE low dv/dt resonant converter

Fig.5 Class DE resonant rectifier topology

This topology introduces a new system of a single stage fluorescent lamps electronic ballast using Class DE low dv/dt rectifier for power factor correction. The circuit consists of EMI filters L_f-C_f, a bridge rectifier D1-D4, a high frequency charge storing capacitor C_d which is connected in parallel with bridge rectifier. A class D low dv/dt resonant converter is used for input current shaping which results in better power factor of the system. The switches usually exhibit zero voltage switching. The capacitor C_B is the bulk capacitor to reduce the ripples in the output from the lamp circuit. The output of the lamp will be rectified voltage output
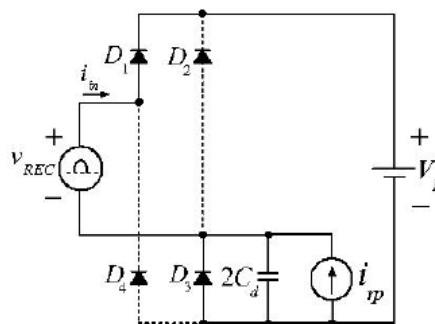

Fig 6. Equivalent circuit of the ICS with the ClassDE
Rectifier

This topology can be divided to two sections.-the input current shaping stage (ICS) and the inverter semi stage. The diodes D_1- D_4 are fast recovery diodes. The diodes in the diagonal turns on during positive half cycle and others turn on during negative half cycle. The output of the bridge rectifier will be rectified full wave sinusoidal voltage. The current

flows through the series inductor which shapes the current depending on the quality factor. If the value of quality factor is high, the current waveform will be close to sine wave which drives the Class DE rectifier
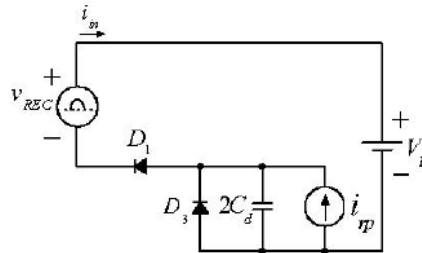

Fig.7 Equivalent circuit when D_1 is moved and voltage source V_{REC}

The voltage across bridge rectifier can be termed as V_{REC}. If the instantaneous value of V_{in} is positive and low then the average voltage $V_{in} - V_{REC}$ is high .The duty cycle D of the rectifier diode current becomes low. If the instantaneous value of V_{in} is positive and high. The average voltage $V_{in} - V_{REC}$ is low. The duty cycle of the diode current becomes high.

C. Class DE low dv/dt current driven source rectifier

The objective of this topology was to introduce low cost single stage electronic ballast with a dc side Class DE low dv/dt resonant rectifier to improve power factor in a more efficient manner. The rectifier is driven by a current source which is of high frequency. A class D series-parallel resonant inverter is included which gives a square output to drive the rectifier. As in the previous topology, it consists of EMI filters and bridge diode rectifier. The output of the bridge rectifier is a rectified output voltage. L_d- C_d is a matching network for the high frequency current source. The important characteristics of the CDESC-RPFC application is that the diode cycle, D_d is dependent on the load. The current flows through the diodes D_{DE1} and D_{DE2} when each diode is turned ON. The diode turns on at low dv/dt in order to reduce noise. Then it passes through the capacitors C_{DE1} and C_{DE2}. Thus the voltage across the diodes are shaped. The driving current i_d remains approximately constant for one switching cycle. The switching frequency is assumed to be higher than the line frequency.
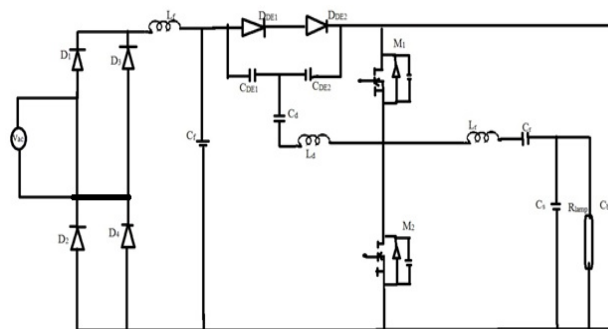

Fig.8 Class DE current driven source rectifier topology

In this concept of power factor correction, to achieve low line harmonics, the dc bus voltage V_B, should be higher than the line voltage. The EMI filter is inserted between the bridge rectifier arrangement and the bulk capacitor to improve the power factor. This ballast semi stage is same as that of Class DE resonant rectifier but the drawback is that it is not applicable to open circuit operations since $R_{LA}=\infty$

The diodes D_{DE1} and D_{DE2} with the capacitors C_{DE1} and C_{DE2} connected in parallel with them contributes for PFC. These are high frequency diodes. In addition to it, a matching network with an inductor L_d and C_d enhance the current flow to a sine waveform. The bulk capacitor C_b is charged by the Class D resonant rectifier and fed to the Class D series-parallel resonant inverter. Mosfet are used here for the switching action because of the anti parallel diodes in their body

for the operation above resonance. The series parallel resonant circuit consists of a resonant inductor L_r and capacitor C_r. The capacitor C_S acts as a dc blocking capacitor.

III. DESIGN PROCEDURE

The 36w electronic ballast is designed for a line rms voltage of 220v and the line frequency is 50Hz. Assuming that the total efficiency of the ballast is 90% and equal to 0.9η. The ballast draws a sinusoidal input current. The input power can be calculated as $P_{in}=P_{out}/\eta$. The amplitude of the input current to ballast draws a current equals to $I_{in}=I_o=\sqrt{2} \, P_{in}/V_{rms}$. The duty cycle at no load condition is D=0 which is the minimum duty ration value. The maximum of duty cycle is 0.5. But the distortion and voltage stress will be more for a maximum value so an immediate value which is less than D_{max} is taken that equals to 0.4. The switching frequency f_s is 84 kHz. The switching frequency is kept more than steady state resonance frequency and then the ZVS switching is ensured. The conduction angle of diode is Ø=0.628 rad/s. The minimum load value for the ballast circuit is also found out.

$$I_{in} = I_{O\max} = \frac{\sqrt{2}P_{in}}{V_{irms}} = \frac{\sqrt{2} \times 40}{220} \approx 0.257 \, \text{A}.$$
---------- (1)

$$\phi_{min} = \pi - 2\pi D_{d\max} = \pi - 2\pi \times 0.4 = 0.628 \, \text{rad/s}.$$
-------- (2)

$$R_{L\min} = \frac{V_B - V_{in}}{I_{O\max}} = \frac{327 - 311}{0.257} \approx 62.256 \, \Omega.$$
---------- (3)

$$f_s = \frac{0.661}{4\pi C_{DE} R_{L\min}} = \frac{0.661}{4\pi \times 10 \times 10^{-9} \times 62.256} \approx 84 \, \text{kHz}.$$
-------- (4)

Components used	Design values
RMS voltage	220V
Bus voltage	327v
Minimum load resistance	62Ω
Duty cycle	0.4rad/s
EMI inductor	5mH
EMI capacitor	209nF
Matching capacitor	100nF
Blocking capacitor	59.53μF
Resonant inductor	609mH
Matching inductor	430.01μH

Fig.9 Design value

IV. SIMULATION RESULTS

This work presented on the idea of a comparative study for different topologies of electronic ballast for power factor correction. The simulation results of the different topologies are presented and the results were discussed in this section.

A .Class D inverter topology

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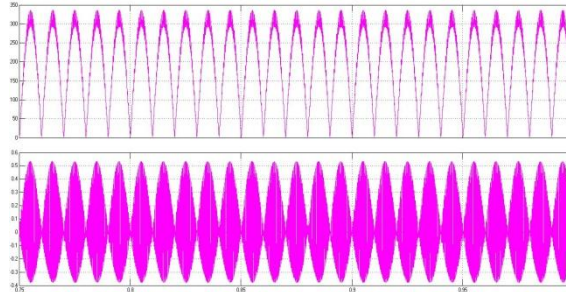
Fig.10 Simulated waveform of rectified output

Fig. 10 shows that the output of the class D inverter topology. The output from the circuit shows more ripple content. The ripple content should be minimized for better power factor of the system. The topology analysed constitute a half bridge inverter that can trigger the circuit but the current through the circuit comprises more ripple resulting in low efficiency and poor lighting
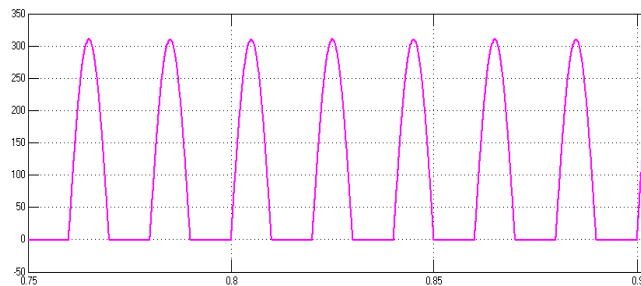

Fig.11 Output waveform from bridge diode rectifier

The figure 11 represents the waveform obtained from the input side of the circuit. The inductor and capacitor   is supposed to suppress the input ripple. Here a half rectified waveform is obtained.

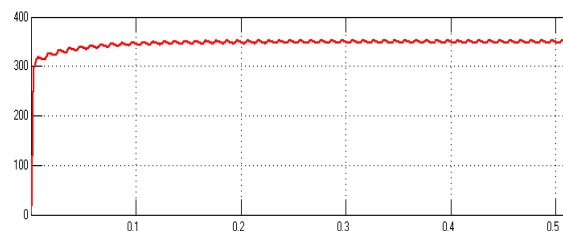## B. Class DE resonant rectifier topology

Fig.12   Rectified output from bridge rectifier

In Fig12, the rectified output of the bridge rectifier of class DE topology is shown. By comparing the output with the class D topology, the ripple content is low. The value is varies between 300v to 305v.
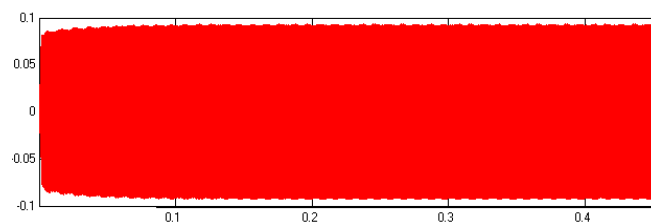

Fig 13.output current from the lamp circuit

The lamp current is constant which shows constant value at the output. So the topology represents better results

which reduced output ripple.

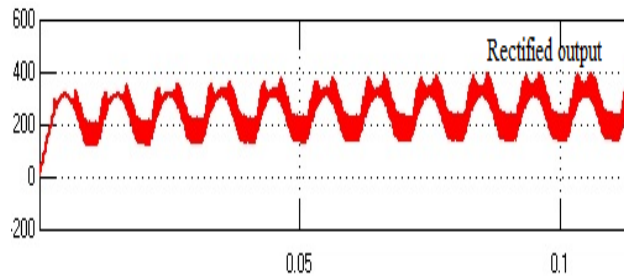### C. Class DE current source driven rectifier

Figure14 Rectified output from bridge rectifier

The figure 14 shows the rectified output from the bridge rectifier. By comparing the output from class DE rectifier circuit the output shows the rectified output more accurately. The value ranges to around 300v.
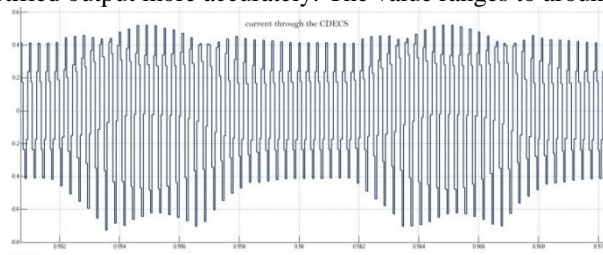

Figure15.Current through CDCSE-RPC

The figure 15 shows the waveform of the driving current which is supposed to correct the current flowing through the circuit. The current is regulated by the inductor L_d and C_d

D. Power factor calculation

The value of power factor depends on load of the circuit. Usually a fluorescent lamp consists of a resistive load. But a negligible value of inductance will be there in order to regulate the current. The load is more of resistive nature and that is the reason of lamp getting hot after a short duration. The value of resistance coil difference in case of materials used like silver coil, copper coil etc. The minimum load value is 62Ω with 3.08mH of inductance. An analysis table is made theoretically with different values of resistance and inductance for maximum power factor

Resistance	Inductance	Power factor
62 Ω	.080 H	0.90
62 Ω	.074H	0.91
62 Ω	.070H	0.92
62 Ω	.064H	0.93
62 Ω	.054H	0.95
62 Ω	.048H	0.96
62 Ω	0.041H	0.97
62 Ω	0.033H	0.98
62 Ω	0.029H	0.99

Table.2 Theoretical calculated values of Resistance and Inductance value for florescent lamp for various power factors

Resistance	Inductance	Power factor
62 Ω	0.029H	0.99
65 Ω	0.029H	0.98
70 Ω	0.029H	0.98
75 Ω	0.029H	0.98
80 Ω	0.029H	1.00
85 Ω	0.029H	0.99
90 Ω	0.029H	0.99
95 Ω	0.029H	0.99
100 Ω	0.029H	0.99

Table.3 Theoretical calculated values of different Resistance and Inductance value for florescent lamp for various power factors

Resistance	Inductance	Power factor
62 Ω	.080 H	0.90
62 Ω	.074H	0.91
62 Ω	.070H	0.92
62 Ω	.064H	0.93
62 Ω	.054H	0.95
62 Ω	.048H	0.96
62 Ω	0.041H	0.97
62 Ω	0.033H	0.98
62 Ω	0.029H	0.99

Table 3 Theoretical calculated different resistance value with different inductance value

VI. CONCLUSION

Class D series parallel resonant rectifier with low dv/dt circuit analysis gave more overall efficiency than the other class D and class DE configuration A control circuitry should be enhancing for the current regulation within the circuit. The class DE current source driven power factor correction rectifier represented a model of controlling the current flow within the circuit with diodes and capacitor. The high frequency current source exhibited a range more than steady state line frequency. It is assumed that additional control circuitry is neglected since the current inner loop contributes PFC. Theoretical analysis of load resistance for different values have been carried out.

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