ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 4, April 2015

Design of Area and Power Efficient Arithmetic and Logic unit

S.Rambabu[1], T.Mani pravallika[2], G.Divya[3], S.Karthik[4], K.Anil kumar reddy[5], B.Dineshgandhi[6]

Assistant Professor, Dept of E.C.E, Santhiram Engineering College, Nandyal, AP, India[1]

IV-B.Tech Student, Dept of E.C.E, Santhiram Engineering College, Nandyal, AP, India[2]

IV-B.Tech Student, Dept of E.C.E, Santhiram Engineering College, Nandyal, AP, India[3]

IV-B.Tech Student, Dept of E.C.E, Santhiram Engineering College, Nandyal, AP, India[4]

IV-B.Tech Student, Dept of E.C.E, Santhiram Engineering College, Nandyal, AP, India[5]

IV-B.Tech Student, Dept of E.C.E, Santhiram Engineering College, Nandyal, AP, India[6]

ABSTRACT: In this paper we presents a implementation of area and power efficient 4 bit Arithmetic And Logic unit (ALU) through concept of gate diffusion input (GDI) technique.ALU is most important and core component of CPU.ALU is also used as core component of number of embedded and micro processor systems.ALU consists of 4x1 multiplexer, 2x1 multiplexer, full adder .These are designed to implement different logical and arithmetic operations such as AND, OR, ADD, SUBTRACT etc. The 4x1 multiplexer, 2x1 multiplexer, full adder are implemented through GDI cells. These are associated to realize 4 bit ALU. The simulation is carried out based on MENTOR GRAPHICS 130nm technologies and compared with pass transistor and CMOS logic realization. The simulation gives that design of ALU through GDI is more efficient with low power consumption, occupies less surface area and faster compared with pass transistor and CMOS logic.

KEYWORDS: CMOS, Full adder, Mux, Power dissipations, ALU, Gate Diffusion Input logic

I.INTRODUCTION

Low power and High speed are the design trade-offs in VLSI industry. **Power consumption, area, speed, noise immunity** has emerged as a primary design constraints for integrated circuits (ICs). The VLSI designers always targets on three basic design goals such as minimizing the transistor count, minimizing the power consumption and increasing the speed. Most of the Very Large Scale IC (VLSI) applications, Full adder circuit is functional building block and most critical component of complex arithmetic circuits like microprocessors, digital signal processors or any ALUs. Almost every complex computational circuit requires full adder circuitry. The entire computational block power consumption can be reduced by implementing low power techniques on full adder circuitry. In this paper, from different existed base papers several full adder circuits based on different low power techniques have been proposed targeting Static CMOS gates are very power efficient because they dissipate nearly zero power when idle. Earlier, the power consumption of CMOS devices was not the major concern while designing chips. Factors like speed and area dominated the design parameters. As the CMOS technology moved below sub-micron levels the power consumption per unit area of the chip has risen tremendously.

In CMOS circuits, the power dissipation classified into **dynamic power dissipation, static power dissipation.** The dynamic power dissipation occurs when charging or discharging of load capacitances and establish path from vdd to gnd called as short circuit. The static power dissipation occurs by Sub threshold conduction when the transistors are off, Tunneling current *through gate oxide and Leakage current through reverse-biased diodes*In which ALU is implemented based on 2:1 MUX, 4:1 MUX, Full adder based on GDI Low power technique

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 4, April 2015

A. Proposed GDI Technique:

***GATE DIFFUSION INPUT* is a new existing method** to reduce power dissipation, propagation delay with less area proposed by Vivechana Dubey and Ravimohan Sairam (Refer page NO.6, IEEE2014). The GDI approach allows implementation of a wide range of complex logic functions using only two transistors. This method is suitable for design of fast, low-power circuits, using a reduced number of transistors shown in below

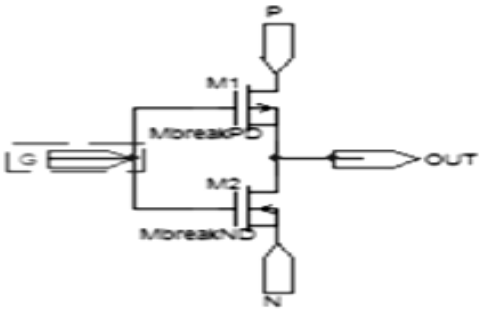


Fig: Basic GDI Cell

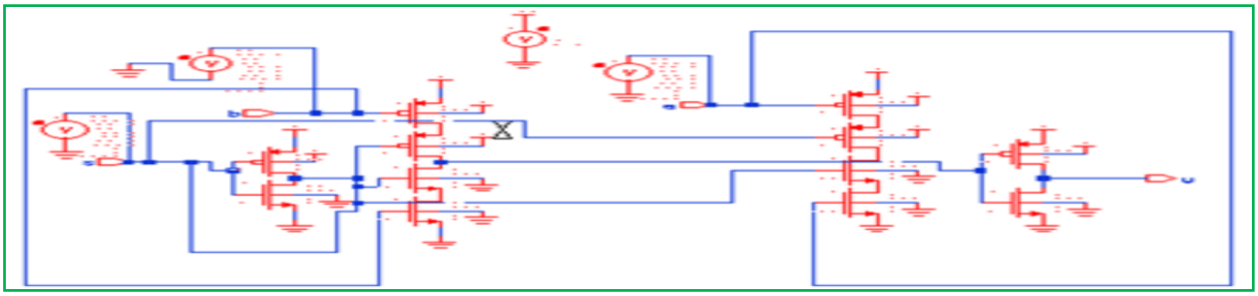
S.No.	N I/P	P I/P	G I/P	Output	Function
1.	0	B	A	A'B	F_1
2.	B	1	A	A'+B	F_2
3.	1	B	A	A+B	OR
4.	B	0	A	AB	AND
5.	C	B	A	A'B+AC	MUX
6.	0	1	A	A'	NOT

Table1: Instruction of Basic GDI Cell

In which, **full adder is designed with2- 4T XOR Gates and 2to 1 MUX .The simulation is carried out MENTORGRAPHICS on 130nm technologies**. An important feature of GDI cell is that the source of the PMOS in a GDI cell is not connected to VDD and the source of the NMOS is not connected to GND. Therefore GDI cell gives two extra input pins for use which makes the GDI design more flexible than CMOS design. But it adds noise in output logic levels by effect off delivered leakage power when transistor is off and degrades the performance of the system.

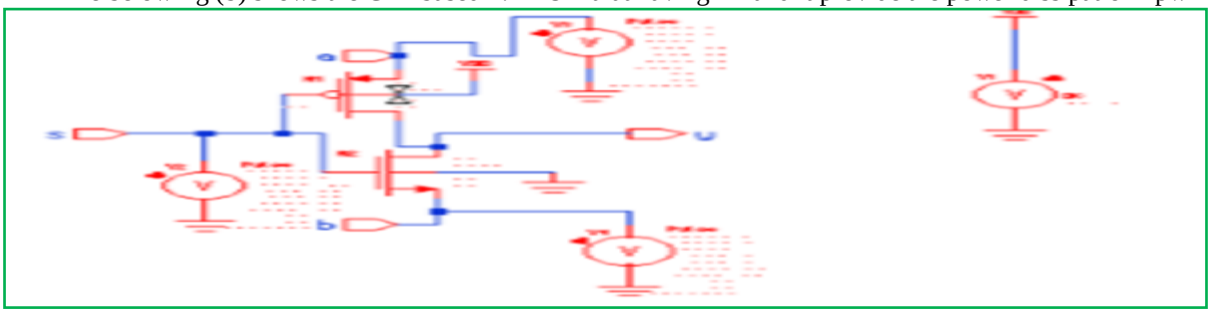
II. IMPLEMENTATION AND COMPARISON OFCMOS2:1MUXAND GDI 2:1MUX

The below fig(a)shows the CMOS based 2:1MUX that having 12T and it provide the power dissipation 296.59uw



Fig(a) **CMOS based 2:1MUXand**

The below fig (b) shows the GDI based 2:1MUX that having 2T and it provide the power dissipation 2pw



Fig(b) **GDI based 2:1MUXand**

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

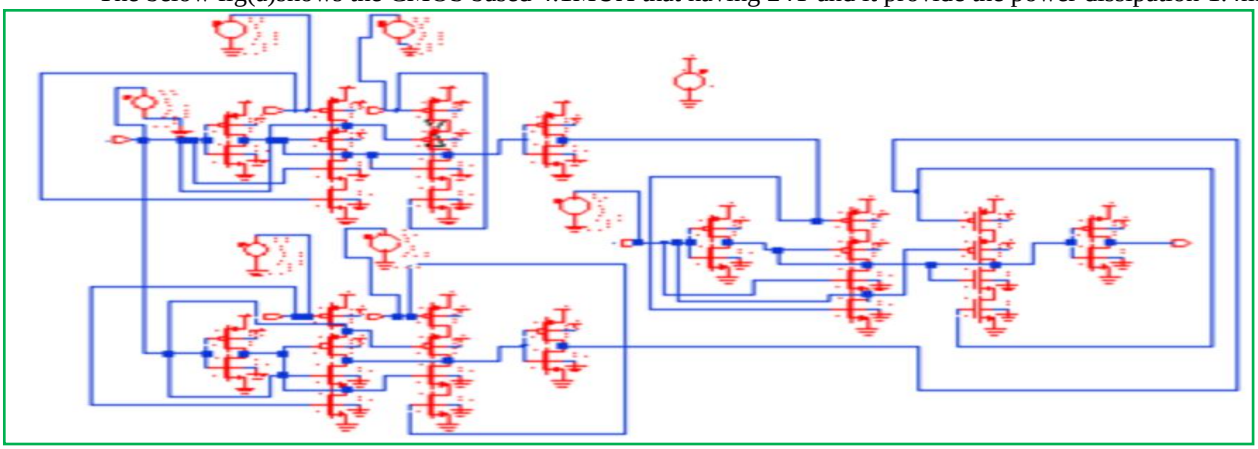
International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 4, April 2015

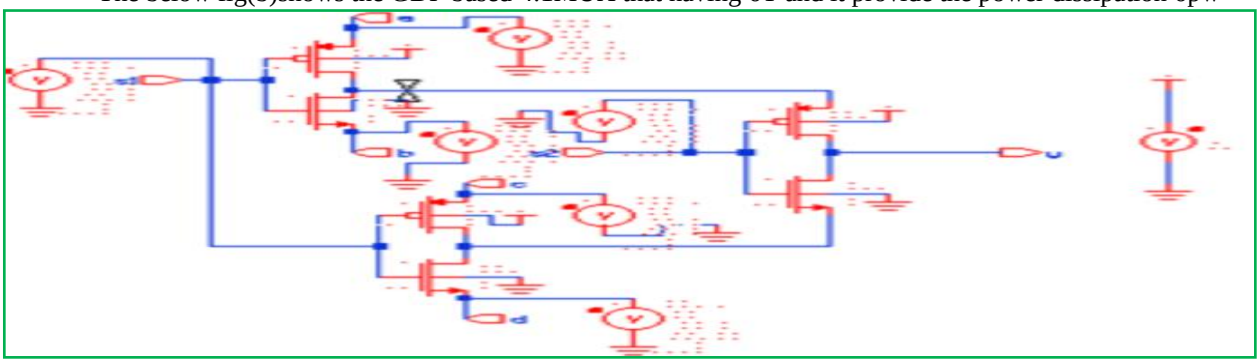
III. IMPLEMENTATION AND COMPARISON OFCMOS4:1MUXAND GDI 4:1MUX

The below fig(a)shows the CMOS based 4:1MUX that having 24T and it provide the power dissipation 1.4mw



Fig(a) **CMOS based 4:1MUXand**

The below fig(b)shows the GDI based 4:1MUX that having 6T and it provide the power dissipation 6pw



Fig(b)GDI **based 4:1MUXand**

IV. IMPLEMENTATION AND COMPARISON OF CMOS AND GDI FULL ADDER

The below fig(a)shows the CMOS based Full adder that having 28T and it provide the power dissipation 29.34nw

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 4, April 2015

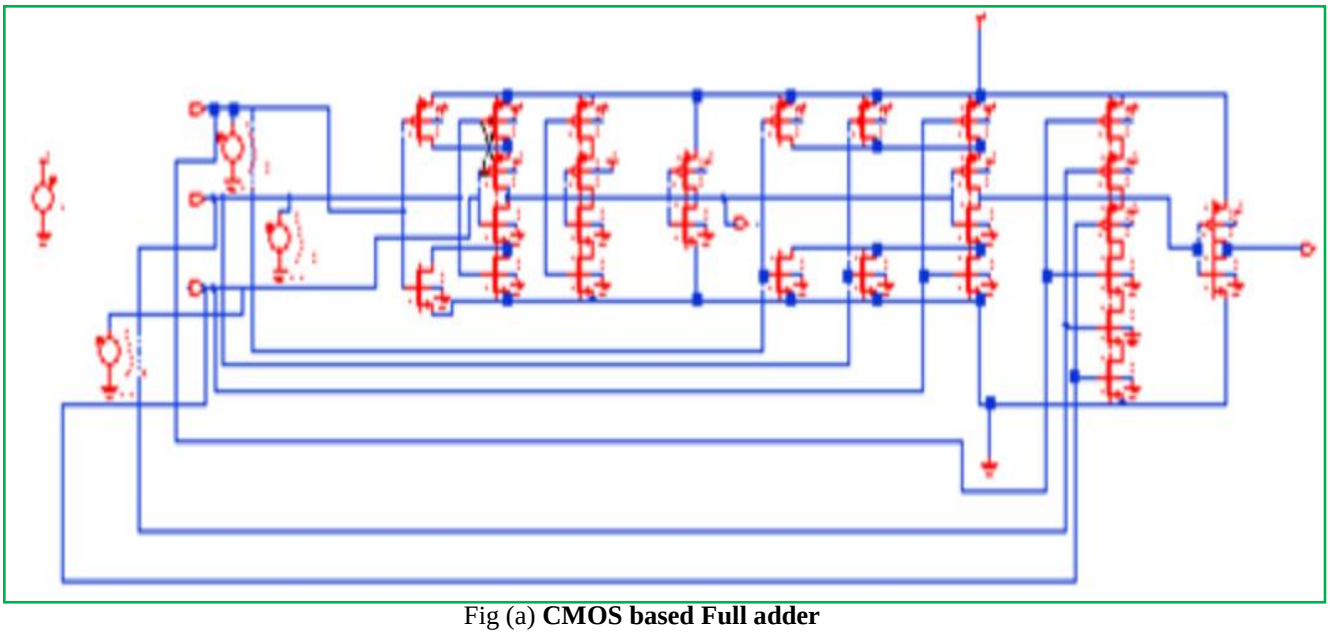


Fig (a) **CMOS based Full adder**

The below fig (b) shows the GDI based Full adder that having 10T and it provide the power dissipation 3.7nw

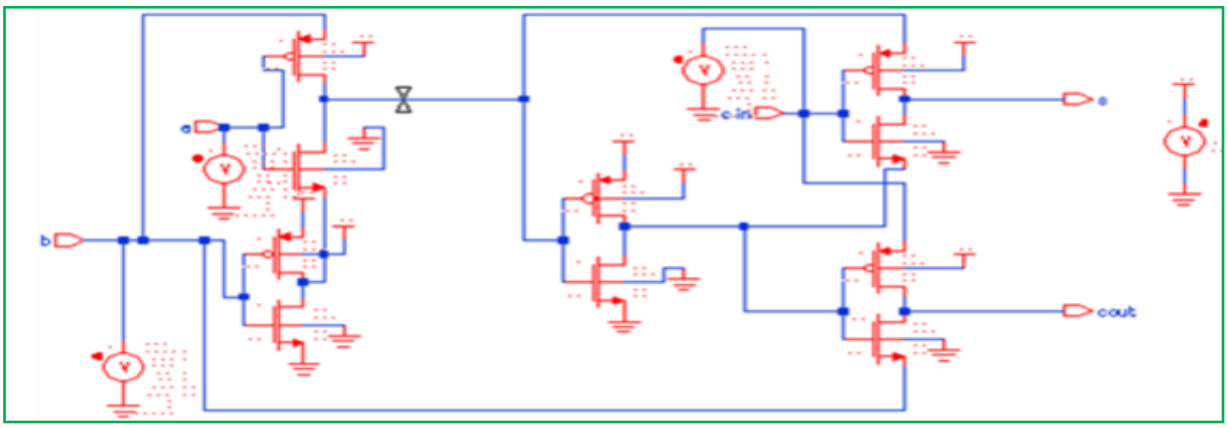


Fig (b) **GDI based Full adder**

V.GDI BASED ALU

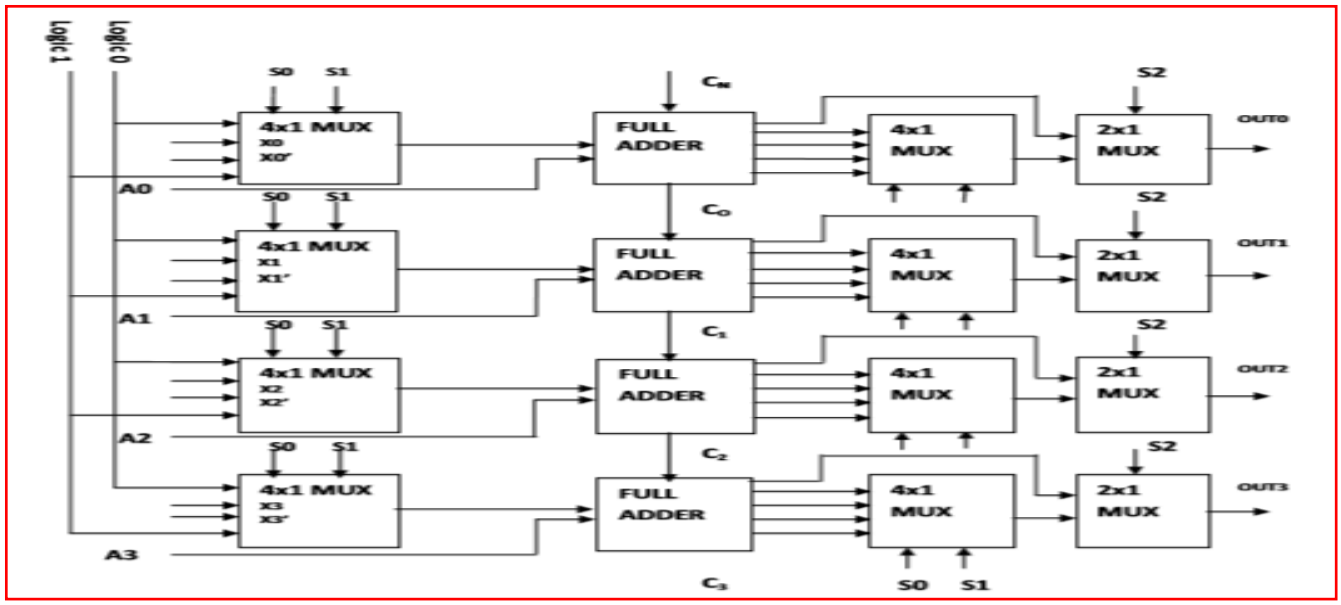
In which implemented ALU with four 2:1 MUX, eight 4:1 MUX and four Full adders based on GDI Technique shown in below fig

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

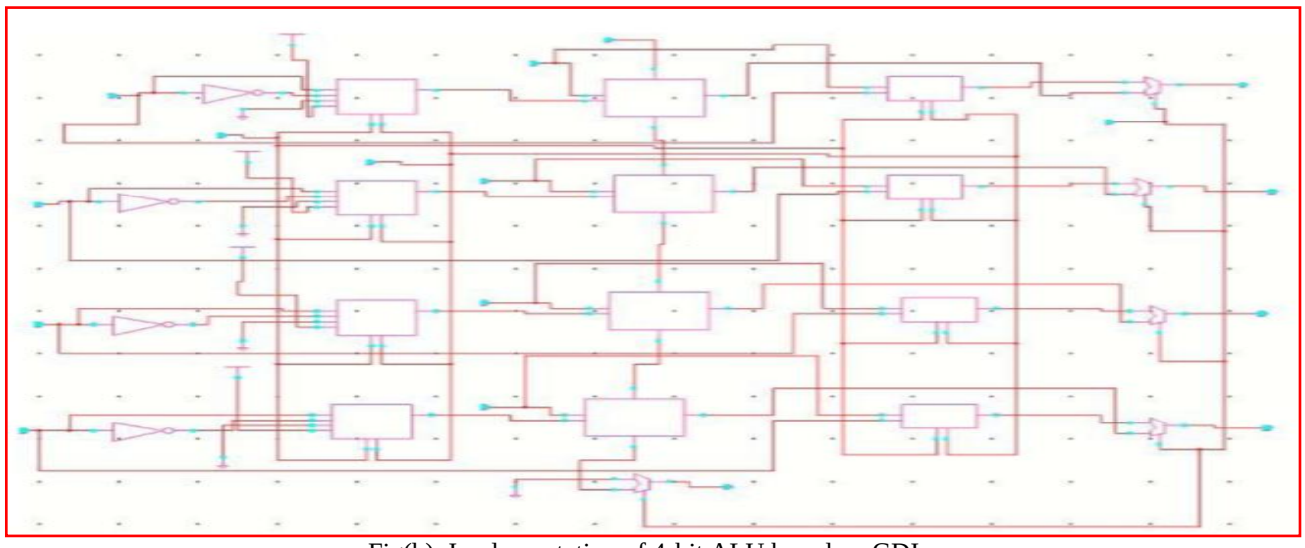
(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 4, April 2015



Fig(a): General structure of 4-bit ALU

The abow structure is 4-bit arithmetic logic unit implemented based on GDI technique. It provide very low power dissipation and occupied very less area compared to conventional based CMOS ALU shown in below comparison table



Fig(b): Implementation of 4-bit ALU based on GDI

VI. SIMULATONS RESULTS AND ANALYSIS

This section describes performance of the proposed design using MENTORGRAPHCS on 130nm technology. The simulated output of 2x1 multiplexer, 4x1 multiplexer and full adder is shown in aboveFigures.The number of transistor required and power consumption for the individual cells of the ALU is listed in table III and the total power consumption and number of transistor of the ALU designed in different ways is listed in table IV.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 4, April 2015

TABLE II. ANALYSIS RESULT OF DIFFERENT BLOCK OF ALU

DESIGN	CELL	POWER	No Of Transistors
CMOS	2:1 MUX	0.7mw	12
	4:1 MUX	1.4mw	24
	Full adder	29.3nm	28
	ALU	4204µw	592
GDI	2:1 MUX	2pw	2
	4:1 MUX	6pw	6
	Full adder	3.75nw	10
	ALU	1030.5 µw	232

VII. CONCLUSION

Power consumption in CMOS circuit is classified in two categorize: static power dissipation and dynamic power dissipation. In today's CMOS circuits static power dissipation is negligible thus not considered as compared to dynamic power dissipation. Dynamic Power dissipation in a CMOS circuit is given by P = CLf VDD2. The power supply is directly related to dynamic power. The numbers of power supply to ground connections are reduced in GDI implementation which reduces the dynamic power consumption. This work presents a 4-bit ALU designed in MENTORGRAPHICS on 130nm technology for low power and minimum area with GDI technique. The 2x1 multiplexer, 4x1 multiplexer, 1-bit full adder with 10- transistors designed using GDI technique is chosen for lowering power consumption and minimum possible area. Power dissipation, propagation delay and the number of transistors of ALU were compared using CMOS and GDI techniques. GDI technique proved to have best result in terms of performance characteristics among all the design techniques.

REFERENCES

[1]. R. Shalem, E. John, and L.K.John, "A novel low-power energy recovery full adder cell," in Proc. Great Lakes Symp. VLSI, Feb. 1999, pp.380–383.

[2]. A.Sharma, R Singh and R. Mehra, "Low Power TG Full Adder Design Using CMOS Nano Technology,"

[3]. L.Bisdounis, D.Gouvetas and O.Koufopavlou, "A comparative study of CMOS circuit design styles for low power high-speed VLSI circuits" Int. J. of Electronics, Vol.84, No.6, pp 599- 613,1998. Anu Gupta, Design Explorations of VLSI Arithmetic Circuits, Ph.D. Thesis, BITS, Pilani, India, 2003.

[4]. Saradindu Panda, N. Mohan Kumar, C.K. Sarkar., "Transistor Count Optimization of Conventional CMOS Full Adder & Optimization of Power and Delay of New Implementation of 18 Transistor Full Adder by Dual Threshold Node Design with Submicron Channel Length" in Computers and Devices for Communication, 2009. CODEC 2009. 4th International Conference on pp: I – 4

[5]. T. Vigneswaran, B. Mukundhan, and P. Subbarami Reddy," A Novel Low Power, High Speed 14 Transistor CMOS Full Adder Cell with 50% Improvement in Threshold Loss Problem" in World Academy of Science, Engineering and Technology 13 2006 pp: I-7.

[6]. T. Esther Rani, M. Asha Rani, Dr. Rameshwar rao, "AREA OPTIMIZED LOW POWER ARITHMETIC AND LOGIC UNIT" 978-1-4244-8679-3/11/$26.00 ©2011 IEEE.

[7]. Manish Kumar, Md. Anwar Hussain, and L.L.K. Singh," Design of a Low Power High Speed ALU in 45nm Using GDI Technique and Its Pe rformance Comparison, CNC 2011, CCIS 142, pp. 458–463, 2011.