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High speed variable length FIFO for POS PHY level-3

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ABSTRACT: Now-a-days a number of applications require very high-speed data processing like online banking, mobile banking, live streaming etc. This proposed work shows that how the variable length and high speed FIFO buffer provide large memory capacity for data packets. A FIFO that is small in size can't do justice with the transfer performance. Due to the fluctuation in the speed of network (sometimes failure of link) and real-time packet processing speed at the receiver, it is necessary to receive the complete packets of a frame to increase the throughput. This paper proposed a high speed and variable length FIFO scheme for high-speed data transfer. Also the target of this paper is over the good-put as well as throughput of the packet data.

KEYWORDS: FIFO, FIFO address pointer, Parallel SRAM, Variable mode, Normal mode, Quality of service, new flags.

I. INTRODUCTION

In the Internet Protocol (IP) network architecture, Synchronous Optical Network/Synchronous Digital Hierarchy (SONET/SDH) is used to transport information such as voice, data, and video. The Packet over SONET (POS) technology supports this transport mechanism and takes advantage of the existing SONET infrastructure. Implementing the POS technology involves direct mapping of the IP layer over SONET, thus, bypassing the ATM layer. The result is an efficient utilization of bandwidth with no ATM cell header, and the elimination of overhead associated with processing ATM cells such as IP encapsulation over ATM, and segmentation size, bandwidth efficiency can be as high as 99% and re-assembly (SAR) depending on the packet. The processing of information (packets) from the source to the destination traverses through layers of functional responsibility. In each layer, the processing of packets can be done with hardware, software, or both. The Lattice POS-PHY Level 3 PHY (PL3-PHY) Layer Interface-core is a highly-configurable core that provides hardware resources for data transfers between the PHY and Link Layer devices that support the POS technology. The majority of networked applications, application layer data frames are basically split into several smaller sized packets, before transmission across the network. The receiving side can make use of the data only if it receives all (sufficiently many to decode) packets of a frame. So it is necessary that a receiver should receive all the packets of frame and that is possible only when the good-put and also through-put of the FIFO buffer should be high. The depth of the FIFO buffer memory leads to delay if the proper interfaces have not done. This discussion tells that today high speed network has interpacket dependency architecture which leads "that we collect it but not got it". This leads us to find the new architecture for FIFO buffer for POS PHY level-3.

The standard FIFO depth of PL3 core is 256 byte, which is less whenever the network congestion or network failure exist. So the packet overflows or packet loss occurs due to low memory size. This scenario motivates us to work on POS PHY level-3 FIFOs architecture. Also the data requirement at any time is increases as the days going past, because no. of users and their usage requirements in form of data increase which leads to high speed data transfer. For example, subscriptions to live broadcasts over IPTV are expected to double and reach some 120 million subscribers worldwide by 2013, according to a recent survey by iSuppli Market Intelligence (2009). This trend motivates efforts for providing better algorithmic solutions to ameliorate network performance in [1] such scenarios.(http://www.isuppli.com/, 2009)

We proposed the High speed variable length FIFO scheme in which the length of FIFO's memory can be adjusted by the network condition. If network continuously read the data then we proposed normal memory mode of

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FIFO and if network not read the data then FIFO will become in variable memory mode. The memory mode of FIFO is dependent on the average push up and pop up speeds. The large memory associated with FIFO is the key for speed. The proposed FIFO will follow the smart algorithm to make decision for its length. The proposed work of this project is based on the hardware, means to design an efficient FIFO to avoid packet data loss and increase goodput and try to increase throughput also. Our concentration is over packet acceptance not the packet selection as other modern ongoing works.

II. RELATED WORK

Various aspects of providing traffic with Quality-of-Service (QoS) guarantees have been studied extensively. The works most related to our problem of packet forwarding with interpacket dependencies are set in the context of video traffic. Admission Control for Statistical QoS proposed by Shroff et al. [16] in which a buffer-less multiplexer introduces and they conclude economics of scale in the number of multiplexed flows was a crucial component in achieving a high degree of accuracy. They also experimentally observed loss curves (loss probability vs. buffer size) . Mehaoual et al. [2], in which a framework for the transport of real-time multimedia trace generated by MPEG-2 applications over ATM networks using an enhanced UBR best effort service (UBR+). Based on encoding MPEG.. They concentrated over minimizing loss of critical video data with bounded end-to-end delay for arriving cells and second, reducing the bad throughput crossing the network during congestion. Dynamic Extended Priority Assignment Scheme (DexPAS), an intelligent packet video drop policy named Nelissen et al [14], in which they suggested different types of switch implementations such as scheduler-based implementations provide a much better performance than the simple switch implementation. Girod et al.[4], in which they concentrated on a several recent advances for channel-adaptive video streaming. their techniques have the common objective of providing efficient, robust, scalable and low-latency streaming video. They conclude three things first, by allowing the client to control the rate at which it consumes data, adaptive media play-out can be used to reduce receiver buffering and therefore average latency, and provide limited rate scalability and secondly, rate-distortion optimized packet scheduling, a transport technique, provides a flexible framework to determine the best packet to send given the channel behaviors, the packets' deadlines, their transmission histories, the distortion reduction associated with sending each packet, and the inter-packet dependencies, thirdly, at the source encoder channel-adaptive packet dependency control can greatly improve the error-resilience of streaming video and reduce latency. [5] Chou et al. (2004), in which they introduce an incremental redundancy error-correction scheme that combats the effects of both packet loss and bit errors in an end-to-end fashion, without support from the underlying network or from an intermediate base station orderd to meet an average transmission- rate constraint while minimizing the average end-to-end distortion.

Stockhammer et al. [17], in which they worked on the separation between a delay jitter buffer and a decoder buffer is in general suboptimal for VBR video transmitted over VBR channels. They introduced a minimum initial delay and the minimum required buffer for a given video stream and a deterministic VBR channel. Katti et al. [15], in which they suggested COPE, a new architecture for wireless mesh networks. In which the addition to forwarding packets, routers mix (i.e., code) packets from different sources to increase the information content of each transmission are concluded. They show that intelligently mixing packets increases network throughput. Their design is rooted in the theory of network coding. They conclude that COPE can be used in multi-hop wireless networks that satisfy the Memory, Omni-directional antenna and Power requirements. Liu et al. [13], in which they suggested a performance analysis for the PCA protocol, considering the bursty nature of multimedia traffic. The mean frame service time and the mean waiting time of frames belonging to different traffic classes are obtained by them. Their model was applied to delay-sensitive traffic for QoS provisioning. They have focused on the interrelation between the AIFS mechanism specified in PCA and the burstiness/correlation properties in the multimedia traffic. Shi et al. [12] in which they suggested a MAC layer congestion control method to deal with wireless packet loss due to errors (as opposed to congestion). Their mechanism was implemented at the end wireless nodes based on the IEEE 802.11 DCF mechanism but without any modification to the TCP layer. Then they allow their congestion control mechanism to adjust its MAC congestion window based on the contention degree and the packet loss rate at the MAC layer. By improving the channel utilization and increasing congestion window for weak nodes, their mechanism improved the throughput performance and fairness performance significantly. Baiji et al. [3], in which they concluded the energy-efficiency and packet-loss trade-off at physical and medium access control layers. They show how energy-efficiency vs. packet-loss Pareto Frontier can be determined. They set E2 vs. packet-loss MOO problem at PHY and MAC layers and find PF - the set of all points with a property that there are no other points improving any objective without degrading another one.

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Scalosub et al. [7], suggested They combining these observations and give the following design criteria for competitive algorithms for the problem:-No-regret policy. Once a frame has a packet admitted to the buffer, make every attempt possible to deliver the complete frame.Ensure progress. Ensure the delivery of a complete frame as early as possible. To implement the first criterion, they will use a dynamic ranking scheme for the traffic. The second criterion takes form in the usage of preemption rules. The balancing between the two criteria is done by a definition of the delicate interplay between the ranking scheme and the preemption rules. They proposed a WEIGHTPRIORITY Algorithm, which follows the design criteria of above two policies. Liu et al. [9] in which they suggested RADA, a dynamic receiving buffer adaptation scheme for high-speed data transfer. RADA employs the receiver's memory utilization using a WMF. They suggested three scenarios as Single Transfer Scenario, Loaded Receiver Scenario and Multiple Transfers Scenario. Towsley et al. [18] in which they show how the burstiness of compressed video complicates the provisioning of network resources for emerging multimedia services. They also conclude for stored video applications, the server can smooth the variable-bit-rate stream by transmitting frames into the client playback buffer in advance of each burst. Copeland et al. [6] in which they stated that in the shared-memory switch architecture, output links share a single large memory. And also in logical FIFO queues were assigned to each link. They also suggested some buffer allocation policies, buffer sharing with Maximum Queue Lengths, SMA (sharing with a minimum allocation) and SMQMA (sharing with a maximum queue and minimum allocation). The above all sharing policies and also some dynamic policies as adaptive control and dynamic threshold related to buffer management scheme were introduced by them. Lin et al. [10], in which they suggested performance of the proposed FASNC scheme was evaluated by conducting a series of simulations using the QualNet simulator with a WiMAX module. In their work performance was evaluated in terms of the good-put, decoding delay and buffer requirements, and was compared with that of HARQ-CC (with chase combining), the optimal NCL scheme, and three N-in-1 ReTX schemes. The performance of the FASNC scheme with feedback periods of first, second, and fourth frames given transmitter buffer sizes ranging from 25 to 300 MPDUs. They also concluded the FASNC scheme switches adaptively between M-SNC and MGC on a frame-by-frame basis in order to effectively utilize the available TxOps.

III. PROPOSED MODEL

In the proposed FIFO model the two memory (dual port RAM) are connected with a decision making machine for selecting the RAM.

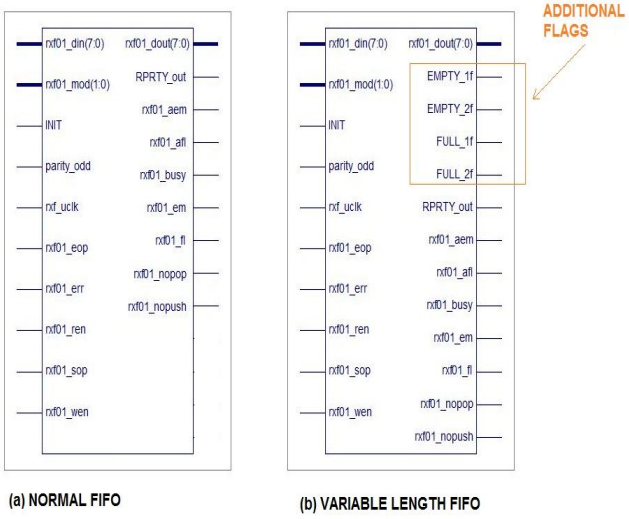

Fig. 1 Schematic block diagram of variable mode

The selection of memory is based upon the how much data is read from the FIFO by network. It can be seen from fig. 2 (a) and fig. 2 (b) in which normal and variable modes and are shown. FIFO The algorithm for variable FIFO is shown in fig. 3 in which Pointer addresses are used for switching between normal memory mode to variable mode and vice versa.

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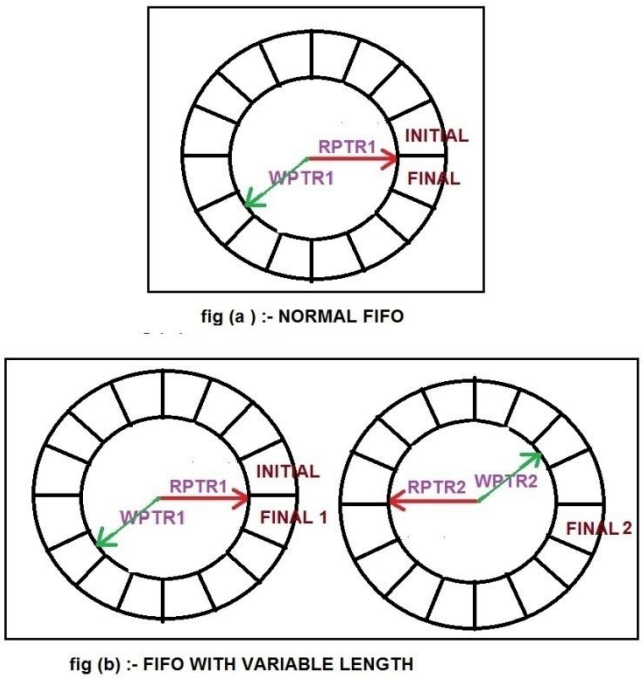

Fig. 2 Normal and Variable FIFOs

The schematic block diagram of normal FIFO and variable mode FIFO are as shown in fig. 1, in which inputs and outputs ports are shown.

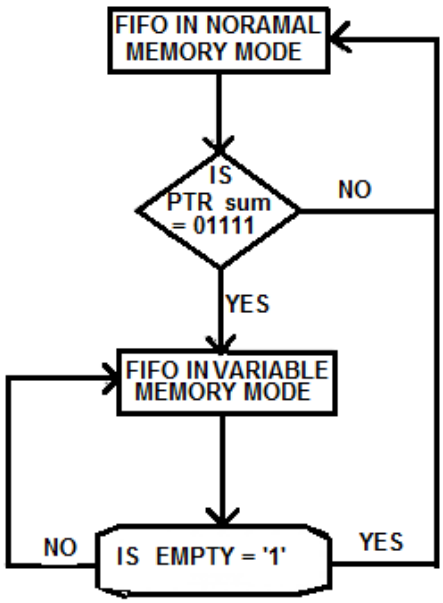

Fig. 3 Algorithm for variable length FIFO.

The variable mode FIFO has four additional flags for RAM1 and RAM2 memory status (EMPTY_1f, FULL_1f, EMPTY_2f and FULL_2f). The algorithm shows in fig 3 the packet counter of FIFO memory and the EMPTY flags

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are used for mode selection. Once FIFO enters into variable mode will not become in normal mode again until the EMPTY flag will high. This means if all the packets are pop from the FIFO will forced FIFO to normal mode.
The different read and write pointers are used for RAM1 and RAM2. This can be seen in fig. 2 (a) and (b).. The algorithm shown in fig 3 is for a 16+16 byte prototype (16 byte normal and 32 byte variable).

IV. SIMULATION RESULTS

This proposed FIFO is a prototype of 16+16 Byte means 16 Byte in normal memory length and then 32 Byte in variable length mode. Different input patterns are applied and tested by test bench waveform of Xilinx ISE 8.2i, which are discussed here.

A. Writing data into FIFO (Push)

Rxf01_sop=1 mark the start of data packets within the rxf01_wen = 1 and data packets writing into FIFO starts if rxf01_fl is '0'. The flags statuses are changed rxf01_em become '0' as shown in fig. 4.Rxf01_eop=1 mark the end of the packets and writing of data packets will stop after the current packet. The flags statuses are changed. If 32 Byte data are written into FIFO then rxf01_fl become '1'.

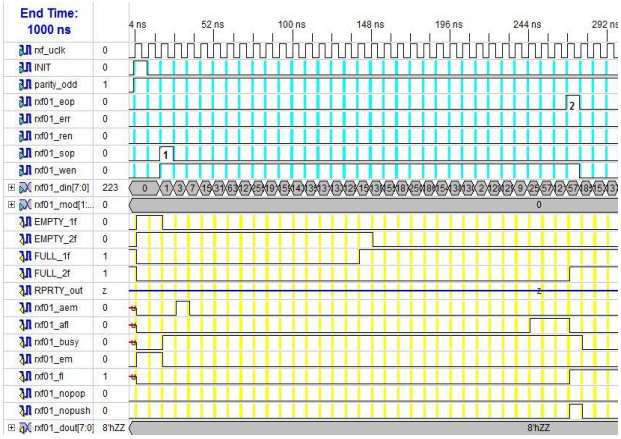

Fig. 4 Writing data packets into FIFO (push)

B. Reading data from FIFO (Pop)

After the writing process the reading process has done when rxf01_ren is asserted and rxf01_empty flag is '0' as shown is fig. 5. The reading process is going continuously till FIFO become empty means rxf01_empty = '1'. Flags are become in initial condition can seen from fig. 5.

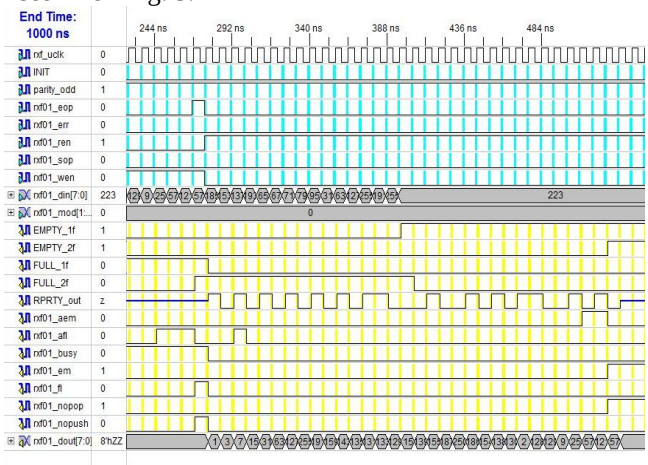

Fig. 5 Reading data packets from FIFO (pop)

Rxf01_parity bit will also available for each data pop up. When the writing process is going on then reading will not done.

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C. Packet discard ability when error occurred

When rxf01_err signal is asserted with rxf01_eop then all the flags and pointers of FIFO will become in initial condition and can be compared by marking line A and marking line 2 in fig. 6. The above process discards the received data. Then again if rxf01_sop is asserted within rxf01_wen = '1' and writing of data into FIFO will starts as shown in fig. 6. This can be evaluate by rxf01_dout [7:0] values as marked by 4 in fig. 6. So the packet discard ability when error is generated has been working properly.

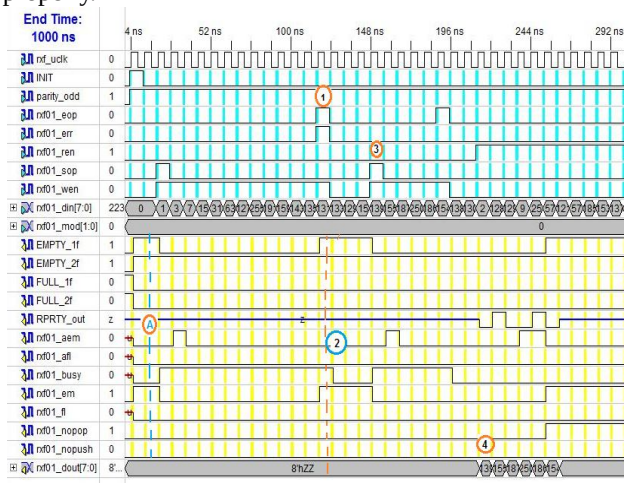

Fig. 6 Packet discard ability when error occurred

D. Writing speed/Reading speed

For writing and reading speed calculation the rxf_uclk is set to time period value of 8.0 ns means clock frequency of 125 MHz during the behaviour simulation using Xilinx ISE 8.2i. Here we are consider the data packet duration which is about 8.0 ns which can be seen in fig. 7 and then calculating the speed by mathematical formula.

Data rate = no. bits x clock frequency

Our proposed FIFO is for 8 bit data packet size. Data rate = 8 x 125000000 = 1 Gbps , (standard is upto 2.45 Gbps for 32 bit OC-48).

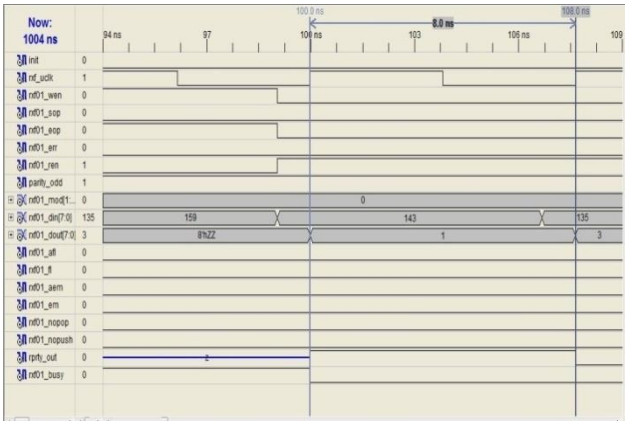

Fig.7 writing or reading duration.

E. Mode switching

The proposed FIFO is of variable length so it is necessary that the evaluation of the proposed work is also on the basis of mode. We are tested the FIFO for 32 byte continuous write operation as shown in fig. 8 in which marking 1 shows the initial status of flags. The proposed model has two RAM which are parallel connected and both have their own full and empty flags. These flags help us to understand the working of the FIFO mode switching. In marking one both RAMs are empty and in marking 2 RAM1 will full after which RAM2 is used to writing the data means the FIFO

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enters in variable mode and RAM2 no longer remain empty after that point. But the variable mode to normal mode switching is possible only when rx01_empty flag will set.

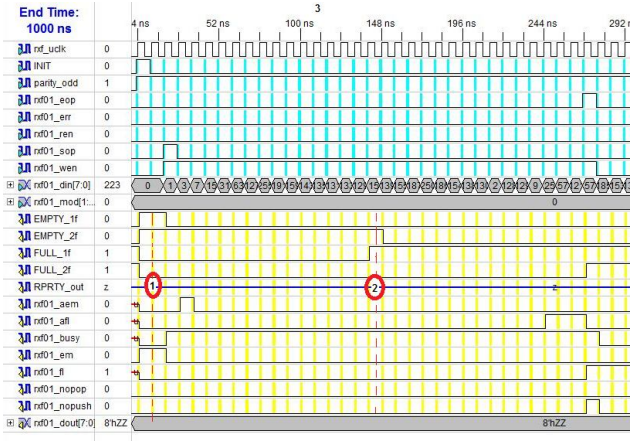

Fig. 8 Mode switching of proposed FIFO

F. Delay between write and read a particular data packets

The delay between a packet enters to the FIFO and retrieved from the FIFO is about 9.0 ns delayed which can be Seen from the fig. 9. In fig. 9 it is marked clearly for a particular data packet write and read.

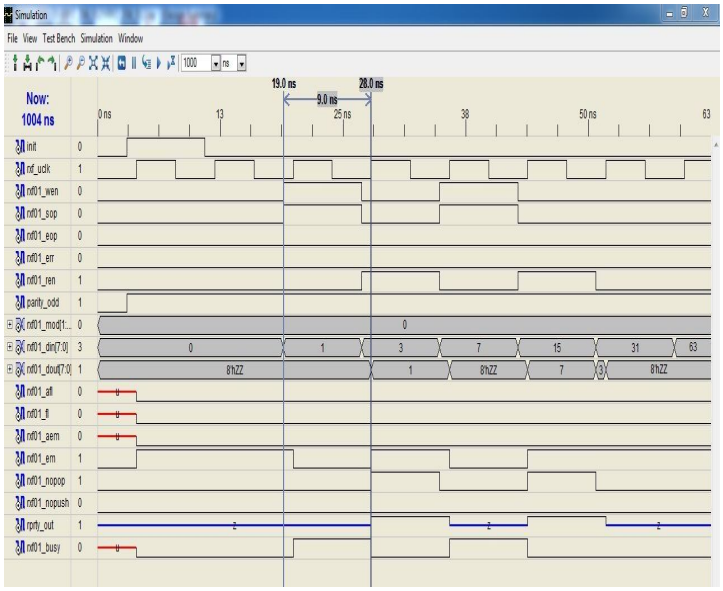

Fig. 9 Delay between write and read a particular data packets.

V. CONCLUSION AND FUTURE WORKS

In this paper we have seen the proper working of proposed FIFO. But the important thing in this paper is the modern high speed data requirements using internet links. The all high speed data links are evaluate on the basis of good-put and through-put of packets. In our proposed work we don't have any packet selection or discard algorithm when network congestion is occurred because our proposed model will accept all the data packets until its memory will not

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indicate the full signal. This leads that our proposed work will offer no doubt high good-put but can't surely say that it will offer high through-put. Our proposed work is tested for high clock frequency (125 MHz) compared to POS PHY level-3 clock (104 MHz standard) to check the high speed response in which the proposed work respond successfully. But the data rate will standard due to its dependency to PL3 core clock rxf_uclk which is 125 MHz for OC-48. The one important care is considered during the design procedure that reading till the Empty of memory is priority in our proposed work. Future works related to FIFO buffer has vast areas such as multi mode FIFO, Standby FIFO etc. This thesis encourages us to search for the better solutions to increase the through-put without affecting the good put. Will the current and future researches find the proper solutions?

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