ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 4, April 2015

A New Technique for Leakage Reduction in DSM Technology

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ABSTRACT: Leakage power is the major constant when scale down the technology in nanometer region. In this paper we propose a novel technique called LECTOR for designing CMOS gates which significantly cuts down the leakage current without increasing the dynamic power dissipation. In the proposal we use lector technique in different logics, we introduce two leakage control transistors (a p-type and a n-type) within the logic gate for which the gate terminal of each leakage control transistor (LCT) is controlled by the source of the other. In this arrangement, one of the LCTs is always "near its cut off voltage" for any input combination. This increases the resistance of the path from V_{dd} to ground, leading to significant decrease in leakage currents. Saving of power by proposed circuit is Basic Nand Gate 62.13%, Force Stack 91.11%, Sleep Transistor with Low V_{th} & High V_{th} 81.12% & 69.59%, with respect to sleepy Keeper 97.46% .

KEYWORDS: LCT, CMOS, Leakage Power, PDP.

I. INTRODUCTION

POWER dissipation is an important consideration in the design of CMOS VLSI circuits. High power consumption leads to reduction in the battery life in the case of battery-powered applications and affects reliability, packaging, and cooling costs. The main sources for power dissipation are: 1) capacitive power dissipation due to the charging and discharging of the load capacitance; 2) short-circuit currents due to the existence of a conducting path between the voltage supply and ground for the brief period during which a logic gate makes a transition; and 3) leakage current. The leakage current consists of reverse-bias diode currents and sub-threshold currents. The former is due to the stored charge between the drain and bulk of active transistors while the latter is due to the carrier diffusion between the source and drain of the OFF transistors.

Scaling down of threshold voltage results in exponential increase of the sub-threshold leakage current [5]. The supply voltage and threshold voltage scaling trends for Intel's microprocessor process technologies are discussed in [6]. It can be seen from Fig. 1 that the leakage power is only 0.01% of the active power for 1- m technology, while it is 10% of the active power for 0.1- m technology. There is a fivefold increase in leakage power as the technology process advances to a new generation. Projecting these trends, it can be seen that the leakage power dissipation will equal the active power dissipation within a few generations. Hence, efficient leakage power reduction methods are very critical for the deep-submicron and nanometer circuits.

II. LITERATURE REVIEW

In digital CMOS circuits power dissipation can be categorized into two types- Peak power and time average power consumption. Peak power being reliability issue determines both performance and lifetime of the chip. The voltage drop effects, caused due to the excessive instantaneous current flow through resistive power network, affect the performance of a design[3-4]. Due to the increased gate and interconnect delay. Due to these large power consumption, device over heat and become less reliable and also the lifetime of the circuits decreases. As a result noise margin are also reduced thus increasing the chance of chip failure due to crosstalk.

2.1 Average power dissipation

The average power dissipation in CMOS digital circuit consists of basically three types of power dissipations, namely:-

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- Dynamic (switching) power dissipation.
- Short circuit power dissipation.
- Leakage power dissipation.

Dynamic (switching) power dissipation

The power dissipation which occurs during the switching activity of a signal is known as dynamic power dissipation. In any digital CMOS circuits, the energy drawn from the power supply, which charges up the output node capacitance, causes the dynamic power dissipation.

Then

$$P_{avg} = \frac{1}{T}\left[\int_0^{T/2} V_{out}\left(-C_{load}\frac{dV_{out}}{dt}\right)dt + \int_{T/2}^{T}(V_{DD}-V_{out})C_{load}\left(\frac{dV_{out}}{dt}\right)dt\right] \quad \text{eq. (1)}$$

From the above equation we get the expression for average dynamic power dissipation as :-

$$P_{avg(dyn)} = \frac{1}{T}C_{load}V_{DD}^2 \quad \text{eq. (2)}$$

$$P_{avg(dyn)} = C_{load}V_{DD}^2 f_{clk} \quad \text{eq. (3)}$$

Where,

C_{load} = Total load capacitance connected to it's output node.
f_{clk} = The clock frequency.
V_{DD} = Supply voltage.

Leakage power dissipation

The main power contribution is CMOS technology is basically Sub-threshols Leakage and gate oxide leakage current is the dominant in nanometer regime.

a) Sub-threshols Leakage

Sub-threshold leakage current is very significant component of the leakage power and this current passes from drain to source through the channel [6-7]. The sub-threshold leakage current is caused basically due to carrier diffusion between the source and drain region of the transistor in weak inversion. For a particular MOS transistor whenever applied gate to source voltage is less than the threshold voltage of the transistor, there is no flow of current. Mathematically

When $V_{gs} < V_t$
$I_{ds} = 0$

b) Gate oxide tunnelling current

Tunnelling through gate oxide occurs because thickness of gate oxide layer is gradually reduced as technology is reducing[7]. The gate oxide tunnelling current is caused because of tunnelling of electrons through nMOS capacitor with a heavily doped n+ polysilicon gate and p type substrate.

2.2 Leakage Reduction Technique

a) SLEEP MODE APPROACH

One of the most commonly known traditional approaches for sub-threshold leakage power reduction in DSM Technology is the sleep approach [12-14]. In the sleep approach, we add PMOS and NMOS transistor known as sleep transistor in power supply and ground for cut of pull up and pull down network from supply voltage this type of technique is basically used for reduction of dynamic power dissipation [9]. These sleep transistors basically made circuit in ideal mode to save the power by removing them from power supply. Figure 2.8 shows the structure of sleep approach. The sleep transistors are turned on when the circuit is active and provide very low resistance in the conduction path so that circuit‟s performance will not affects due to these additional transistors [10].

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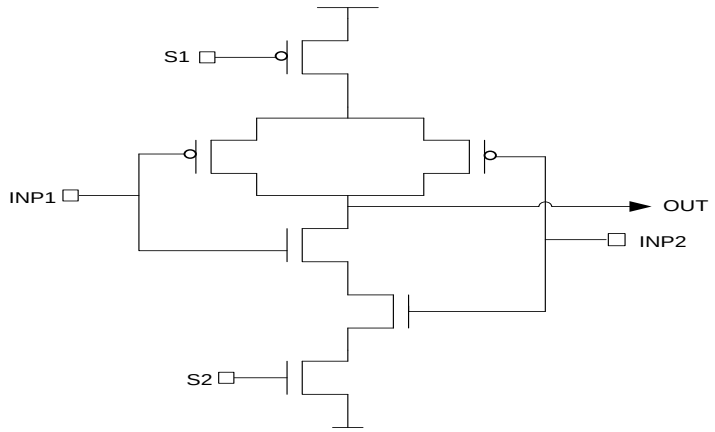

Fig.1. Sleep Approach NAND gate

b) STACK APPROACH

Another technique to leakage power by stack the transistor, which forces a stack help in exponentially reduction of Sub-threshold leakage by breaking down an existing transistor into two half size transistors [11]. The stack transistor arrangement is to increase the number of off transistor in stack. If two transistors are off instead of single off transistor highly reduces the leakage. The stack transistor and sleep transistor in each network are connected parallel which exponentially reduces I_{SUB} by maintaining proper W/L ratio of stuck transistor which means that circuit is in ideal state save the power consumption as shown in Figure 2.9 [12]. The main drawback of force stack approach is that we cannot use the High V_{th} transistor for further reduction of the leakage current. The stack approach show reduction of DIBL effect hence better leakage savings[13-12].

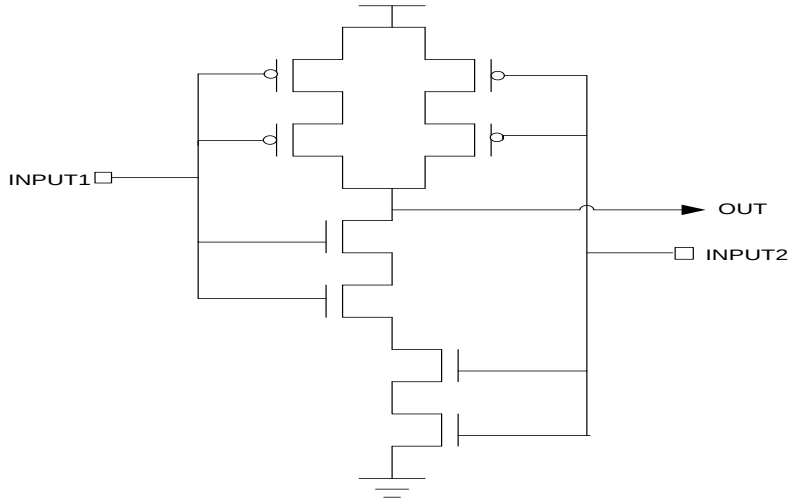

Fig.2. Stack Approach based 2 input NAND gate

c) SLEEPY STACK APPROACH

In his approach we are using stack approach which combine with sleep approach for better improvement of leakage current when one is in active mode another in sleep mode, as shown in Fig. 2.10. The sleepy stack technique divides existing transistors into two transistors each typically with the same width half the size of the original single transistor‟s width. Then sleep transistors are added in parallel to one of the transistors in each set of two stacked transistors; the divided transistors reduce leakage power using the stack effect while retaining state [15]. The drawback which come in force stack approach that we cannot use High V_{th} transistor, but with the help of sleep transistor we can use High V_{th} transistor for further leakage reduction[16]. By combining these two approaches, we have fruitful

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(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 4, April 2015

reduction of power consumption during sleep mode while retaining exact logic state. The penalty of this approach is increased area [14].

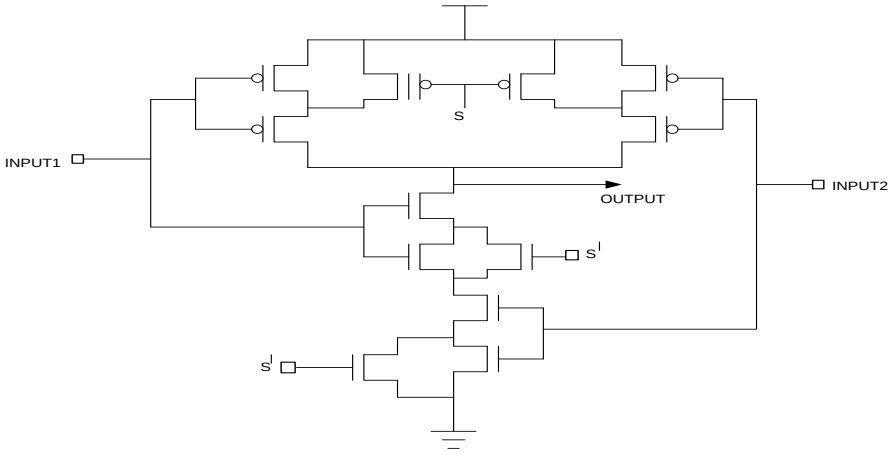

Fig.3. Sleepy Stack Approach based 2 input NAND gate

d) SLEEPY KEEPER APPROACH

Another leakage power reduction technique is the "sleepy keeper" approach. The structure of the sleepy keeper approach as well as its operation is described here. The basic problem with traditional CMOS is that the transistors are used only in their most efficient, and naturally inverting, way: namely, PMOS transistors connect to V_{DD} and NMOS transistors connect to GND [9]. It is well known that PMOS transistors are not efficient at passing GND; similarly, it is well known that NMOS transistors are not efficient at passing V_{DD}. However, to maintain a value of „1" in sleep mode, given that the „1" value has already been calculated, the sleepy keeper approach uses this output value of „1" and an NMOS transistor connected to V_{DD} to maintain output value equal to „1" when in sleep mode [7-8]. As shown in Figure 2.11,

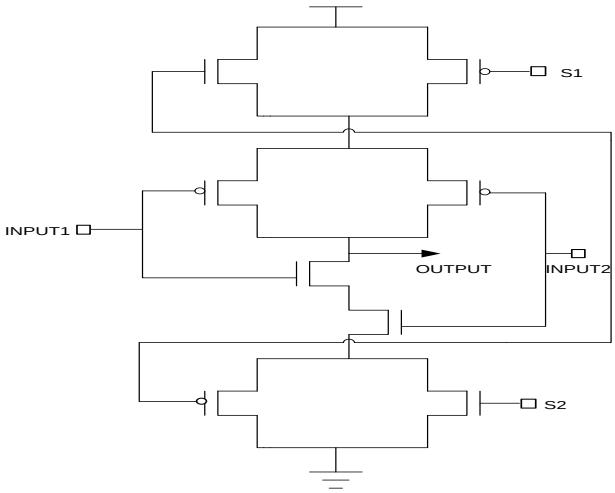

Fig.4. Sleepy keeper Approach based 2 input NAND gate

e) Lector Technique

Exploits an idea of an effective stacking of the transistors in the path from supply voltage to ground. Two leakage control transistor (LCTs) are introduces in each CMOS gate such that one of the LCTs is near its cut off region of the operation. Drawbacks like propagation delay and area overheads are overcome by transistor sizing and using SCCG gates for LECTOR (Leakage Control Transistor respectively. From arrangement of Structure of PMOS and NMOS (LCTs) always operates in its near cut off region. In the path of supply voltage more than one transistor is OFF in the

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LECTOR approach which mitigates leakage current flow in the circuit by providing proper stacking effect from V_{DD} to Gnd. The main drawback of this approach is that it does not provide proper logic at output level as shown in figure. 3.8. In this technique, two leakage control transistors are introduced between pull-up and pull-down network within the logic gate (pull-up and pull-down network) for which the gate terminal of each (LCT) is controlled by the source of the other. This arrangement ensures that one of the LCTs always operates in its near cut off region. The Lector is implemented in 2 input, 3 Input, 4 Input Nand Gate with the help of this we can implement this technique in Mux for Leakage and Power reduction.

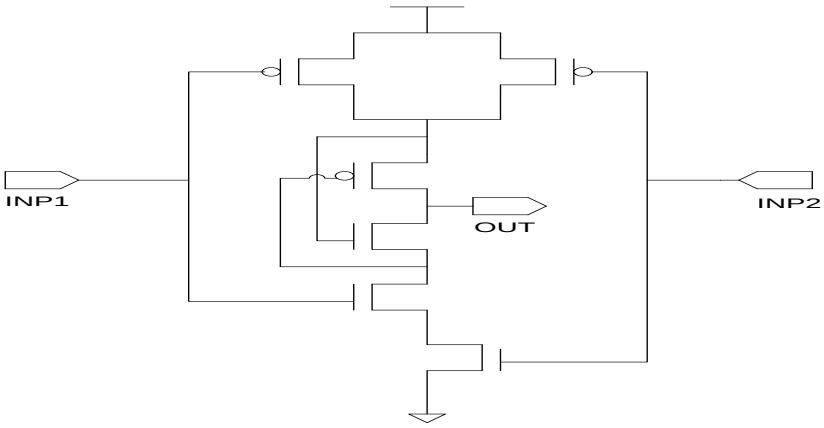

Fig.5. Lector NAND gate

III. Proposed Work

In this section, a new Modified Sleepy Keeper with Stacking of the Transistor with High V_{th} & Low V_{th} Transistor has been proposed. The proposed circuit is compared with well-known previous approaches, i.e., Basic NAND Gate, Forced stacking, Sleep transistor with Low V_{th}, Sleep transistor with High V_{th} & Sleepy Keeper. Firstly the proposed NAND gate circuit operation is explained. In sleep mode, the sleep transistors are off, i.e. transistor M1, M2 and Y_1,Y_2 are off. We do so by making S=0 and hence S'=1. Now see that the working of the basic NAND gate the output of the NAND gate is one either input is Zero with different combination of the input vector. In the proposed Circuit the utilization of the sleepy keeper Approach with Stacking of the transistor is incorporated for further reduction of the Leakage power in the circuit.

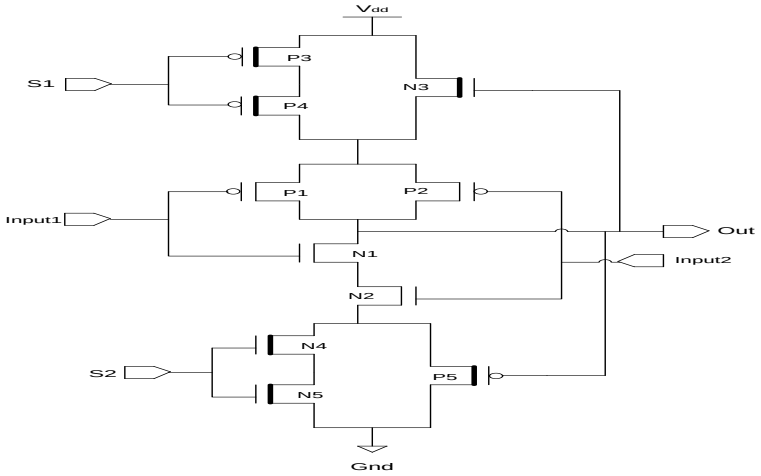

Fig.6. Proposed technique with high V_{th} transistors

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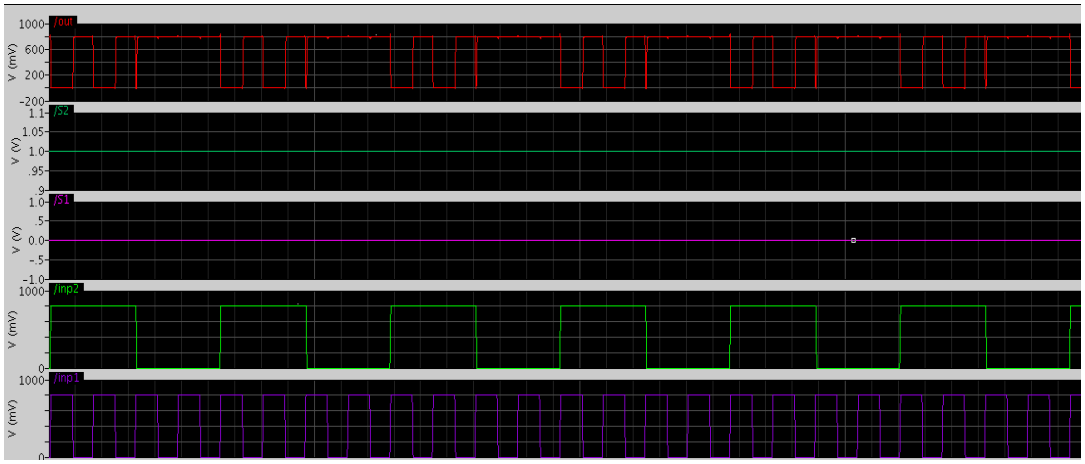

Fig.7.Output waveform of the proposed Circuit.

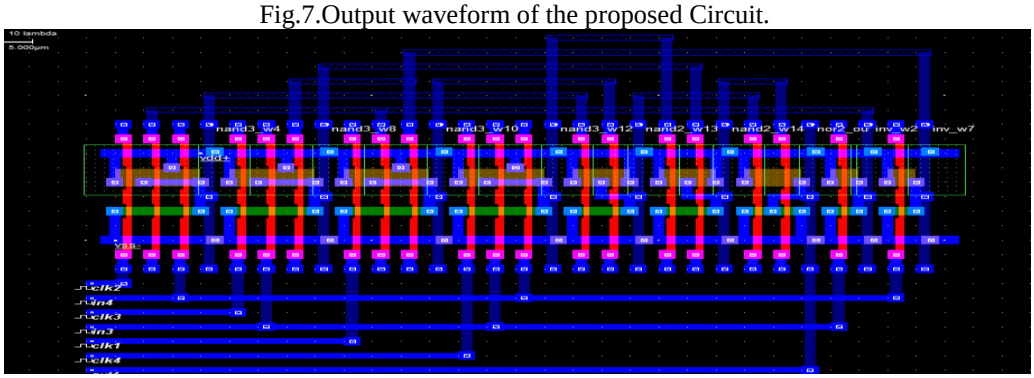

Fig.8. Layout Diagram of Proposed Circuit

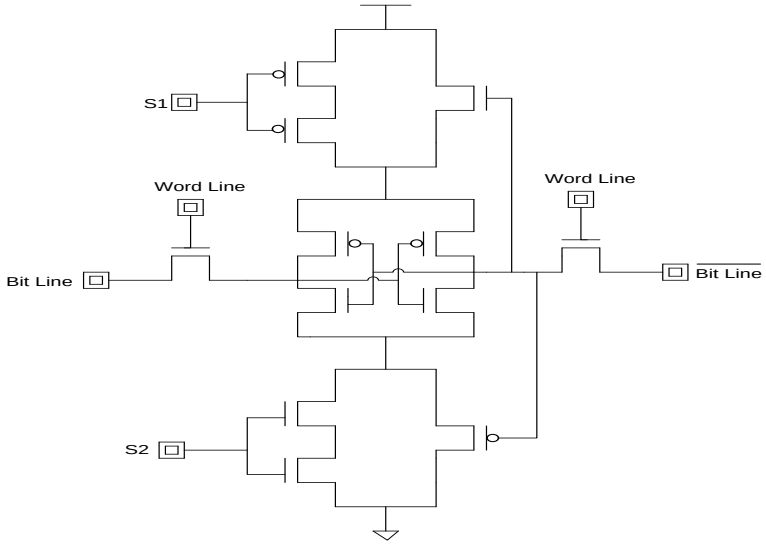

Fig.9. A SRAM cell in Proposed Approach

IV. RESULTS AND DISCUSSION

Simulation is performed of various leakage reduction technique like basic 2 & 3 input NAND gate, sleep approach, sleepy keeper and sleepy stack and proposed approach using BISM4 Cadence virtuoso with 1V supply at 65nm channel

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length for reduction of average power delay and calculation of leakage current. The circuits are simulated with high threshold and low threshold NMOS and PMOS transistors.

Table .1. Dynamic Power, delay & PDP Calculation of different Technique

Technique	**Average Power(uW)**	**Delay(ns)**	**Power Delay Product(PDP)**	**Static Power(ns)**
Base case NAND Gate	1.532	3.70	5.668	107.2
Forced stacking	2.49	9.76	24.30	7.869
Sleep Transistor with Low Vth	1.255	6.917	8.680	5.287
Sleep Transistor with High Vth	1.614	3.99	6.43	1.23
Sleepy Keeper	2.094	35.65	74.65	1.467
Lector With Sleep	1.213	2.61	3.165	1.141
Proposed Circuit with Low Vth	1.081	0.028	0.0302	1.032
Proposed Circuit with High Vth	0.921	0.081	0.0746	0.8149

Table.II. Dynamic power, Static power, Delay and PDP analysis of 4*1 Multiplexer

State	Dynamic power(nW)	Static power(pW)	Delay(pSec)	PDP(1E-21)
00	203.5	317	302.3	95.82
01	128.7	341.12	149.8	51.09
10	123.8	341	81.18	27.68
11	102.4	365	154.2	56.283

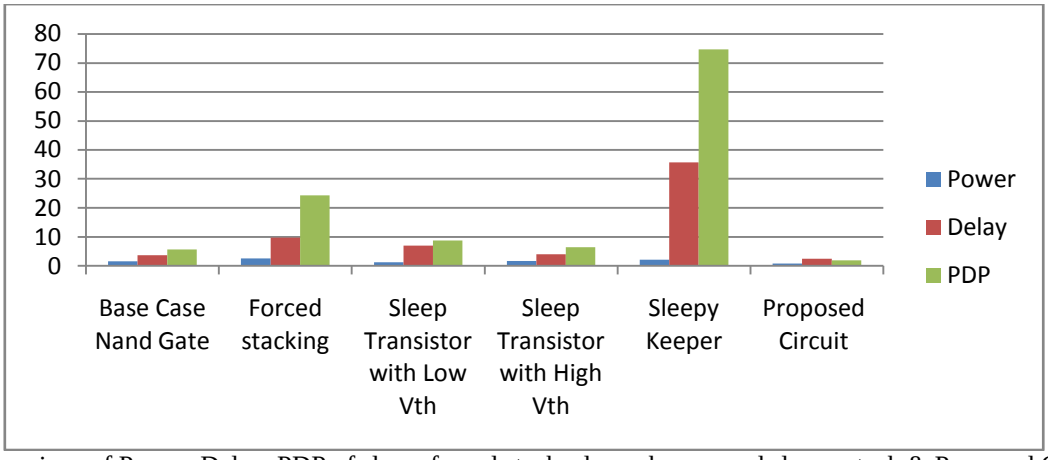

Fig.9. Comparison of Power, Delay, PDP of sleep, forced stack, sleepy keeper and sleepy stack & Proposed Circuit.

V. CONCLUSION

The research provides intense focus on leakage current/power analysis and next generation DSM technology. It reflects upon dominating face of leakage power dissipation such as I_{SUB}, I_{GATE}, and I_{BTBT} which are creating higher leakage in DSM VLSI design during idle mode. It proposes a technique for reducing the leakage current during idle mode of circuit. WLS Free Node algorithm uses four variants to effectively control I_{SUB} current of the device. This proposed algorithm gives better leakage reduction solution as compared with the other conventional and relevant techniques and

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(An ISO 3297: 2007 Certified Organization)

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there is no need of technology modification, no change of fan-out logic state of WLS gates during idle mode and needs no additional power supply. LECTOR method found more effective in both standby and active mode of operation. If propagation delay is taken as the performance metrics, then sleep transistor method is proved effective method in the standby mode.

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