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Highly Optimized APC-OMS Based Recursive Least Square (RLS) Adaptive Filter with Fast Convergence Rate

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ABSTRACT: The Recursive Least Square (RLS) adaptive filter is the most popular and widely used adaptive filter not only because of its simplicity but also because of its satisfactory convergence performance. Memory based structures are used in many kind of Digital Signal Processing (DSP) application. Memory-based structures are better performance in area minimization compare with multiply-accumulate structures and have many other advantages such as reduced latency. The Anti-Symmetric Product Coding (APC) and Odd-Multiple-Storage (OMS) techniques were used for Look-Up-Table (LUT) in adaptive FIR filter. Memory-based structure such as APC and OMS techniques are used for efficient low power design using LUT partitioning. Hence, the combination of these two techniques provides reduction in LUT size to one-fourth in adaptive FIR filter when compared with the conventional Look -Up -Table (LUT) of adaptive FIR filter.

KEYWORDS: Anti-symmetric product coding, Odd multiple storage, Look-up-table, Recursive least square ,Adaptive FIR filter.

I. INTRODUCTION

A conventional look-up-table (LUT)-based multiplier is shown in Table.1, where A is a fixed coefficient, and X is an input word to be multiplied with A. Assuming X to be a positive binary number of word length L, there can be $2L$ possible values of X, and accordingly, there can be $2L$ possible values of product $C = A \cdot X$.
Therefore, for memory-based multiplication, an LUT of $2L$ words, consisting of pre computed product values corresponding to all possible values of X, is conventionally used. The product word $A \cdot Xi$ is stored at the location Xi for $0 \leq Xi \leq 2L - 1$, such that if an L-bit binary value of Xi is used as the address for the LUT, then the corresponding product value $A \cdot Xi$ is available as its output.

A. LUT's in FPGAs

Three ways of using RAM blocks as multipliers are available. They are basic single look-up table multiplier, partial product multiplier, and RAM based constant coefficient multiplier. For the Accelerator devices, the single look-up-table approach can create a very fast, but narrow, 4-bit multiplier.

B. Basic Look-Up Table (LUT)-Based Multipliers

A basic LUT-based multiplier is simply a look-up table with the addresses arranged so that part of the address is the multiplicand and the other part is the multiplier. The data width should be set to the sum of the address width to accommodate the product.

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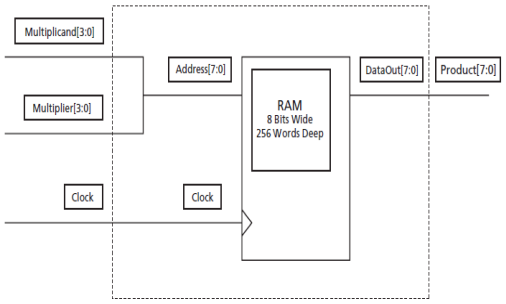

Fig.1 Storage and Demonstrates A 4×4 Bit Multiplier

Since the memory block in the accelerator is synchronous, this configuration will result in a synchronous multiplier. The multiplier's clock frequency is only limited by the data access time of the memory. This approach is more efficient than implementing multipliers in gates, but it can consume a large amount of memory. The amount of memory required increases with the square of the bit width.

C. PARTIAL PRODUCT MULTIPLIERS

One way to mitigate the amount of memory required is to use partial product multiplication. This technique combines the look-up table approach with elements of longhand multiplication. For example, to multiply 24 × 43 = 1032 using longhand, we simplify the problem into the sum of 4 multiplication functions and three addition functions (4×3 + ((2×3) ×10)) + ((4×4) + ((2×4) ×10) ×10) = 1032.

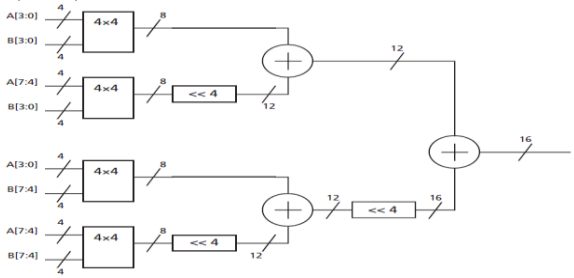

Fig. 2 Constant Coefficient Multiplier

D. CONSTANT COEFFICIENT MULTIPLIER

A third approach to using memory blocks as multipliers is employing a constant coefficient multiplier. In many cases, especially in Digital Signal Processing (DSP) applications, the multiplicand remains constant and only the multiplier varies. Although can create a constant coefficient multiplier using pure logic, implementing this function in RAM creates a much faster multiplier and uses very few logic gates.

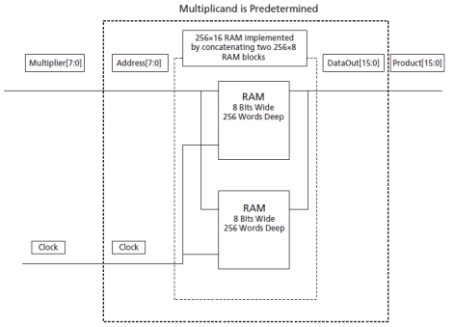

Fig.3 Block of 256×16 Bit Words

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This type of multiplier scales linearly with the width of the values being multiplied. While a basic look-up table 8×8 multiplier uses one block of 65536×16 bit words, 128 Kbytes of storage, and the partial product look-up table multiplier uses four blocks of 256×8 bit words, 1 Kbyte, the constant coefficient multiplier requires only one block of 256×16 bit words, 0.5 Kbyte, and does not incur the cost of the additional logic and delay incurred by using the partial product multiplier.

II. DESIGN METHODOLOGY

A. APC FOR LUT OPTIMIZATION

In addition, the sum of product values corresponding to these two input values on the same row is 32*A*. Let the product values on the second and fourth columns of a row be *u* and *v*, respectively. Since one can write $u = [(u + v)/2 - (v - u)/2]$ and $v = [(u + v)/2 + (v - u)/2]$, for $(u + v) = 32A$, we can have

$$u = 16A - \left[\frac{v-u}{2}\right] \quad v = 16A + \left[\frac{v-u}{2}\right].$$

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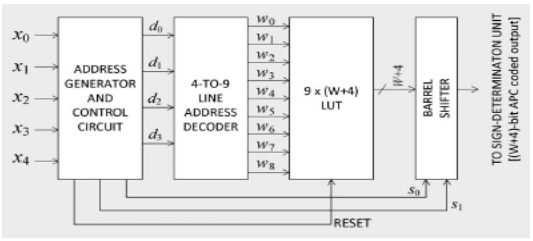

Fig.4 Proposed APC–OMS combined LUT design

Product word = 16*A* + (sign value) × (APC word) where sign value = 1 for *x*4 = 1 and sign value = −1 for *x*4 = 0. The product value for *X* = (10000) corresponds to APC value "zero," which could be derived by resetting the LUT output, instead of storing that in the LUT.

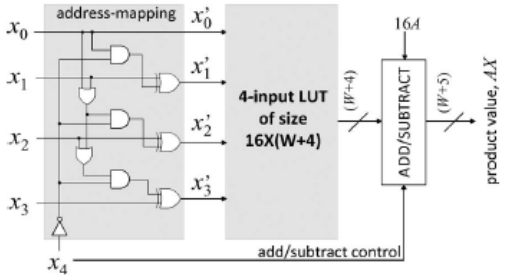

Fig.5 LUT-based multiplier for *L* = 5 using the APC technique

III. MODIFIED OMS FOR LUT OPTIMIZATION

for the multiplication of any binary word *X* of size *L*, with a fixed coefficient *A*, instead of storing all the 2*L* possible values of $C = A \cdot X$, only (2*L*/2) words corresponding to the odd multiples of *A* may be stored in the LUT, while all the even multiples of *A* could be derived by left-shift operations of one of those odd multiples.

A. APC words for different input value

Based on the above assumptions, the LUT for the multiplication of an *L*-bit input with a *W*-bit coefficient could be designed by the following strategy.

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Input, X	product values	Input, X	product values	address $x_3'x_2'x_1'x_0'$	APC words
0 0 0 0 1	A	1 1 1 1 1	$31A$	1 1 1 1	$15A$
0 0 0 1 0	$2A$	1 1 1 1 0	$30A$	1 1 1 0	$14A$
0 0 0 1 1	$3A$	1 1 1 0 1	$29A$	1 1 0 1	$13A$
0 0 1 0 0	$4A$	1 1 1 0 0	$28A$	1 1 0 0	$12A$
0 0 1 0 1	$5A$	1 1 0 1 1	$27A$	1 0 1 1	$11A$
0 0 1 1 0	$6A$	1 1 0 1 0	$26A$	1 0 1 0	$10A$
0 0 1 1 1	$7A$	1 1 0 0 1	$25A$	1 0 0 1	$9A$
0 1 0 0 0	$8A$	1 1 0 0 0	$24A$	1 0 0 0	$8A$
0 1 0 0 1	$9A$	1 0 1 1 1	$23A$	0 1 1 1	$7A$
0 1 0 1 0	$10A$	1 0 1 1 0	$22A$	0 1 1 0	$6A$
0 1 0 1 1	$11A$	1 0 1 0 1	$21A$	0 1 0 1	$5A$
0 1 1 0 0	$12A$	1 0 1 0 0	$20A$	0 1 0 0	$4A$
0 1 1 0 1	$13A$	1 0 0 1 1	$19A$	0 0 1 1	$3A$
0 1 1 1 0	$14A$	1 0 0 1 0	$18A$	0 0 1 0	$2A$
0 1 1 1 1	$15A$	1 0 0 0 1	$17A$	0 0 0 1	A
1 0 0 0 0	$16A$	1 0 0 0 0	$16A$	0 0 0 0	0

Table.1 APC words for different input values

1)A memory unit of $[(2L/2) + 1]$ words of $(W + L)$-bit width is used to store the product values, where the first $(2L/2)$ words are odd multiples of A, and the last word is zero.
2) A barrel shifter for producing a maximum of $(L - 1)$ left shifts is used to derive all the even multiples of A.
3) The L-bit input word is mapped to the $(L - 1)$-bit address of the LUT by an address encoder, and control bits for the barrel shifter are derived by a control circuit.

D. OMS-based design of the LUT of APC words

input X' $x_3'x_2'x_1'x_0'$	product value	# of shifts	shifted input, X''	stored APC word	address $d_3d_2d_1d_0$
0 0 0 1	A	0	0 0 0 1	$P0 = A$	0 0 0 0
0 0 1 0	$2 \times A$	1			
0 1 0 0	$4 \times A$	2			
1 0 0 0	$8 \times A$	3			
0 0 1 1	$3A$	0	0 0 1 1	$P1 = 3A$	0 0 0 1
0 1 1 0	$2 \times 3A$	1			
1 1 0 0	$4 \times 3A$	2			
0 1 0 1	$5A$	0	0 1 0 1	$P2 = 5A$	0 0 1 0
1 0 1 0	$2 \times 5A$	1			
0 1 1 1	$7A$	0	0 1 1 1	$P3 = 7A$	0 0 1 1
1 1 1 0	$2 \times 7A$	1			
1 0 0 1	$9A$	0	1 0 0 1	$P4 = 9A$	0 1 0 0
1 0 1 1	$11A$	0	1 0 1 1	$P5 = 11A$	0 1 0 1
1 1 0 1	$13A$	0	1 1 0 1	$P6 = 13A$	0 1 1 0
1 1 1 1	$15A$	0	1 1 1 1	$P7 = 15A$	0 1 1 1

Table .2 OMS-based design of the LUT of APC words

The word to be stored for X = (00000) is not 0 but $16A$, which we can obtain from A by four left shifts using a barrel shifter. However, if $16A$ is not derived from A, only a maximum of three left shifts is required to obtain all other even multiples of A. A maximum of three bit shifts can be implemented by a two-stage logarithmic barrel shifter, but the implementation of four shifts requires a three-stage barrel shifter. For X = (10000), the APC word "0" is derived by resetting the LUT output, by an active-high RESET signal given by

$$\text{RESET} = (x0 + x1 + x2 + x3) \cdot x4.$$

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IV. PROPOSED LUT OPTIMIZATION SCHEME

A. LUT Multiplier Using APC

The structure and function of the LUT-based multiplier for $L = 5$ using the APC technique. It consists of a four-input LUT of 16 words to store the APC values of product words as given in the sixth column of Table.1, except on the last row, where 2*A* is stored for input $X = (00000)$ instead of storing a "0" for input $X = (10000)$. Besides, it consists of an address-mapping circuit and an add/subtract circuit.

B. LUT USING MODIFIED OMS

The proposed APC–OMS combined design of the LUT for $L = 5$ and for any coefficient width W. It consists of an LUT of nine words of $(W + 4)$-bit width, a four-to-nine-line address decoder, a barrel shifter, an address generation circuit, and a control circuit for generating the RESET signal and control word ($s1s0$) for the barrel shifter.while 2*A* is stored for input $X = (00000)$ at LUT address "1000," as specified in Table 3.2. The decoder takes the 4-bit address from the address generator and generates nine word-select signals, i.e., $\{wi$, for $0 \le i \le 8\}$, to select the referenced word from the LUT.

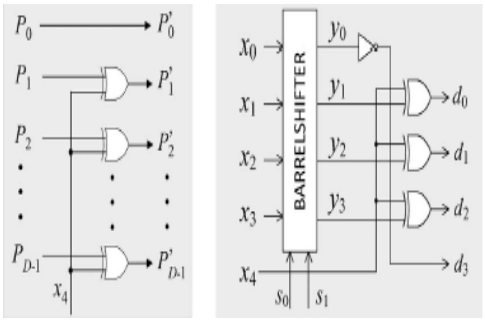

Fig .6 (a) sign modification LUT output. (b) Address-generation circuit.

The control bits $s0$ and $s1$ to be used by the barrel shifter to produce the desired number of shifts of the LUT output are generated by the control circuit, according to the relations

$$s_0 = \overline{x_0 + \overline{(x_1 + \overline{x_2})}}$$
$$s_1 = \overline{(x_0 + x_1)}.$$

Note that ($s1s0$) is a 2-bit binary equivalent of the required number of shifts specified in Tables 3.1 and 3.2.

C. BLOCK DIAGRAM OF ADAPTIVE FIR FILTER

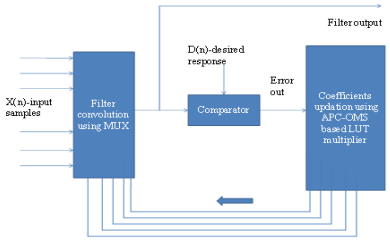

Fig.7 Block Diagram for Adaptive Filter

Adaptive filters differ from other filters such as FIR and IIR in the sense that

- The coefficients are not determined by a set of desired specifications
- The coefficients are not fixed.
- With adaptive filters the specifications are not known and change with time.

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- Applications include: process control, medical instrumentation, speech processing, echo and noise calculation and channel equalization.

V. RESULTS AND DISCUSSION

MODULES:

A. Performance of RLS
B. Power analyser
C. Synthesis report

A. PERFORMANCE OF RLS

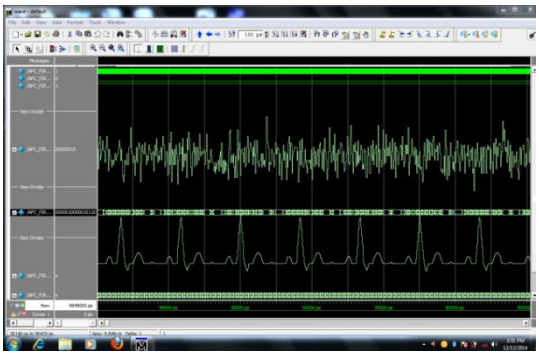

Fig. 8 Simulated output

In the fig.8, shows the Convergence performance of system identification with RLS.

B.POWER ANALYZER

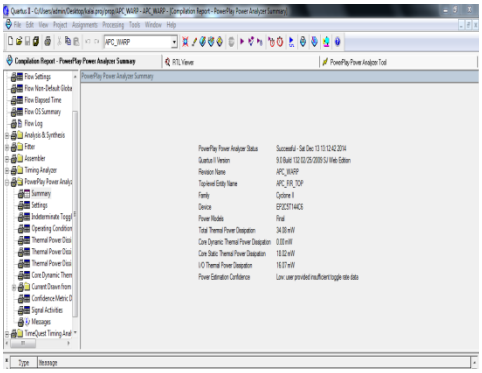

Fig. 9 Flow summary report

In the fig.9, show the power analyser with the help of QUARATUS-II software.

POWER ANALYZER

OVERCOME	VALUES
Existing System	60.52Mw
Proposed System	34.08mW

Table.1 power analyzer

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In this tabulation.1, show the different between existing system and proposed system.

D. SYNTHESIS REPORT

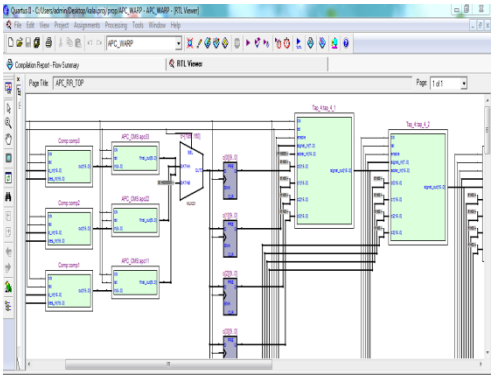

Fig.10 RTL Schematic report for efficient FIR filter

In this fig.10 show the area minimization with the help of APC-OMS techniques.

VI. CONCLUSION

In this paper simulation is carried out by using the APC-OMS based multiplier to reduce total logical area consumption. The Anti-Symmetric Product Coding (APC) and Odd-Multiple-Storage (OMS) techniques were used for Look-Up-Table (LUT) FIR filter. Hence, the combination of these two techniques provides reduction in LUT size to one-fourth in adaptive FIR filter, it improving the convergence performance of system identification by using Recursive Least Square approach, synthesis the performance of power and timing analyzer.

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BIOGRAPHY

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