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Estimating the Power Delay Product in Adder Circuit

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ABSTRACT: The main aim of this project is to design a 1- bit full adder using an alternative logic structure and estimating the power delay product. Power delay Product is used find the energy efficiency of the full adder circuit. Power delay product is compared with both alternative logic structure and the existing structure.The layout is designed and simulation results will be obtained using an EDA tool MICROWIND 2.

KEYWORDS: Alternative logic structure, Adder, Pass Transistor Logic.

I. INTRODUCTION

Energy-efficiency is one of the most required features for modern electronic systems designed for high-performance and portable applications. The power-delay product (PDP) Metric relates the amount of energy spent during the realization of a determined task, and stands as the more fair performance metric when comparing optimizations of a module designed and tested using different technologies and scenarios.

Addition is a fundamental arithmetic operation that is broadly used in many VLSI systems, such as application-specific digital signal processing (DSP) architecture and microprocessors. Full adder is the core of many arithmetic operations such as addition/subtraction, multiplication, division and address generation. In majority of these systems, the adder is part of the critical path that determines the overall performance of the system. That is why enhancing the performance of the full adder cell results of great interest [1]. There are three major components of power dissipation in complementary metal oxide semiconductor (CMOS) circuits: switching power, short circuit power and static power. Reducing whichever of these components will end up with lower power consumption for the whole system.

In this paper, we report the design and performance comparison of two full-adder cells implemented with an alternative internal logic structure, based on the multiplexing of the Boolean functions XOR/XNOR and AND/OR, to obtain balanced delays in SUM and CARRY outputs, respectively, and pass-transistor logic styles, in order to reduce power consumption. The resultant full-adders show to be more efficient on regards of power consumption and delay when compared with other ones reported previously as good candidates to build low-power arithmetic modules.

This paper is organized as follows. Section II presents the internal logic structure adopted as standard in previous papers for designing a full-adder cell. Section III introduces the alternative internal logic structure and the pass-transistor logic styles used to build the two proposed full-adders. Section IV reviews the results obtained from the simulations, and Section V concludes this work.

II. PREVIOUS WORK

Several papers have been published regarding the design of low power full adders, trying on both: the logic style and the logic structure used to build the adder module. Since the standard CMOS realization [2], several full adders built

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upon different static logic styles have been presented, namely: Differential Cascode Voltage Switch (DCVS) [3], Complementary Pass-Transistor Logic (CPL) [4], Double Pass-Transistor Logic (DPL)[5], and Swing Restored CPL (SR-CPL) [6]. On the base of these logic styles, some work has been done to build new full adders by changing the internal logic structure of the module. In earlier work [7], transmission function theory was used to build a full adder formed by three main logic blocks: a XOR-XNOR gate to obtain A EXOR B and A EXNOR B signals (Block 1), and EXOR blocks or multiplexers to obtain the SUM (So) and CARRY (Co) outputs (Blocks 2 and 3), as shown in Figure 1.

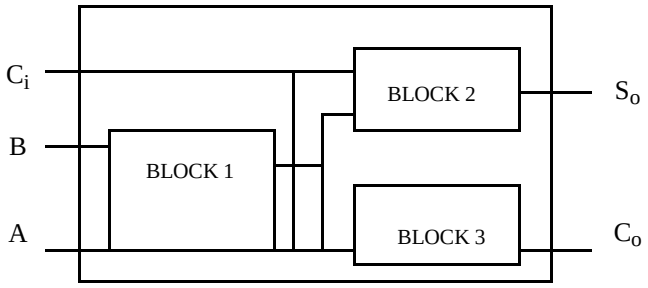

Fig. 1.Full-adder cell formed by three main logical blocks.

TABLE I

TRUE-TABLE FOR A 1-BIT FULL-ADDER: A, B, AND C ARE INPUTS; S_0 AND C_o ARE OUTPUTS

C	B	A	S_o	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

A deep comparative study to determine the best implementation for Block1 was presented in [8], and an important conclusion was pointed out in that work: the major problem regarding the propagation delay for a full-adder built with the logic structure shown in Fig. 1, is that it is necessary to obtain an intermediate A XOR B signal and its complement, which are then used to drive other blocks to generate the final outputs. Thus, the overall propagation delay and, in most of the cases, the power consumption of the full-adder depend on the delay and voltage swing of the A XOR B signal and its complement generated within the cell. So, to increase the operational speed of the full-adder, it is necessary to develop a new logic structure that does not require the generation of intermediate signals to control the selection or transmission of other signals located on the critical path.

III. ALTERNATIVE LOGIC STRUCTURE FOR A FULL ADDER

Examining the full adder's true table in Table I, it can be seen that the S_o output is equal to the A XOR B value when C=0, and it is equal to A XNOR B when C=1. Thus, a multiplexer can be used to obtain the respective value taking the C input as the selection signal. Following the same criteria, the C_o output is equal to the A.B value when

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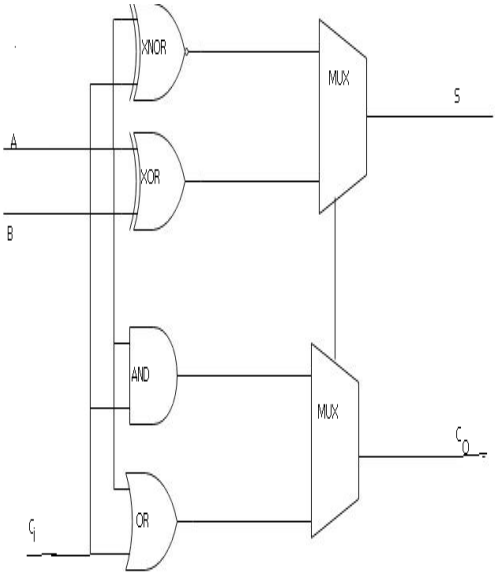
C=0, and it is equal to A+B value when C=1. Again, C can be used to select the respective value for the required condition, driving a multiplexer.
Hence, an alternative logic scheme to design a full adder cell can be formed by a logic block to obtain the signals A XOR B and A XNOR B, another block to obtain the A.B and A+B signals, and two multiplexers being driven by the C input to generate the S_O and C_O output s, as shown is Fig. 2

A. Double Pass Transistor Logic(DPL)

The DPL is a modified version of CPL, in which both nMOS and pMOS logic networks are used together to alleviate the problem of the CPL associated with reduced high logic level. As this provides full swing on the output, no extra transistors for swing restoration is necessary. Two-input AND/NAND DPL realization is achieved by connecting a Pull



. Fig. 2. Alternative logic scheme for designing full-adder cells.

The features and advantages of this logic structure are as follows.

• **There are no signals generated internally that control the** selection of the output multiplexers. Instead, the C input signal, exhibiting a full voltage swing and no extra delay, is used to drive the multiplexers, reducing so the overall propagation delays.

• **The capacitive load for the C input has been reduced, as it is** connected only to some transistor gates and no longer to some drain or source terminals, where the diffusion capacitance is becoming very large for sub-micrometer technologies. Thus, the overall delay for larger modules where the C signal falls
on the critical path can be reduced.
• **The propagation delay for the** So and Co outputs can be tuned up individually by adjusting the XOR/XNOR and the AND/OR gates; this feature is advantageous for applications where the skew between arriving signals is critical for a proper operation, and for having well balanced propagation delays at the outputs to reduce the chance of glitches in cascaded applications.

• **The inclusion of buffers at the full**-adder outputs can be implemented by interchanging the XOR/XNOR signals, and the AND/OR gates to NAND/NOR gates at the input of the multiplexers, improving in this way the performance

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for load-sensitive applications. Based on the results obtained, new full-adder has been designed using the DPL logic style, and the new logic structure presented in Fig. 2. Fig. 3 presents the internal logic used for the full-adder design. The AND/OR gates and XOR/XNOR gates are using a DPL logic style. A pass-transistor based multiplexer to obtain the So and C_O output and a pass-transistor based multiplexer to get the Co output. The circuit diagram of the full adder designed using a double pass transistor logic is shown in Fig. 4. The full adder is designed using 0.18µm technology.

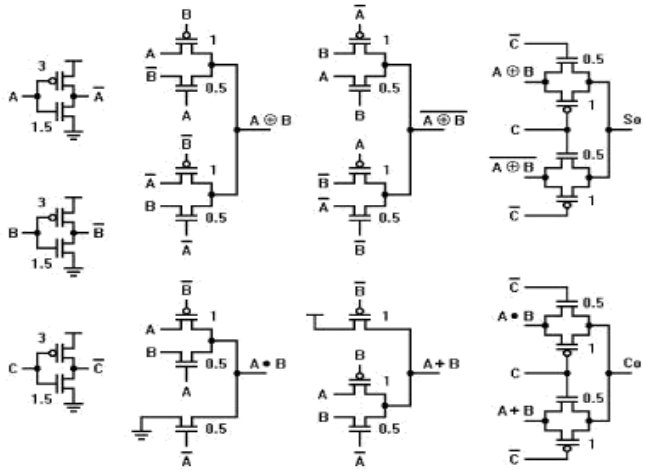

Fig.3. Internal Logic for the full adder using alternative logic structure

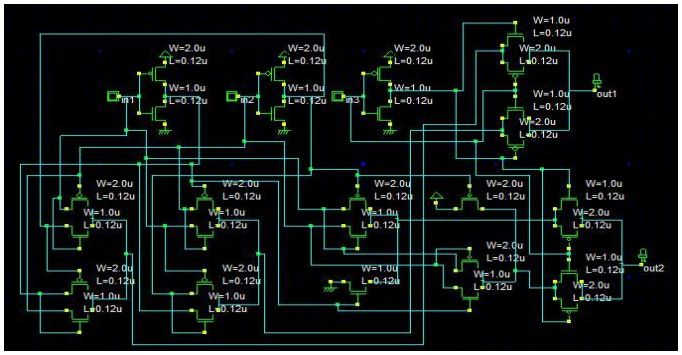

Fig.4. Circuit diagram of full adder using DPL logic

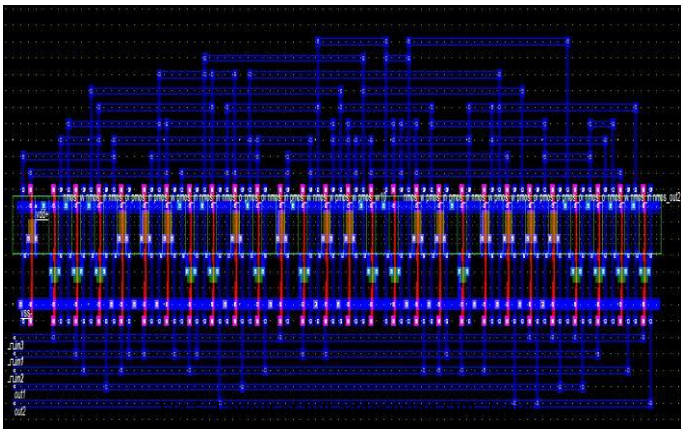

Fig.5. shows the layout of the full adder using alternative logic structure. The layout is designed using Microwind an EDA tool with 0.18µm technology.

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IV. SIMULATION AND RESULTS

The post layout simulation obtained is shown in Fig.6. First three waveform represents inputs C, B, A respectively. The fourth and fifth waveform represents S_o and C_o output respectively.

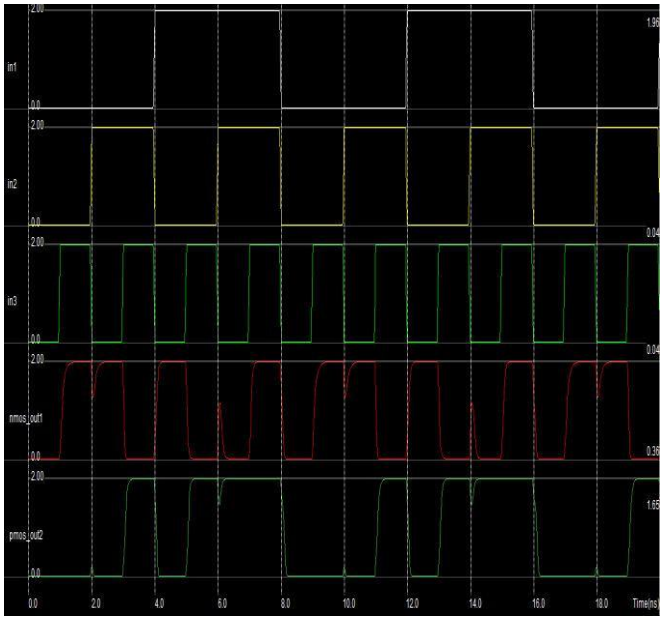

Fig.4. Simulation result of full adder using DPL logic

A. Result Analysis

TABLE II
RESULT ANALYSIS

Full Adder Type (DPL)	Dissipated Power(mw)	Propagation Delay(ns)	PDP (pj)
Existing	0.167	5.032	1.030
Proposed	0.135	2.630	0.512

Table II shows the post layout simulation results obtained using Microwind. From the results obtained, it is been found that the proposed full adder report low dissipation power and low propagation delay.
From the table II it is been evident that there is 60% reduction in PDP of proposed full adder when compared with the PDP of the existing one.

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V. CONCLUSION

To calculate the Power delay for a adder using an alternative logic structure and pass transistor logic. The simulation result was obtained and the Power Delay Product (PDP) was calculated using an EDA tool Microwind. From the result obtained it is been found that there is 60% reduced PDP when compared with the existing one and it is evident that the proposed system is energy efficient .

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