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Baseband Digital Coherent Transponder for Satellites

Devikka.S[1], Dr.T.V.U.Kiran Kumar*[2]

Assistant Professor, Dept. of ECE, Jerusalem College of Engineering, Chennai, Tamil Nadu, India[1]

Assistant Professor, Dept. of ECE, Bharath University, Chennai, Tamil Nadu, India[2]

* Corresponding Author

ABSTRACT: Digital Modulators are designed and implemented using XILINX ISE Tool based on Very Large Scale Integration (VLSI). This is majorly to implement and obtain digitalize signals in software defined radio (SDR) for signal power. SDR is a very widespread solution, whose modulation / demodulation methodology consists in programming the software in a dedicated programmable logic device (FPGA). This results in a high degree of versatility in the equipment because the same physical hardware can be used to implement different digital modulators / demodulators. In this context, Field-programmable gate-arrays (FPGA's) are the best solution, due to their best performance. Using XILINX software tools, the digital modulators schematic and simulations are designed and are presented, which helps to obtain accurate design constraints. Here by using Spartan 3E the implementation is done and the results are observed.

KEYWORDS: Digital Modulation, FPGA, VLSI, Xilinx

1. INTRODUCTION

In general communication modulation is "the process of varying one or more properties of a periodic waveform i.e., the carrier-signal, for transmitting a modulating signal that contains information".
Modulation of a sine waveform is used to transform a baseband message signal into a pass band signal. A device that performs modulation is known as a modulator. A device that performs the inverse operation of modulation is known as a demodulator. A device that performs operations as modulator and demodulator is known as modem.
The aim of digital modulation methods is to transfer a narrow band digital signal, in this scheme, as a bit stream over another digital transmission system.

Despite simple transmitter and receiver architecture of Digital modulators and its modulation technique is still commonly used in Wireless communication. Binary Phase shift keying (BPSK) is data transfer technique with different amplitude of carrier frequency. As it is sensitive to propagate the channel variation, thus it is has been widely used in low power wireless transceiver for system simplicity.

S band TT&C transponder is based on a software-defined–radio (SDR) architecture. This is used to develop a low-cost and lightweight S-Band TT&C transponder, for Low Earth Orbit (LEO) missions and targets earth observation missions with short mission durations of 3-5 years. The TT&C transponder as a functional assembly consists of two physically separate modules (the electronics module), commonly referred to as the TT&C transponder and the duplexer.

These digital modulation techniques were implemented on FPGA device. Simulation results consist of bit error rate of digital signals of modulators, source consumption of BPSK and FPGA-based, bit rate of BPSK on Xilinx ISE suite complier using Verilog language. Thus digital modulators were implemented on FPGA.

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In addition to, bit error rate of BASK and BPSK modulation techniques was compared using Xilinx. In this paper, for BPSK and BASK modulation, FPGA based modulator is presented. Finally, simulation results are obtained.
The Digital Signal Processing and the Channel Coding Stages where implemented within a FPGA (Spartan 3 line, from Xilinx) to take advantage of the massive parallel computation power of these devices and to have the possibility to scale up to ASIC devices.

The aim of this paper is implementation of fully digital modulators that employ the minimum number of digital blocks suitable for educational purpose, software-defined radio systems and are integrable with the FPGA board using Spratan3E. Furthermore, the implemented FPGA designs can be used in a digital communication course to demonstrate digital-modulation techniques.

II. OVERVIEW OF DIGITAL MODULATORS

The major technique for digital modulation based on keying is BPSK (binary phase-shift keying): a finite number of phases are used [1].
A unique pattern of binary bits have being assigned by digital modulators and each phase, frequency or amplitude encodes an equal number of bits and the specific phase, frequency or amplitude comprises the symbol [2].
Thus M=2N, Here each symbol represents a message consisting of *N* bits. If the symbol rate (also known as the baud rate) is fs symbols/second (or baud), the data rate is Nfs bit/second.

III. CONCEPT OF BINARY PHASE SHIFT KEYING

Digital modulation is the process by which digital symbols are transmitted into waveforms that are compatible with the characteristics of the channel .The modulation process converts a baseband signal into a band pass signal compatible with available transmission facilities receiver because it correlates the received signal composed of the transmitted signal plus noise with a sinusoidal signal that is phase-locked to the transmitted carrier [3-4].
The purpose of the correlation receiver is to reduce the received symbol to a single point or statistic that is used by the decision circuit to determine which symbol was transmitted (either 0 or The same as the carrier, with 0º initial phase, but if "0" was transmitted, the modulated signal would change with 180º.

The aim of the paper is to generate BPSK modulation which is a popular modulation technique used in communication industry, thus its symbol error performance and bandwidth efficiency [5]. The BPSK (Binary Phase Shift Keying) is one of the three basic binary modulation techniques. It has as a result only two phases of the carrier, at the same frequency, but separated by 180º.
If "1" was transmitted, the modulated signal remained the same as the carrier, with 0º initial phase, but if "0" was transmitted, the modulated signal would change with 180º, 1. The aim of the paper is to generate BPSK modulation which is a popular modulation technique used in communication industry, thus its symbol error performance and bandwidth efficiency [6].

IV. BPSK TRANSMITTER

The binary wave and sinusoidal carrier wave k1(t) are applied to a product modulator. The carrier and timing pulses used to generate the binary wave are usually extracted from a common master clock. The desired phase shift keying wave is obtained at the modulated output [7]. Thus a binary phase shift keying wave may also be viewed as a special form of double suppressed carrier (DSBSC) modulated wave.

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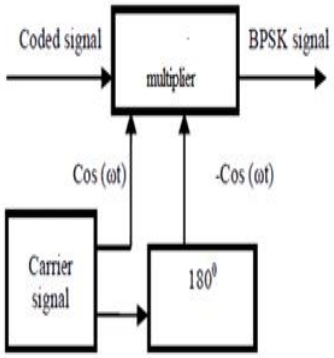

Fig. 1. BPSK TRANSMITTER

E. BPSK RECEIVER:

To reconstruct the original binary sequence of 1's and 0's, we apply the noisy phase shift keying wave x(t) to a correlator, which is also supplied with a locally generated coherent signal k1(t).The correlator output, x1 is compared with a threshold of 0 volts [8].

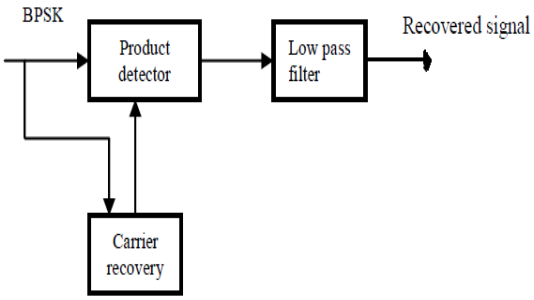

Fig. 2.BPSK RECEIVER

F. CONDITION:

If x1>0 the receiver decides in favour of symbol 1.

If x1<0, it decides in favour of symbol 0.All digital communication systems, the combination of the modulator and demodulator simultaneously are performed.

Digital modulation schemes are possible because the transmitter-receiver pair have prior knowledge of how data is encoded and represented in the communications system. In all digital communication systems, the modulator and demodulator that consists of the transmitter and the receiver are structured so that they perform inverse operations.

Non-coherent modulation methods do not require a receiver reference clock signal that is phase synchronized with the sender carrier wave. In this case, modulation symbols are asynchronously transferred and an opposite is known as coherent modulation.

G. HARDWARE IMPLEMENTATION:

The hardware implementation of BPSK system is done using HDL coder and the components of System Generator. The following tools are necessary for the simulation and implementation

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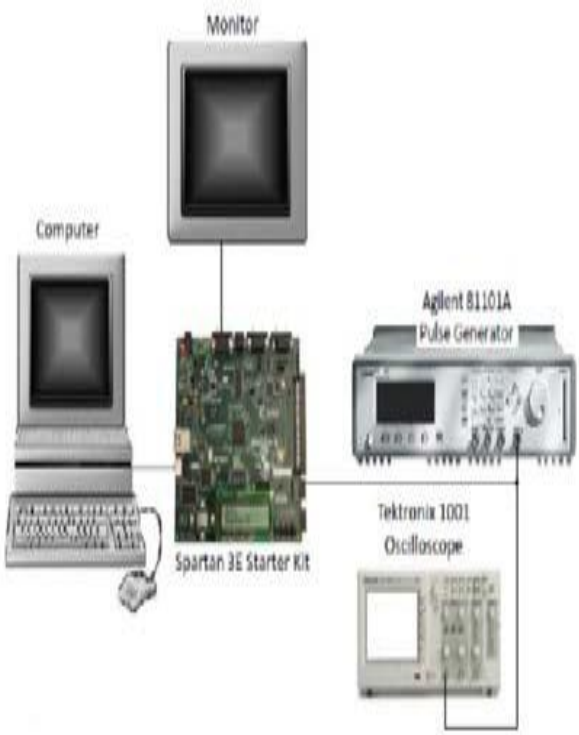

Fig. 3. FPGA KIT IMPLEMENTATION

H. SPECIFICATIONS:

The specification of the transmitter is listed below:

Transmitter		
Tx Frequency Range	2200 ... 2300	MHz
Dynamic Range	+27 ... +33	dBm
Carrier Frequency Stability	initial ±1	ppm
	aging ±5	ppm
Modulation Formats	1) PCM (NRZ-L)/BPSK	
	2) PCM (NRZ-L)/(O)QPSK	
Data Rates	1) 64 ... 1024	kbps
	2) 1 ... 6.25	Mbps
Error Vector Magnitude	<10	%
Tx Power Consumption	14	W
Supply Voltage	22 ... 34	V
Mass	0.78	kg
Volume	145 x 110 x 50	mm^3
Operating Temperature Range	-20 ... +60	°C
Radiation Tolerance	10	kRad

Table. 1. BPSK TRANSMITTER

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The specification of the receiver is given by:

Receiver		
Rx Frequency Range	2025 ... 2120	MHz
Dynamic Range	-135 ... -40	dBm
Noise Figure	2	dB
Modulation Formats	1) PCM/PSK/PM 8kHz SC	
	2) PCM/PSK/PM16kHz SC	
	3) PCM/BPSK	
Data Rates	1) 0.5 / 1 / 2	kbps
	2) 1 / 2 / 4	kbps
	3) 64 ... 1024	kbps
Carrier Acquisition Threshold	-120	dBm
Carrier Tracking Threshold (35kHz/s)	-125	dBm
Carrier Tracking Range	±150	kHz
Carrier Acquisition Sweep Rate	35	kHz/s
BER Threshold ($1x10^{-6}$)[4kbps/16kHz SC]	-117	dBm
Rx Power Consumption	4	W

Tab. 2. BPSK RECEIVER

IV. SIMULATED RESULT

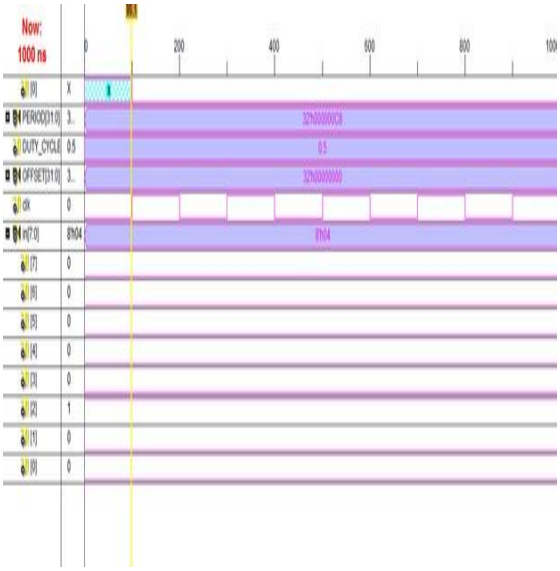

Fig. 4. Output of BPSK

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VI. CONCLUSION

The BPSK Modulator in the Verilog environment with blocks are implemented. The results given by the development board exactly matches with the results obtained from simulation setup. Since the results obtained in hardware are dependent of the design in software, it is much simpler to carry out changes in these results by means of the software, even after having finished the design and its implementation.

After implementing the BPSK modulator, we want to realize a BPSK system. The system will consist of a modulator and demodulator and the signal from the modulator to demodulator will pass through a channel affected by noise. The modulated and demodulated signals will be also routed to monitors, performance can be calculated.

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