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Comparison of Power and Area in High Performance Fir Filter Architecture for Fixed and Reconfigurable Application

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ABSTRACT*:* Transpose form finite impulse response (FIR) filters are inherently pipelined which supports the multiple constant multiplications (MCM) that provides the solution in important storage of the computation. But that transpose form of configuration is not directly supporting the block processing which is not like as direct form configuration. The possibility of realization of block FIR filter is in transpose form configuration is explored for the area-delay efficient realization of huge order FIR filter for the applications which is both fixed and also reconfigurable with minimized register complexity ,a flow graph for transpose form block FIR filter is derived that is based on the detailed computational analysis of transpose form configuration of FIR filter, a generalized block formulation is provided. The architecture obtains the less ADP (area delay path) and less EPS (energy per sample) when compare to the previous block execution of direct form structure for large or medium filter length. The proposed architecture of this project analysis, area , delay and power consumption using Xilinx 7.1i.

KEYWORDS: component; block processing, finiteimpluse response(FIR),reconfigurable architecture (key words)

I. INTRODUCTION

A process of creating an integrated circuit (IC) by combining thousands of transistors into a single chip is known as very large scale integration.

A finite impulse response (FIR) filter is a filter structure that can be used to represent any sort of frequency response in digital form. An FIR filter is usually implemented by using a series of delays, multipliers, and adders to create the filter's output.

After manufacture the designer or customer designed a semiconductor device which can be reconfigurable to all the environment is termed as field programmable gate array.

The number adders along the critical path of the multiplier block of a transposed form fir filter. The transpose form requires larger word length for the intermediate register which can increase the power consumption.

The FIR filter with transposed structure has register between adders and can achieve high throughput without added any extra pipeline register. The transpose form is self pipelined with cycle period the delay of a adder and multiplier.

On the other hand, the number of additions is reduced in the MCM method which is required for the realization of multiplications , we will get common sub expression which is multiplied with a set of constants. The MCM scheme is more effective ,when a common operand is multiplied with more number of constants.

But, MCM blocks can be formed only in the transpose form configuration of FIR filters .The number adders along the critical path of the multiplier block of a transpose form FIR filter that requires large word length for the intermediate register which can increases the power consumption.

For the advantage of the MCM schemes and the fundamental pipelining for area-delay efficient realization of larger order FIR filters for both fixed and reconfigurable application ,we explore the possibility of realization of block fir filter in transpose form configuration .

Reconfigurable FIR filter whose filter coefficients change dynamically during run time plays an important role in the software defined radio (SDR) systems, multi-channel filters, and digital up/down converters.

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A set of input is shifted through by n number of registers (SR) also called "taps". The transposed form of the FIR filter produces the same output as the direct form. The difference is that it forms all the multiplications of a variables at the same time.

The main advantage of using FIR filter is that an exact linear phase response can be obtained . The shift register are moved to the delay output from a multiplication instead of the input.

II. MATHEMATICAL FORMULATION OF TRANSPOSE FORM FIR FILTER

The output of an FIR filter of length N can be computed using the relation

$$y(n) = \sum_{i=0}^{N-1} h(i).x(n-i) \qquad \ldots\ldots (1)$$

The computation of (1) can be expressed by the recurrence relation

$$Y(z)=[z^{-1}(\cdots(z^{-1}(z^{-1}h(N-1)+h(N-2))+h(N-3))\cdots+h(1))+h(0)]X(z) \qquad \ldots\ldots (2)$$

COMPUTATIONAL ANALYSIS

The data-flow graphs (DFG-1 and DFG-2) of transpose form FIR filter for filter length N=6, as shown in Fig..1,for a block of two successive outputs{y(n),y(n−1)} that are derived from (2). The product values and their accumulation paths in DFG-1 and DFG-2 of Fig..1 are shown in dataflow tables (DFT-1 and DFT-2) of Fig. .1. The arrows in DFT-1 and DFT-2 of Fig. .1 represent the accumulation path of the products.

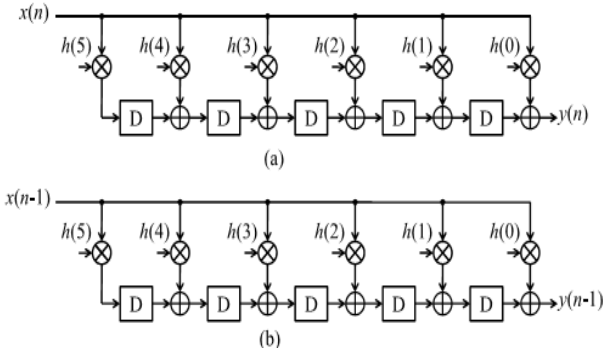

Fig.1. DFG of transpose form structure for N =6. (a) DFG-1 for output y(n). (b) DFG-2 for output y (n−1).

The arrows inDFT-1 and DFT-2 of Fig.2 represent the accumulation path of the products. We find that five values of each column of DFT-1are same as those of DFT-2.

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ccs	M_1	M_2	M_3	M_4	M_5	M_6
1	$x(n\text{-}5)h(5)$	$x(n\text{-}5)h(4)$	$x(n\text{-}5)h(3)$	$x(n\text{-}5)h(2)$	$x(n\text{-}5)h(1)$	$x(n\text{-}5)h(0)$
2	$x(n\text{-}4)h(5)$	$x(n\text{-}4)h(4)$	$x(n\text{-}4)h(3)$	$x(n\text{-}4)h(2)$	$x(n\text{-}4)h(1)$	$x(n\text{-}4)h(0)$
3	$x(n\text{-}3)h(5)$	$x(n\text{-}3)h(4)$	$x(n\text{-}3)h(3)$	$x(n\text{-}3)h(2)$	$x(n\text{-}3)h(1)$	$x(n\text{-}3)h(0)$
4	$x(n\text{-}2)h(5)$	$x(n\text{-}2)h(4)$	$x(n\text{-}2)h(3)$	$x(n\text{-}2)h(2)$	$x(n\text{-}2)h(1)$	$x(n\text{-}2)h(0)$
5	$x(n\text{-}1)h(5)$	$x(n\text{-}1)h(4)$	$x(n\text{-}1)h(3)$	$x(n\text{-}1)h(2)$	$x(n\text{-}1)h(1)$	$x(n\text{-}1)h(0)$
6	$x(n)h(5)$	$x(n)h(4)$	$x(n)h(3)$	$x(n)h(2)$	$x(n)h(1)$	$x(n)h(0)$

(a)

ccs	M_1	M_2	M_3	M_4	M_5	M_6
1	$x(n\text{-}6)h(5)$	$x(n\text{-}6)h(4)$	$x(n\text{-}6)h(3)$	$x(n\text{-}6)h(2)$	$x(n\text{-}6)h(1)$	$x(n\text{-}6)h(0)$
2	$x(n\text{-}5)h(5)$	$x(n\text{-}5)h(4)$	$x(n\text{-}5)h(3)$	$x(n\text{-}5)h(2)$	$x(n\text{-}5)h(1)$	$x(n\text{-}5)h(0)$
3	$x(n\text{-}4)h(5)$	$x(n\text{-}4)h(4)$	$x(n\text{-}4)h(3)$	$x(n\text{-}4)h(2)$	$x(n\text{-}4)h(1)$	$x(n\text{-}4)h(0)$
4	$x(n\text{-}3)h(5)$	$x(n\text{-}3)h(4)$	$x(n\text{-}3)h(3)$	$x(n\text{-}3)h(2)$	$x(n\text{-}3)h(1)$	$x(n\text{-}3)h(0)$
5	$x(n\text{-}2)h(5)$	$x(n\text{-}2)h(4)$	$x(n\text{-}2)h(3)$	$x(n\text{-}2)h(2)$	$x(n\text{-}2)h(1)$	$x(n\text{-}2)h(0)$
6	$x(n\text{-}1)h(5)$	$x(n\text{-}1)h(4)$	$x(n\text{-}1)h(3)$	$x(n\text{-}1)h(2)$	$x(n\text{-}1)h(1)$	$x(n\text{-}1)h(0)$

(b)

Fig.2. (a) DFT of multipliers of DFG shown in Fig.2.1(a) corresponding to output y(n). (b) DFT of multipliers of DFG shown in Fig.3.1(b) corresponding to output y (n−1).

The computation of DFT-3 can be realized by DFG-3 of non-overlapping blocks, as shown in Fig.3. We refer it to block transpose form type-I configuration of block FIR filter. The type –I configuration involves same number of adders and multipliers.

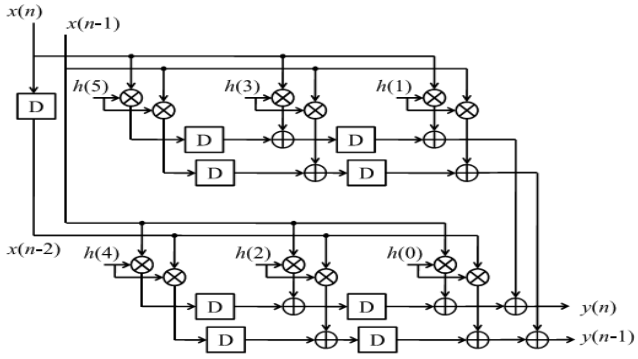

Fig.3. Merged DFG (DFG-3: transpose form type-I configuration for block FIR structure).

MCM BASED IMPLEMEMTATION OF FIR FILTER

The MCM method on the other hand reduces the number of additions required for the realization of multiplications by common sub expression sharing, when a given input is multiplied with a set of constants. MCM blocks can be formed only in the transpose form configuration of FIR filters.

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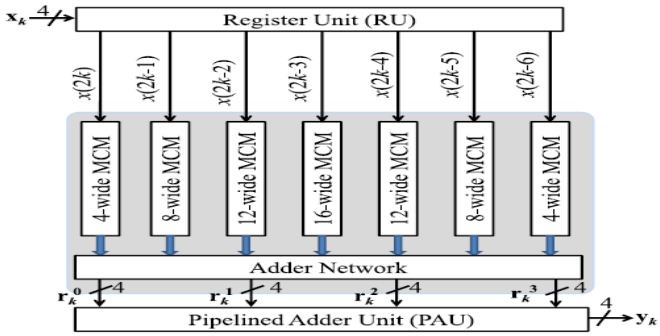

Fig.4 MCM based structure of fixed FIR filter

MCM can be applied in both horizontal and vertical direction of the coefficient matrix. The sample *x (4k−3)* appears in four rows or four columns of the following input matrix.

III. PROPSED STRUCTURE

By using this 32 tap FIR filter for Low pass, High pass, Band pass, and band stop filter and to analysis the performance, efficiency, speed, and power consumption for the respective filter types. Below figure shows the block diagram of the proposed system.

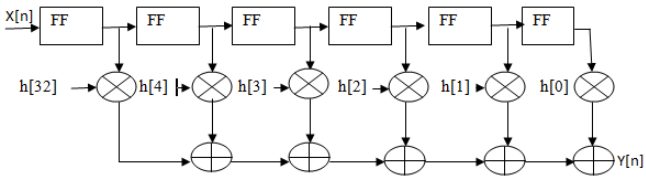

Fig.6. DFG of transpose form structure for N=32

Let's look at an example of 32-tap discrete finite impulse response (FIR) filtering, which can be expressed

$$Y[n]=\sum_{k=0}^{32} x[n-k]h[k].....(3)$$

FPGA can perform 32 parallel operation to provide the result in one clock cycle using the parallel filtering architecture. In contrast, computer processors require more than one clock cycle to provide the same result, as illustrated in the following pseudo-code:

```
for k=0 to 32
 y[n]=x[n-k]×h[k]
 end for
```

The NCO used for signal generation with required frequency range. NCO is used in the modulation block.

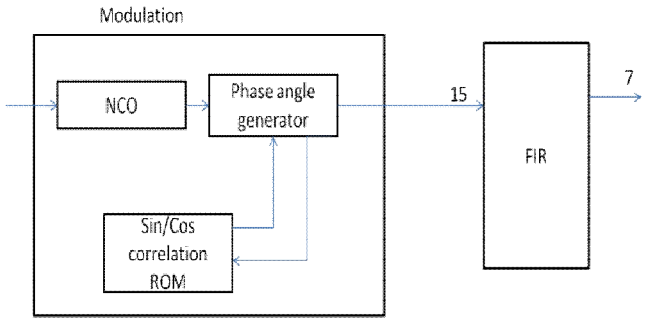

Fig.5.modulation block

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A low-pass filter is a filter that passes signals with a frequency lower than a certain cut off frequency and attenuates signals with frequencies higher than the cut off frequency. The amount of attenuation for each frequency depends on the filter design. The filter is sometimes called a high-cut filter, or treble cut filter in audio applications. A low-pass filter is the opposite of a high-pass filter. A band-pass filter is a combination of a low-pass and a high-pass filter.

Low-pass filters exist in many different forms, including electronic circuits (such as *filter* used in audio), anti - aliasing filters for conditioning signals prior to analog -to-digital conversion, digital filters for smoothing sets of data, acoustic barriers, blurring of images, and so on. The moving average operation used in fields such as finance is a particular kind of low-pass filter, and can be analysed with the same signal processing techniques as are used for other low-pass filters. Low-pass filters provide a smoother form of a signal, removing the short-term fluctuations, and leaving the longer-term trend.

. The primary functions of filters are one of the followings:

a) To confine a signal into a prescribed frequency band as in low-pass, high-pass, and band-pass filters.
b) To decompose a signal into two or more sub-bands as in filter-banks, graphic equalizers, sub-band coders, frequency multiplexers.
c) To modify the frequency spectrum of a signal as in telephone channel equalization and audio graphic equalizers.
d) To model the input-output relationship of a system such as telecommunication channels, human vocal tract, and music synthesizers.

Depending on the form of the filter equation and the structure of implementation, filters may be broadly classified into the following classes.

a. Linear filters versus nonlinear filters.
b. Time-invariant filters versus time-varying filters.
c. Adaptive filters versus non-adaptive filters.
d. Recursive versus non-recursive filters.

In this chapter we are mainly concerned with linear time-invariant (LTI) filters. These are a class of filters whose output is a linear combination of the input and whose coefficients do not vary with time.

The main advantage of this FIR filters are reduced filter length, less element to used, reduced cycle period.

IV. SYNTHESIS RESULT

We have coded the proposed structure in Model Sim 6.5b for filter length of tap 16, 32.so ,we are increase the based upon the power level in testing 32 –tap is suitable and we are get the good efficiency level. A graph are plotted are using be estimated values and shown in fig.(8,9).we have estimated ADP (area/sampling frequency) and EPS(power/sampling frequency)of the proposed structure of transpose form structure. The proposed structure has 4.6% less ADP and 7.2% less EPS.

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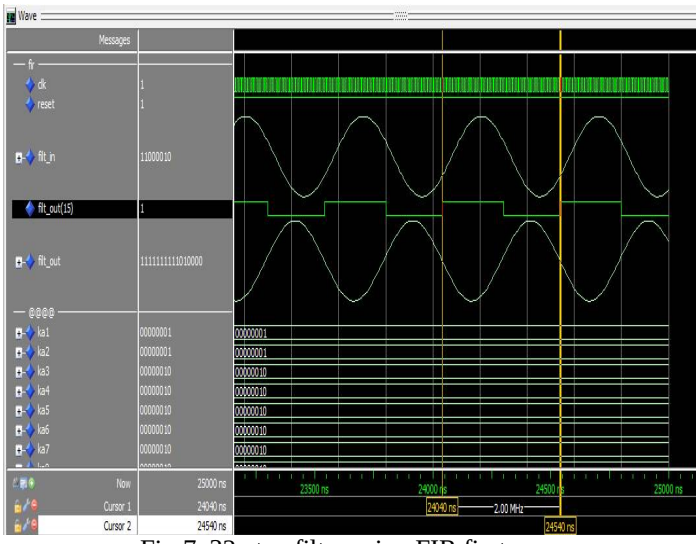

Fig:7 32 –tap filter using FIR fix types

TABLE I

Synthesis results of proposed structure and existing structure using 32-tap

Taps	**Area(um^2)**	**Power(w)**	**Delay**
8 tap	54836	0.114	7.343
16 tap	70521	0.120	10.176
32 tap	93296	0.145	15.999

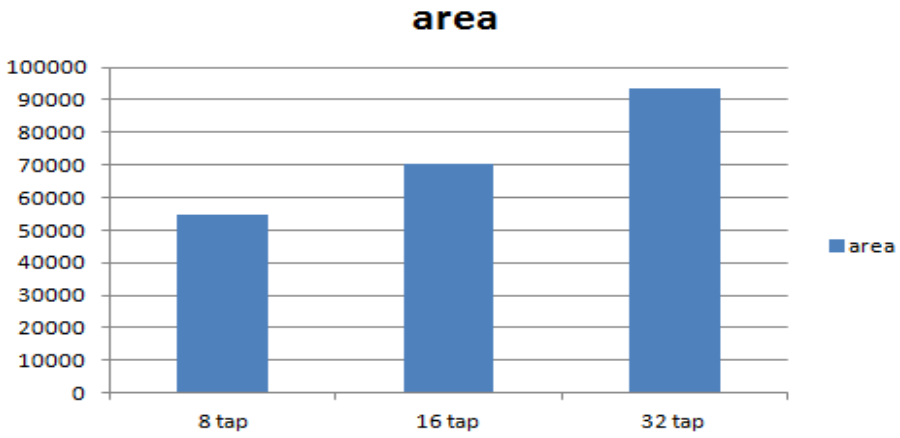

Fig:8 Comparison of area

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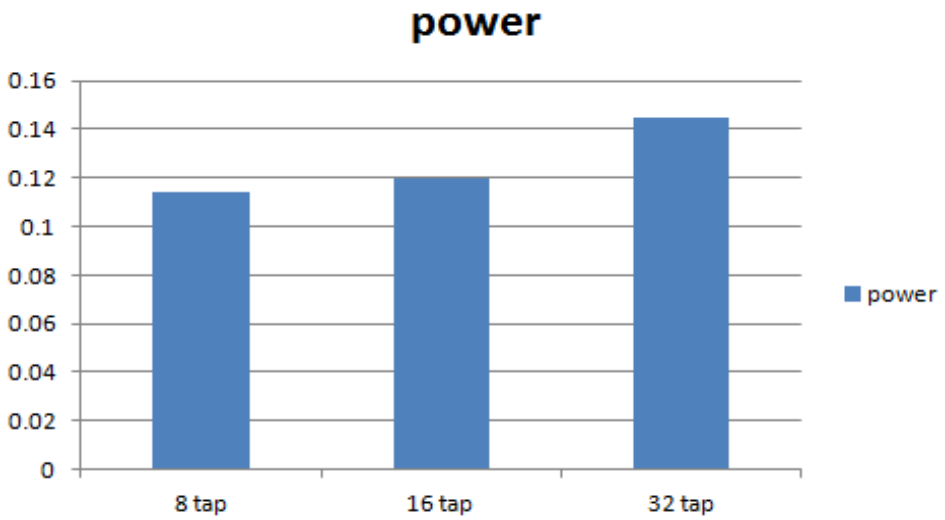

Fig:9 Comparison of power

V.CONCLUSION

In this paper we have found that the possibility of realization of block FIR filter in transpose form configuration of area, delay and power for the efficient realization of both fixed and reconfigurable applications. A transpose form block FIR filter in a generalized block form is presented and based on that we have derived transpose form block filter for reconfigurable applications. we have presented a scheme about 32-tap FIR filter for low pass, high pass, and band reject filter and to analysis the above mentioned specification. Performance comparison shows that the proposed structure involves significant 4.6% less ADP and 7.2% less EPS then the existing block direct form structure has 13% less ADP and12.8% less EPS.

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