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Design of Low Power Half Adder Using Adaptive Voltage Level (AVL) Technique

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ABSTRACT: In VLSI arithmetic circuits plays a important role. In this adder is one of the arithmetic circuits. In this paper, the half adder is being designed by using adaptive voltage level (AVL) techniques. These design are used to reduce the power consumption compared to other conventional design. We can reduce the value of the total power dissipation by using adaptive voltage level at ground (AVLG) technology in which the ground potential is raised to reduce power consumption and adaptive voltage level at supply (AVLS) in which the supply potential is increased to reduce the power consumption. This paper represents how to control the power by using AVL technique. The Half adder design using AVL technique are compared to the conventional half adder design based on the power consumption, propagation delay, speed, layout area and number of transistor is preferred. Power consumption of the proposed design is measured and compared. The result shows that there is a reduction in power and transistor count for this proposed method. The circuit is simulated on Micro Wind 3.1 and DSCH in CMOS technology.

KEYWORDS: Half adder, AVL technique, Low Power, High Speed Transistor Count, VLSI

I.INTRODUCTION

In Very Large Scale Integration the increasing demand for low power consumption is increased. Adder is a combinational circuit in which it represents the smallest unit used for the addition in the digital system. The adder is not only used for the arithmetic calculation in many device processors but also used in the other part of the processor for address calculations table indices, and similar operations. In these the half adder is a simpler device compared to other adders. This combinational circuit is used for the addition of two binary digits which is used for push-pop logical operation. Although adders can be constructed for many numerical representations, such as binary-coded decimal or excess-3, the most common adders operate on binary numbers. In cases where two's complement or ones' complement is being used to represent negative numbers, it is trivial to modify an adder into an adder–subtractor. Other signed number representations require a more complex adder.

Half adder is a combinational arithmetic circuit that adds two numbers and produces a sum bit (S) and carry bit (C) as the output. If A and B are the input bits, then sum bit (S) is the X-OR of A and B and the carry bit (C) will be the AND of A and B. From this it is clear that a half adder circuit can be easily constructed using one X-OR gate and one AND gate. Half adder is the simplest of all adder circuit. So if the input to a half adder have a carry, then it will be neglected it and adds only the A and B bits. That means the binary addition process is not complete and that's why it is called a half adder. A half adder is a device that can add two bits and returns the value, along with a carry value. The difference between a half adder and a full adder is that a half adder only accepts two bits, while a full adder adds two bits and a carry.

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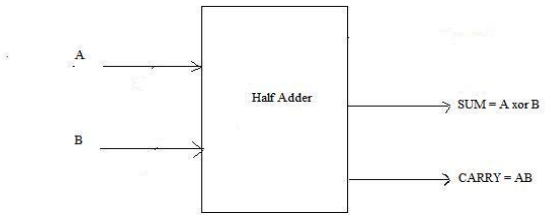

Fig 1: Logic Symbol of Half Adder

The XOR Gate is responsible for finding the sum without worrying about a carry. XOR works here because if A and B are the same, then it will return 0, and if the values are different (one is a 1, one is a 0), then it will return a 1. The AND Gate is there to handle the carry. If both A and B are 1, the XOR gate will return 0, but the AND gate will differentiate if it is (0, 0) or (1, 1) and have a carry value if it is the latter. Figure 1 shows the logic symbol of the half adder.

II.RELATED WORK

They are many papers that have published for reducing the power consumption of the arithmetic circuits such as full adder circuit and half subtractor. In these papers they have designed the circuit by using much logic design style such as Complementary Pass Transistor design style, Transmission Gate design style, Hybrid CMOS design style, Bridge design style and many. These designs are modified by using the adaptive voltage level technique which have two method such as adaptive voltage level at ground and adaptive voltage level at source based on the CMOS technology at different sizes. In these work they have many limitations which have been listed

a) The main limitation of these papers is they have designed the circuit by using the adaptive voltage level technique only for the arithmetic circuit like half subtractor and full adder excluded the circuit for the half adder.
b) The other limitation of this work is about the usage of number of transistor. They had used more number of transistors by using various design style. Due to increase in the number of transistor the reduction in power consumption would not be done up to the desired level of the technique.
c) Using this adaptive voltage level technique they had to use additional number of CMOS transistor in these work by which it increase the transistor count and leakage current of the transistor.
d) The routed wires and compiled cells which had been used in this proposed design of the arithmetic circuit such as full adder and half subtractor are more due to increase in the number of transistor used.

III.CONVENTIONAL HALF ADDER

In the conventional half adder circuit compared to the previous work the number of transistor used to design the half adder are very less. In these design we have used 3 PMOS transistor and 3 NMOS transistor to form the half adder circuit compared to the previous work it is very less in count. The leakage current of these half adder are very less compared to the previous work. The layout design of this conventional half adder circuit is simulated by using the Micro wind software. At VDD = 1.0 V the power consumption of this conventional half adder circuit is given as 5.525 micro watt on the based on the 65nm CMOS technology. In 90 nm CMOS technology the power consumption of this half adder is 10.243 micro watts. In this Conventional half adder design the number of routed wires used, the number of compiled cells and the propagation delay are reduced compared to the previous work.

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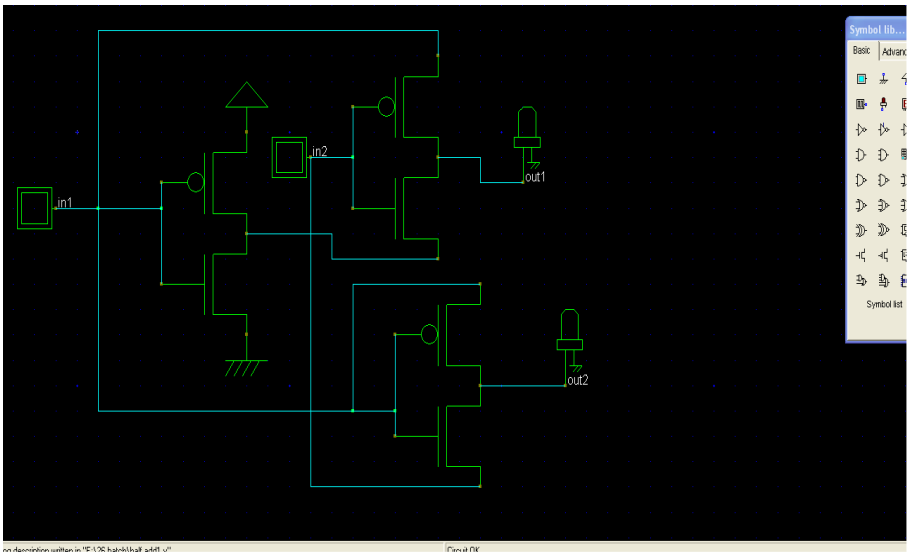

Fig 2: Conventional Half Adder circuit design

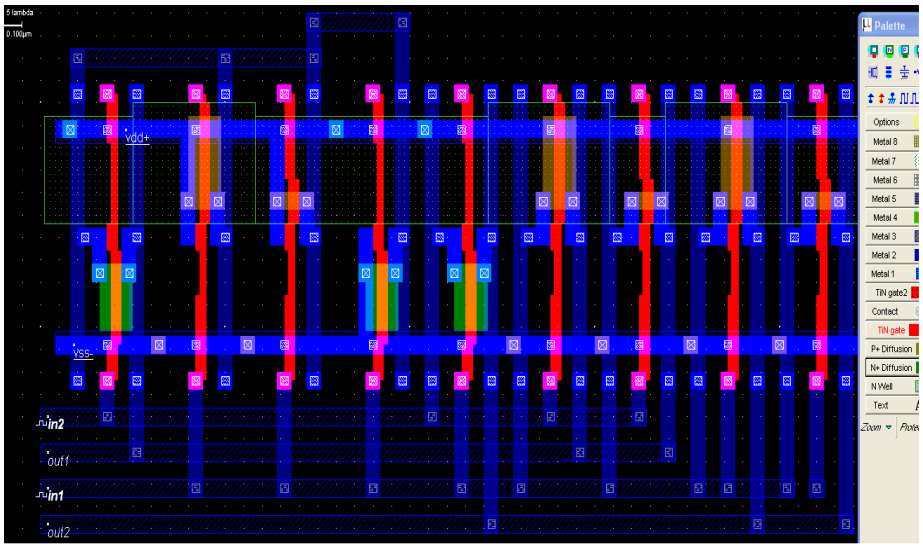

Fig 3: Conventional Half Adder design layout diagram

Figure 2 shows the conventional half adder circuit design and figure 3 shows the layout of the Conventional half adder

IV.PROPOSED WORK

A. Half adder circuit using AVL technique:

In this Adaptive Voltage Level technique the power consumption can be reduced from the conventional half adder design. In order to reduce the power consumption an additional control circuit which can be used at the upper end of the circuit to bring down the supply voltage value .It would reduce power leakage on each transistor known as Adaptive Voltage Level at Supply (AVLS) technique.

Likewise we also have another control circuit which can be use at the lower end of the circuit to lift the ground potential of the conventional half adder circuit .It would also reduce the power leakage known as Adaptive Voltage

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Level at Ground (AVLG) technique. The complete effect of these techniques on the power consumption can be described as follows.

B. Half adder circuit using AVLG technique:

In Adaptive Voltage Level at Ground (AVLG) technique the additional control circuit consists of combination of 1-NMOS and 2-PMOS transistors which are connected in parallel. Additionally an input clock is applied at the input terminal of the NMOS transistor in the control circuit and the rest of the PMOS transistors in the control circuit are connected to the ground terminal. This AVLG control circuit is placed at the ground terminal of the conventional half adder circuit. It would lift the ground potential of the circuit to reduce the power consumption of the conventional half adder design. Depending upon the input the output also varied and the usage of clock is to prevent any defect in half adder function during power consumption.

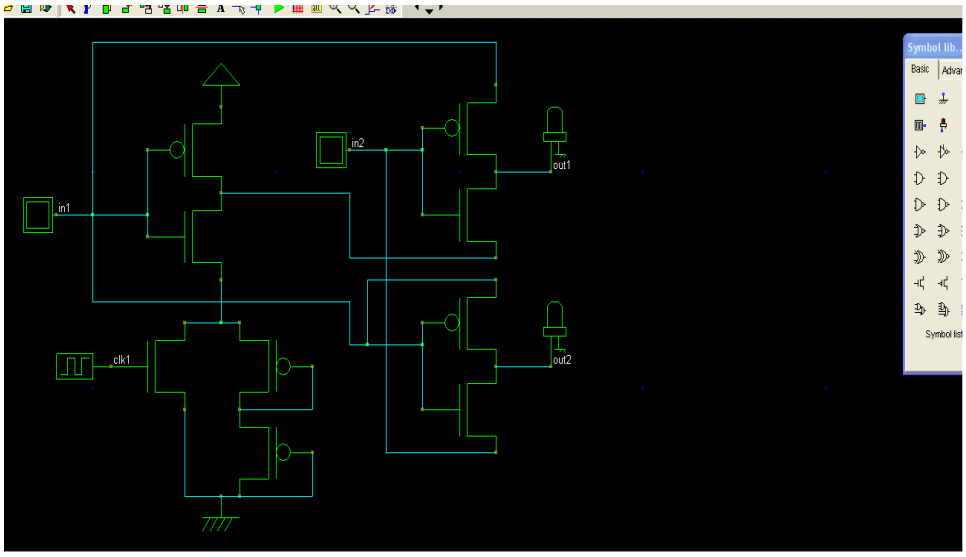

Fig 4: Half adder design using AVLG technique

Figure 4 shows the half adder design using AVLG technique. The layout of this half adder design is simulated.

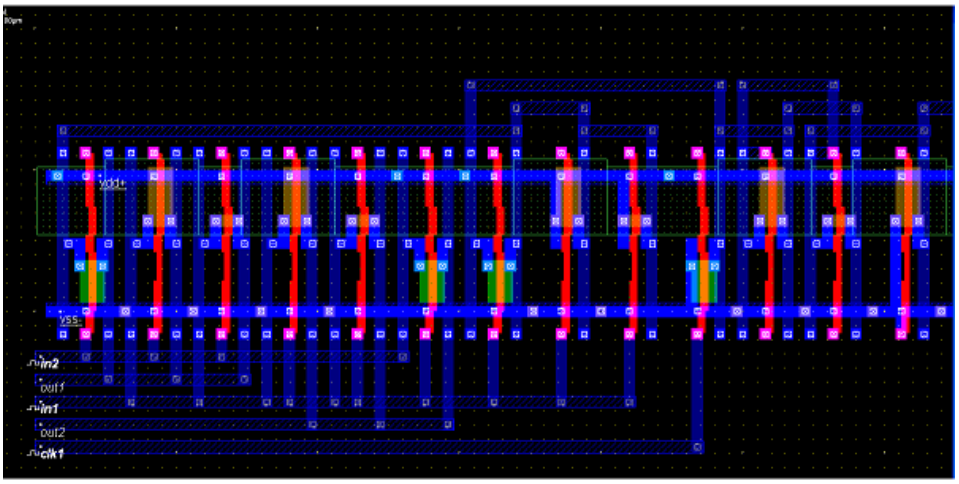

Fig 5: Layout diagram of half adder using AVLG technique.

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At VDD = 1.0 V the power consumption of this half adder design is 3.124 micro watt in 65 nm CMOS technology and the power consumption of this design on 90nm CMOS technology is about 6.741 micro watt. From this we can understood that the power consumption is reduced about 56% less when compared to the conventional half adder design.

C. Half adder circuit using AVLS technique:

In Adaptive Voltage Level at Supply (AVLS) technique the additional control circuit is made up of combination of 1 PMOS and 2 NMOS transistor connected in parallel. At which an input clock is applied at the input terminal of the PMOS transistor and the rest of the NMOS transistor is connected to the drain terminal. This AVLS control circuit is placed at voltage supply source terminal of the conventional half adder design in which supply is given through this control circuit. This control circuit at the upper end would bring down the supply voltage given to the whole circuit in order to reduce the power consumption of the conventional half adder design. When the input is varied corresponding output will be produced. It would reduce the leakage power by reducing the gate to source voltage and gate to drain voltage. This design would be responsible for very low power consumption.

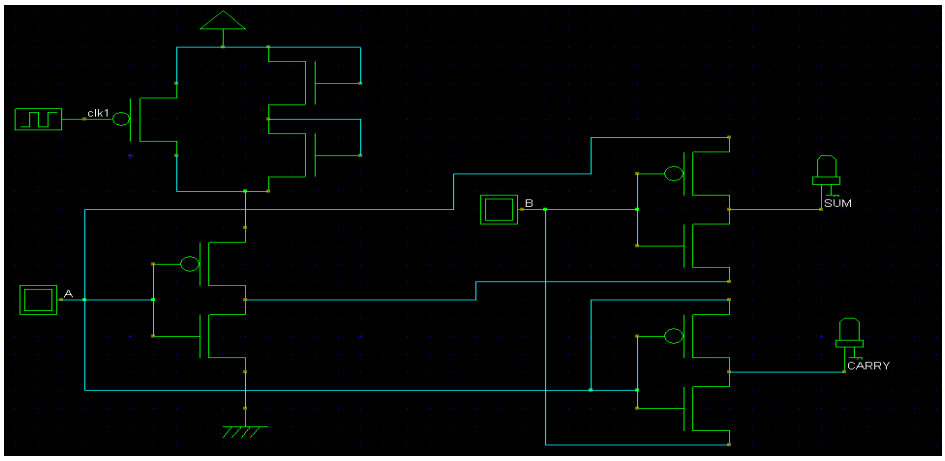

Fig 6: Half adder design using AVLS technique

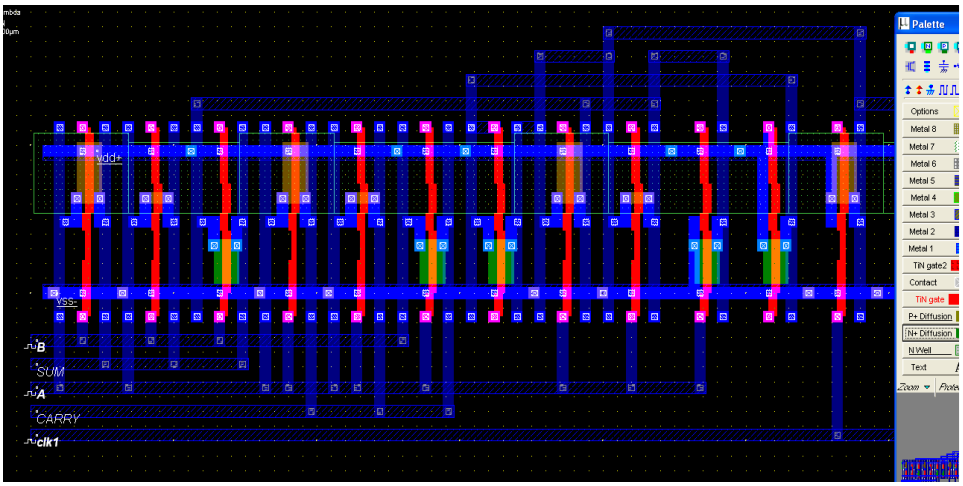

Fig 7: Layout design of half adder using AVLS technique

Figure 6 shows the half adder design using AVLS technique and the figure 7 shows the layout design of the half adder using AVLS technique which is simulated. At VDD =1.0 V the power consumption of this half adder design is about

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3.011 micro watt based on the 65nm CMOS technology. In 90nm CMOS technology the power consumption of this half adder design is about 6.406 micro watts. From this we can understand that the power consumption is reduced compared to the conventional half adder design. Compared to the AVLG technique in AVLS technique the power is reduced more efficiently.

V.SIMULATION RESULTS AND WAVEFORMS

In this we have shown the simulated results of the power consumption, propagation delay, routed wires, speed and the compiled cells in the form of tabulation and also in the form of waveform we have shown the results.

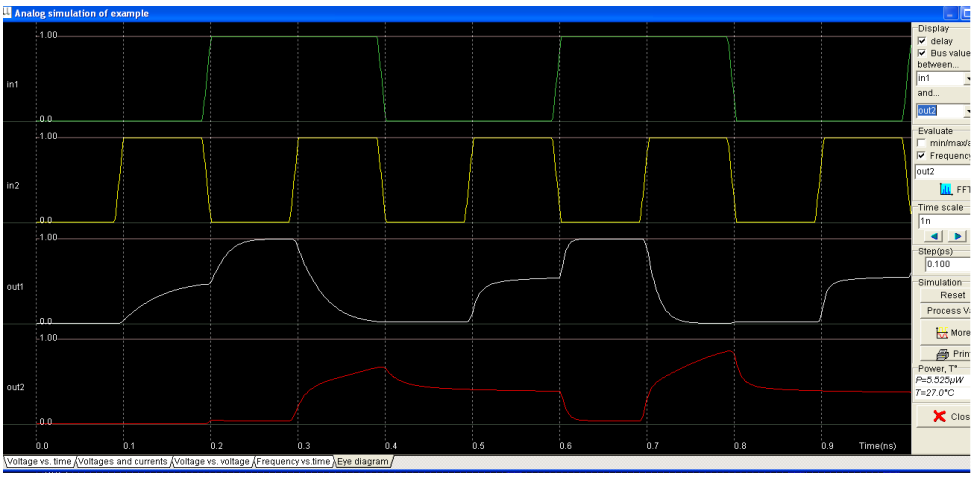

Fig 8: Simulated waveform of the conventional half adder design

Figure 8 shows the simulated waveform of the conventional half adder design and the figure 9 shows the simulation waveform of the half adder design using AVLG technique.

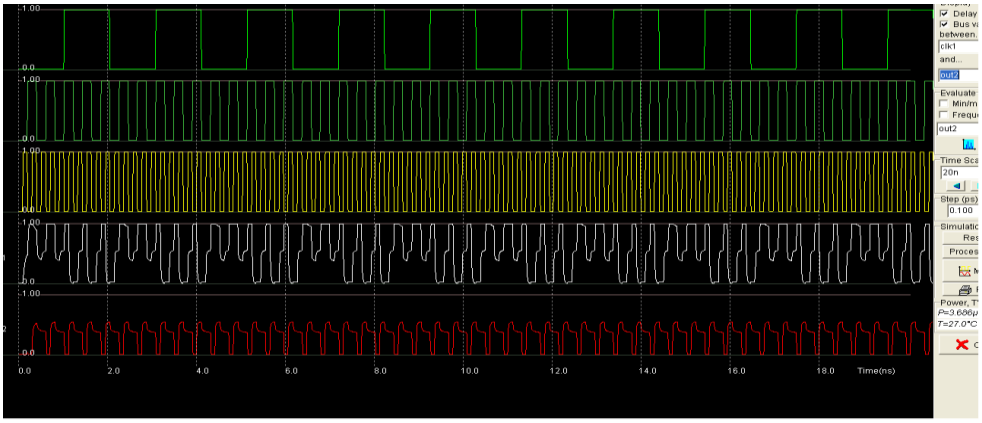

Fig 9: Simulated waveform of the half adder design using AVLG technique

Figure 10 shows the simulated waveform of the half adder design using AVLS technique. From the result we can understood that the power reduction is more in the Adaptive Voltage Level at Supply technique in designing the half adder. The parameters which can show the advantage of this adaptive voltage level technique is shown in the form of tabulation

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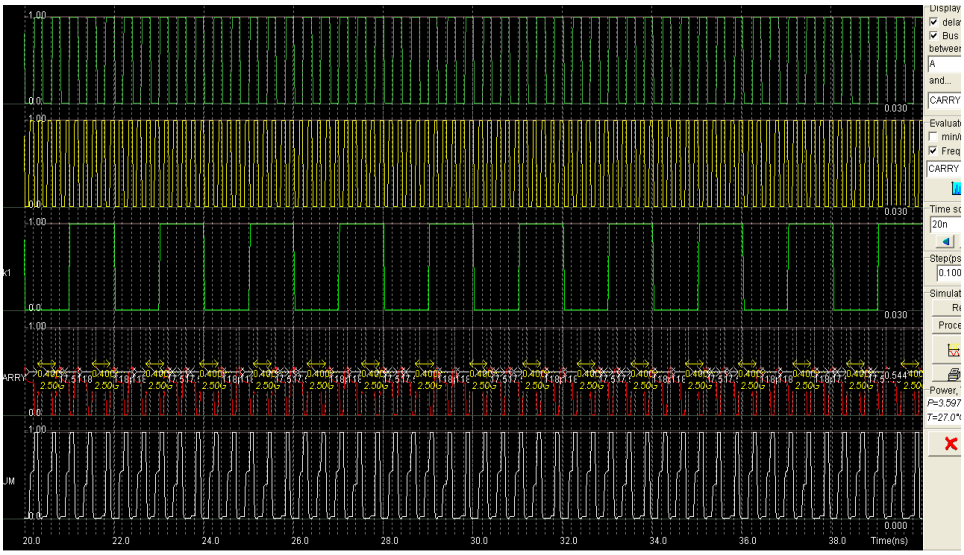

Fig 10: Simulated waveform of the half adder design using AVLS technique

S.NO	Parameters	Conventional	AVLG	AVLS
1	Power consumption (microwatt)	5.525	3.124	3.011
2	Routed wires	15	20	20
3	Compiled cells	6/6	9/9	9/9
4	Layout area (micro meter square)	20.5	36.9	36.9
5	Propagation delay (ps)	1.01	0.123	0.091
6	No .of PMOS &NMOS transistors	3,3	5,4	4,5

Table 1: Comparison of the conventional half adder with half adder using AVLG & AVLS technique on 65 nm CMOS technology

Table 1 and Table 2 shows the comparison of the conventional half adder design with the half adder using AVLG and AVLS technique. From this we can understand that the power consumption is reduced when compared to the conventional design and the half adder using AVLS technique is more efficient in consuming the power than the half adder design using AVLG technique. Leakage current is also a very important factor in designing a system. Leakage current is very small in half adder design using AVLS technique compared to other technique.

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S.NO	Parameters	Conventional	AVLG	AVLS
1	Power consumption (microwatt)	10.243	6.741	6.406
2	Routed wires	15	20	20
3	Compiled cells	6/6	9/9	9/9
4	Layout area (micro meter square)	63.0	62.5	62.5
5	Propagation delay (ps)	45	30	18
6	No .of PMOS &NMOS transistors	3,3	5,4	4,5

Table 2: Comparison of the conventional half adder with half adder using AVLG & AVLS technique on 90 nm CMOS technology

VI. CONCLUSION

The simulation result of this half adder design using AVL technique shown that the power consumption is reduced. Various parameters which have been shown in the simulation result have influence on designing in VLSI design. In this the half adder design using AVL technique are generated in both 65nm and 90nm CMOS technology to know and study about various parameters like propagation delay and the power consumption. From this parameter we can understood that the optimized half adder is produced. When compared to the other technique the AVLS design of half adder is more efficient in speed, power consumption and leakage current. It also uses less number of routed wires compared to other design technique.

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