



Fuzzy Based Interline Unified Power Quality Conditioner for Power Quality Enhancement

Dr. M. Surya Kalavathi¹, K.K. Vasishta Kumar², Mohd. Zabi.³

Professor, Dept. of EEE, JNTU College of Engineering, JNTU, Hyderabad, India¹

Assistant Professor, Dept. of EEE, GITAM School of Technology, GITAM, Hyderabad, India²

PG Student [PSA] , Dept. of EEE, GITAM School of Technology, GITAM, Hyderabad, India³

ABSTRACT: In this paper Fuzzy based Interline Unified Power Quality Conditioner (iUPQC) for power quality enhancement. A Fuzzy Logic Controller (FLC) is based on fuzzy sets and fuzzy rules with their membership functions of inputs and outputs. A control technique of two active filters is to control the sinusoidal reference. In iUPQC; Series Active Filter (SAF) works as a current source and Parallel Active Filter (PAF) works as a voltage source and due to these there is a high and low impedances occurs which is indirectly compensates the harmonics and disturbances of the grid voltage and load current and also impedance path is low harmonic at load current. To deal with sinusoidal reference for well-known frequency spectrum, a technique of pulse width modulation (PWM) is used. A simulation design control, power flow analysis is proposed in interline unified power quality controller (iUPQC) and to eliminate harmonics using a Fuzzy Logic Controller (FLC). In this paper is discussed about structure, control and capability of the iUPQC with Fuzzy Controller technique and efficiency is verified through MATLAB Simulation.

KEYWORDS: SAFs and PAFs filters, Fuzzy sets and Fuzzy rules with control design and simulation, power line conditioning.

I.INTRODUCTION

Nonlinear loads always reduces the power quality at electrical grid and contain a high harmonic which effect the critical loads. To overcome such problems we are using UPQC is low distortion of harmonic to regulate voltage from the loads and undistorted the current from the utility grid. In UPQC they are two types of filters SAF and PAF, PAF is a current source and SAF is a voltage source both of them are a non-sinusoidal reference and also compensate the harmonic in grid voltage and load current. It is a complex method to solve such problems we are using active filters to control the harmonics and to eliminate harmonics fuzzy controller. Its conditioner consists of two single-phase current source inverters where the SAF is controlled by a current loop and the PAF is controlled by a voltage loop both of them are interconnected to fuzzy controller and grid current and load voltage are sinusoidal, and therefore, their references are also sinusoidal. This concept is called “*dual topology of unified power quality conditioner*” (iUPQC), and the control schemes use the $p-q$ theory, for a real time of positive sequence. The aim of this paper is to propose Fuzzy based Interline Unified Power Quality Conditioner for power quality enhancement to eliminate the harmonic from source to load. In ABC reference the proposed control scheme is developed for the classical control theory is without the need for coordinate transformers and digital control implementation. The references to both SAF and PAF with fuzzy logic controller is a pure sinusoidal, dispensing the harmonic extraction from the grid current and load voltage.

II. DUAL UPQC

Dual iUPQC its structure is shown in Fig.1. In the iUPQC, the SAF works as a current source and PAF works as a voltage source both of them are synchronized with the grid voltage uses sinusoidal references to the classical topology for both active filters. The high impedance occurs at SAF to indirectly compensate the harmonics, unbalances, and disturbances of the grid voltage. The connection transformer voltages are equal to the difference between the grid voltage and the load voltage. In the same way, the PAF indirectly compensates the unbalances, displacement, and harmonics of the grid current, providing a low-impedance path for the harmonic load current.

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 4, April 2015

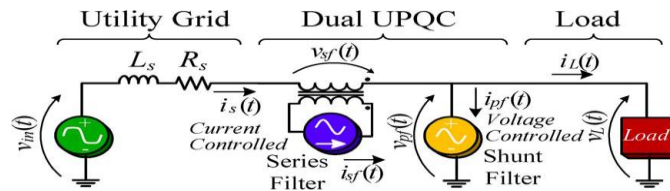


Fig.1Dual UPQC (iUPQC).

III.FUZZY LOGIC CONTROL

FLC determined by the set of linguistic rules. The mathematical modeling is not required in fuzzy controller due to the conversion of numerical variable into linguistic variables. FLC consists of three part: a. Fuzzification, b. Interference engine, c. Defuzzification. The fuzzy controller is characterized as; For each input and output there are seven fuzzy sets. For simplicity a membership functions is Triangular. Fuzzification is using continuous universe of discourse. Implication is using Mamdani's "min" operator. Defuzzification is using the "height" method. FLC block diagram as shown in figure 2.

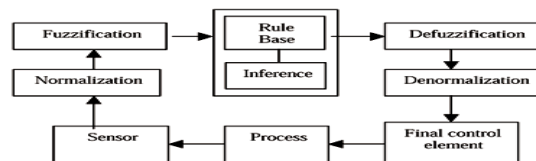


Fig.2 Fuzzy Logic Controller

a. Fuzzification

Membership function values are assigned to the linguistic variables, using seven fuzzy subsets: NB (Negative Big), NM (Negative Medium), NS (Negative Small), ZE (Zero), PS (Positive Small), PM (Positive Medium) and PB (Positive Big). The partition of fuzzy subsets and the shape of membership function adapt the shape up to appropriate system. Input error $E(k)$ and change in error $CE(k)$ of values which is normalized by an input scaling factor as shown in table 1.

Table 1: Fuzzy Rules

$\frac{e}{\Delta e}$	NB	NM	NS	ZE	PS	PM	PB
NB	NB	NB	NB	NB	NM	NS	ZE
NM	NB	NB	NB	NM	NS	ZE	PS
NS	NB	NB	NM	NS	ZE	PS	PM
ZE	NB	NM	NS	ZE	PS	PM	PB
PS	NM	NS	ZE	PS	PM	PB	PB
PM	NS	ZE	PS	PM	PB	PB	PB
PB	ZE	PS	PM	PB	PB	PB	PB

In this system the input scaling factor is between -1 and +1 has design. The triangular shape of the membership function of this arrangement presumes that for any particular input there is only one dominant fuzzy subset. The input error $E(k)$ and change in error $C(k)$ for the FLC is given as

$$E(K) = \frac{P_{ph(K)} - P_{ph(K-1)}}{V_{ph(K)} - V_{ph(K-1)}} \quad (1)$$

$$C(K) = E(K) - E(K - 1) \quad (2)$$

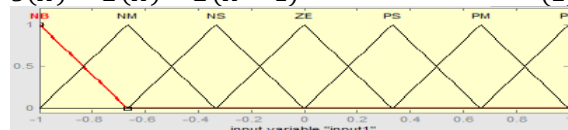


Fig.3 Input1 Membership function

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 4, April 2015

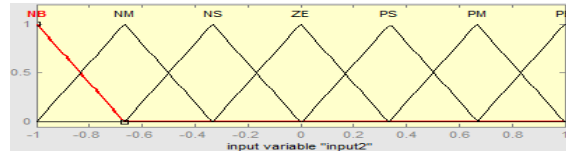


Fig.4 Input2 Membership function.

b. Inference Method

Several composition methods such as Max–Min and Max-Dot have been proposed and Min method is used. Minimum operator and Maximum operator of output membership function is of each rule and it is shown in Table 1.

c. Defuzzification

As a plant usually requires a non-fuzzy value of control, a defuzzification stage is needed. To compute the output of the FLC, "height" method is used and the FLC output modifies the control output. Further, the output of FLC controls the switch in the inverter. In order to control these parameters, they are sensed and compared with the reference values. To achieve this, the membership functions of Fuzzy controller are: error, change in error and output as shown in Figs. (3), (4). In the present work, for fuzzification, nonuniform fuzzifier has been used. If the exact values of error and change in error are small or large, they are divided conversely.

$$u = -[\alpha E + (1 - \alpha) * c] \quad (3)$$

The α is self-adjustable factor and to regulate operation. E is the error of the system, C is the change in error and u is the control variable. If the system is not in balanced it indicates an error 'E' if the value is large. While the error 'E' value is small it indicates that the system is near to balanced state. If system is unbalanced, the control variables should be enlarge to balance the system as early as possible. For system stability overshoot plays an important role. For restraining oscillations and system stability it requires less overshoot. 'C' plays an important role, while the role of 'E' is diminished. The optimization is done by α . The set of Fuzzy controller rules is given in Table 1.

IV. POWER CIRCUIT

The power circuit of the proposed scheme of iUPQC is made up of two four-wire three-phase converters connected back to back and their respective output filters, as shown in Fig.5. Three single-phase transformers are used to connect the SAF to the utility grid, and PAF is connected to the load. The specification of the iUPQC as shown in Table 2. The passive components are shown in Table 3.

TABLE 2: DESING SPECIFICATION OF iUPQC

Input line to line RMS voltage	$V_{in}=220V$
Output nominal power	$P_o=2500VA$
DC link voltage	$V_b=400V$
Utility grid frequency	$f_{grid}=50Hz$
Switching frequency of SAFs and PAFs	$f_s=20KHz$
Transformer ratio	$n=1$

TABLE 3: COMPONENT SPECIFICATION OF POWER MODULES

Leakage inductance of SAF coupling Transformer	$L_{lg}=2.33\text{mH}$
Transformer ratio of the SAF coupling Transformer	$n=1$
SAF connection inductance	$L_{sf}=650\mu\text{H}$
PAF connection inductance	$L_{pf}=650\mu\text{H}$
DC Link Capacitance	$C_b=3\text{mF}$

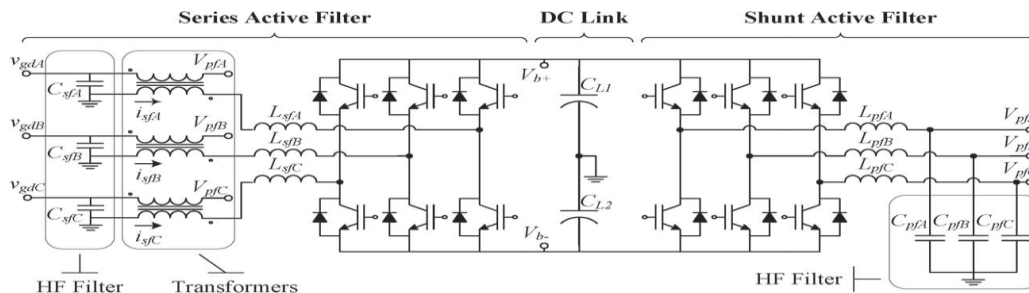


Fig.5 Power circuit of the iUPQC.

V. OUTPUT PASSIVE FILTER DESIGN

Single-phase wiring diagram of iUPQC, is shown in Fig. 6. The grid impedance is $Z_s = j\omega L_s + R_s$, and leakage impedance of coupling transformer is $Z_{lg} = j\omega L_{lg} + R_{lg}$, in series and shunt filters, the voltage sources is v_{sc} and v_{pc} and the harmonic which are generated from the switches are composed by the components. The high frequency of iUPQC is filtered by the output passive filters for sinusoidal grid current and load voltage as shown in Fig.6. SAF and PAF output impedances is shown in Fig.7 and Fig.8. The current source is in series and connected to voltage source v_{sc} and inductance L_{sf} , in PAF. The transfer function of PAF in high-frequency filter is derived in equation (3) and circuit is shown in Fig.8.

$$\frac{v_L(s)}{v_{pc}(s)} = \frac{1}{L_{pf} C_{pf}} \cdot \frac{1}{s^2 + s \cdot \frac{1}{C_{pf} R_L} + \frac{1}{L_{pf} C_{pf}}} \quad (3)$$

Power design of inductor L_{pf} , and cutoff frequency of filter capacitor C_{pf} which is of 2.9-kHz and $10\mu\text{F}$. The transfer function of SAF in high-frequency filter is derived in equation (4) and circuit is shown in Fig.7. and also the α, β, γ equations (5),(6) and (7).

$$\frac{i_s(s)}{v_s(s)} = \frac{n}{sL_{sf} + [n^2[sL_{tg} + R_{tg} + \alpha + \beta]\gamma]} \quad (4)$$

where,

$$\alpha = \frac{sL_{pf} R_L}{s^2 L_{sf} C_{pf} R_L + sL_{sf} + R_L} \quad (5)$$

$$\beta = \frac{sL_{rd} + R_{rd}}{s^2 L_s C_{sf} + sC_{sf} R_s + 1} \quad (6)$$

$$\gamma = s^2 C_{sf} L_s + sC_{sf} R_{lg} + 1 \quad (7)$$

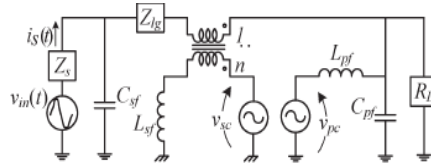


Fig.6 Single-phase wiring diagram of the dual UPQC.

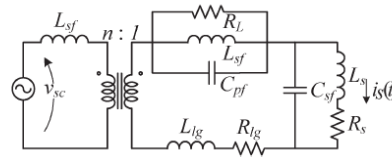


Fig.7 Equivalent circuit as viewed by SAF.

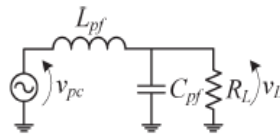


Fig.8 Equivalent circuit as viewed by PAF.

Here cutoff frequency of filter capacitor C_{pf} which is of 45-kHz and $1\mu\text{F}$. The low cutoff frequency response is reduce the filter bandwidth of the SAF, and grid voltage contents the harmonic. The leakage impedance of coupling transformers is of low-frequency attenuation is undesirable and intrinsic towards the characteristic. As per the previous articles, it deal with the same iUPQC control strategy, the output filter of inductor is impose of voltage and SAF current and through the filter its frequency is sinusoidal with current. It is a narrow band frequency control to distort the current drained from the utility grid. The usage of high-power coupling transformers, with low leakage inductance, and the design of higher voltage dc link, allowing the imposition of higher current rate of change on the filter output inductor, and solutions to change the characteristics of the filter in low frequencies.

VI. PROPOSED CONTROL SCHEME

The proposed iUPQC control structure is an ABC reference frame based on the compensation of harmonics, unbalances, disturbances, and displacement . To compensate we are using the SAF is a current loop and PAF is a voltage loop in order to ensure the sinusoidal grid current and load voltage with low harmonic distortion. The dc link voltage is a reference amplitude for the current loop, in the power factor converter control schemes of SAF. With the sinusoidal references for both SAF and PAF controllers are generated by a digital signal processor (DSP), and to ensure the grid voltage synchronism using a phase locked loop.

A. SAF Control

The control scheme of SAF as shown in Fig.9. It consists of two voltage loops and three current loops which are identical to grid. The total dc link voltage is regulated to one voltage loop and another voltage loop is avoiding the unbalance towards dc link capacitors and grid current is independently tracking to each grid input reference. For a low-frequency of total dc link voltage control loop and its response is determined the reference amplitude for the current loops. Due to these we can increase the load to overcoming input of grid current and to decrease the voltage of an dc link supplies of an resultant active power consumption. The grid current reference is increased by voltage controller to restore the dc link voltage. The neutral point of three phase four wire converter is represent by the circuit is shown in Fig.9 and current source is parallel with the dc link impedance and its source is average charge of current . The resistor R_b is infinite ($R_b \rightarrow \infty$); in a circuit to represent instantaneous active power consumption of the dc link is related to switching period is null for the utility grid voltage frequency. The average charge current of the dc link is given by

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 4, April 2015

$$I_{eq} = \frac{3}{2} \cdot \frac{n \cdot V_{gdpk} \cdot I_{sfpk}}{V_b} \quad (8)$$

$$G_{vsf}(s) = \frac{V_b(s)}{I_{sf}(s)} = \frac{3}{2} \cdot n \cdot \frac{V_{gdpk}}{V_b} \cdot \frac{1}{\frac{1}{R_b + sC_b}} \quad (9)$$

Where, V_{gdpk} Peak of the grid voltage;

V_b DC link voltage;

R_b Load equivalent resistance;

C_b Total dc link equivalent capacitance;

n Transformer ratio.

The open loop transfer function (*OLTF*_v) is given by

$$OLTFv(s) = G_{vsf}(s) \cdot \frac{K_{vsf}}{K_{isf}} \cdot K_{mfs} \quad (10)$$

where,

K_{mfs} multiplier gain;

K_{vsf} voltage sensor gain;

K_{isf} current sensor gain.

The K_{mfs} is of multiplier integrated circuit and the peak signal generated by the DSP.

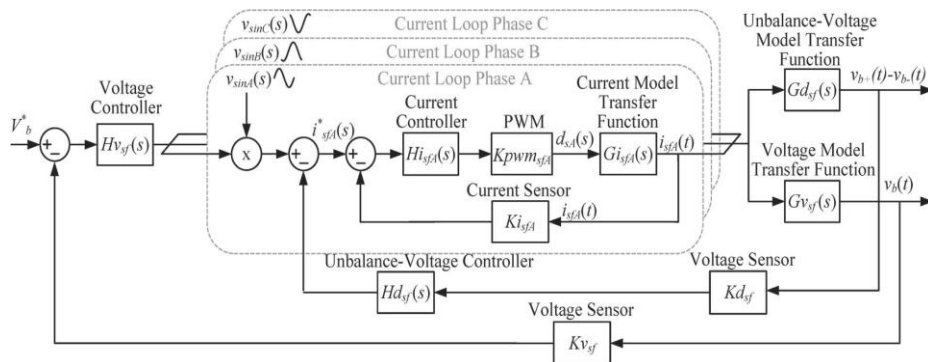


Fig.9 Control block diagram of the SAF controller.

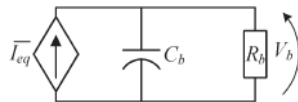


Fig.10 Equivalent circuit of the SAF voltage loop.

A proportional integral (PI) controller is designed to regulate, and ensures a crossover frequency of 4 Hz and a phase margin of 45° with total voltage loop frequency, and including the open-loop transfer function (*OLTF*_v), controller transfer function ($H_{v_{sf}}$), compensated loop transfer function ($OLTF_v + H_{v_{sf}}$). Under the unbalanced voltage loop condition the grid current reference is $i_{sc(t)}$ and C_{L1} and C_{L2} is equilibrium the voltage loop in a dc link capacitor. To analysis of these function a current $i_{sc(t)}$ is a neutral point, and $d(t)$ is a duty cycle. The single-phase four wire convertor is of two current sources on the inverter switches. The unbalanced voltage loop transfer function is obtained by mesh analysis and Laplace is given by

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 4, April 2015

$$G_{d_{sf}(s)} = \frac{V_{b+(s)} - V_{b-(s)}}{I_{sc}(s)} = \frac{3}{2 \cdot s \cdot C_b} \quad (11)$$

The open-loop transfer function ($OLTF_d$) is given by

$$OLTF_{d(s)} = G_{d_{sf}(s)} \cdot \frac{K_{d_{sf}}}{K_{i_{sf}}} \quad (12)$$

Where, $K_{d_{sf}}$ Differential voltage sensor gain.

A proportional integral (PI) controller is designed to eliminate, and ensures a crossover frequency of 0.5Hz and a phase margin of 50° with frequency of differential voltage loop, and including the open-loop transfer function ($OLTF_d$), controller transfer function ($H_{d_{sf}}$), compensated loop transfer function ($OLTF_d + H_{d_{sf}}$). It consists of three identical current loops, except for the 120° phase displacements. To decoupling the voltage loop and its source on the coupling transformer and the current loop transfer function as shown in Fig.11. The dynamic model of an circuit has an average value related to the switching period and voltage $v_{s(t)}$ and $v_{L(t)}$ are constants. The current loop transfer function and small signal is analyzed by Laplace is given

$$G_{i_{f}(s)} = \frac{I_{sc}(s)}{D(s)} = \frac{V_b}{sA_1 + n^2 \cdot (R_s + R_{lg})} \quad (13)$$

where,

$$A_1 = n^2 \cdot (L_s + L_{lg}) + L_{sf} \quad (14)$$

and

L_s series grid inductance;

R_s series grid resistance;

L_{lg} leakage inductance of the coupling transformer;

R_{lg} series resistance of the coupling transformer.

The open-loop transfer function ($OLTF_i$) is given by

$$OLTF_{i(s)} = G_{i_{sf}(s)} \cdot K_{p_{wmsf}} \cdot K_{i_{sf}} \quad (15)$$

where,

$K_{p_{wmsf}}$ series filter pulse width modulation (PWM) modulator gain and its equal to the inverse peak value of the triangular carrier.

A proportional integral (PI) controller is designed to tack the current reference, and ensures a crossover frequency of 5 kHz and a phase margin of 70° with frequency response of current loop, and including the open-loop transfer function ($OLTF_i$), controller transfer function ($H_{i_{sf}}$), compensated loop transfer function ($OLTF_i + H_{i_{sf}}$).

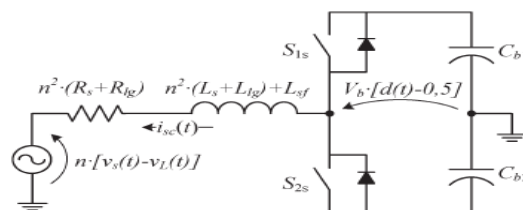


Fig.11 Single-phase equivalent circuit of SAF.

B. PAF Control

A control block diagram of shunt active filter is shown in Fig.12. The control scheme of three identical load voltage and towards feedback loops in 120° phase displacement. The transfer function of voltage loop is analyzed by a single-phase equivalent circuit as shown in Fig.13. The voltage loop transfer function is using average values for switching period and small signal is analyzed by Laplace is given

$$G_{v_{pf}(s)} = \frac{V_b}{L_{pf} C_{pf}} \cdot \frac{1}{s^2 + s \left(\frac{1}{C_{pf} R_L} \right) + \frac{1}{L_{pf} C_{pf}}} \quad (16)$$

where, $G_{v_{pf}(s)} = \frac{V_L(s)}{D(s)}$

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 4, April 2015

The open-loop transfer function ($OLTF_{v_{pf}}$) is given by

$$OLTF_{v(s)} = G_{vsf}(s) \cdot K_{pwm_{pf}} K_{v_{pf}} \quad (17)$$

Where,

$K_{pwm_{pf}}$ shunt filter PWM modulator gain.

A additional (PID) pole controller is designed to track the voltage reference, and ensures a crossover frequency in a proportional integral derivate of 4 kHz and a phase margin of 35° with frequency response of voltage loop, and including the open-loop transfer function ($OLTF_{v_{pf}}$), controller transfer function ($H_{v_{pf}}$), compensated loop transfer function ($OLTF_{v_{pf}} + H_{v_{pf}}$).

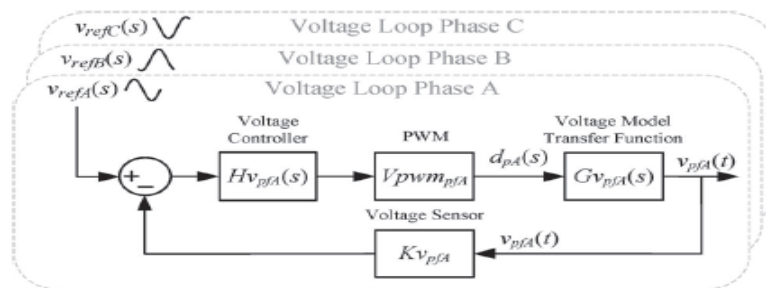


Fig.12 Control block diagram of the PAF voltage loop.

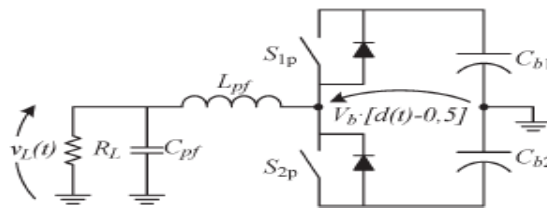
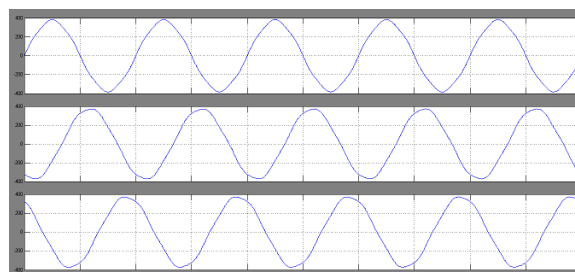


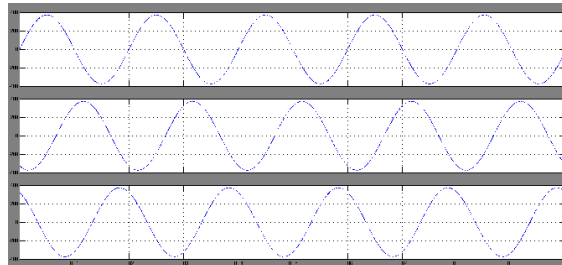
Fig.13 Single-phase equivalent circuit of PAF.

VII.RESULT

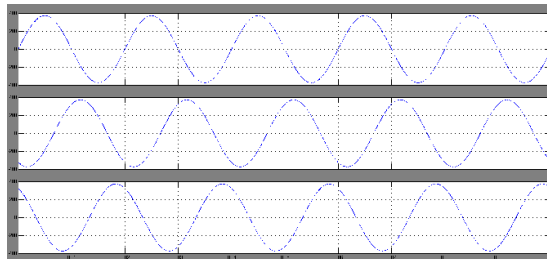
The result is obtained through fuzzy based Interline Unified Power Quality Conditioner for power quality enhancement. From grid source to load we are eliminating the harmonics using SAF and PAF filters and Fuzzy Logic Controller and injecting the dip voltage and compensating with DC link current load to discrete the RMS voltage. Hence the result output is without harmonics from grid source to load.



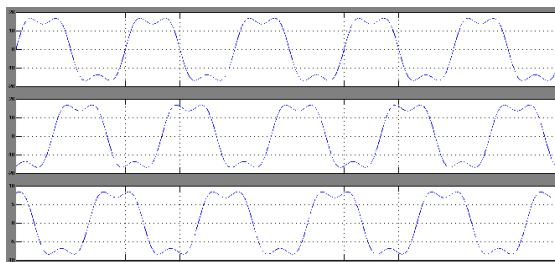
(a) Vabc.



(b) Iabc.

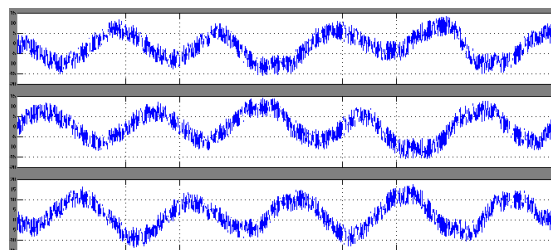


(c) Vabc.

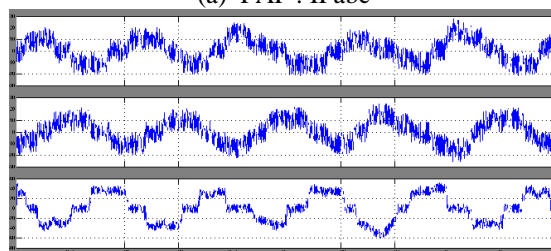


(d) Iabc.

Fig.14. (a),(b),(c) Waveform of normal source to load voltage and (d) source to load current with harmonic.



(a) PAF : IFabc



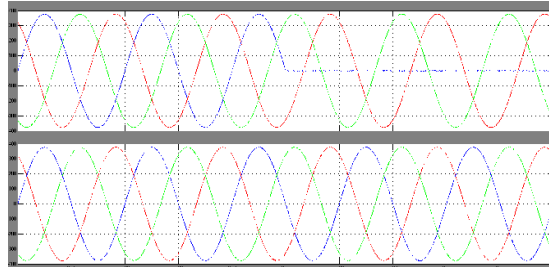
(b) SAF: VFabc.

Fig.15. (a),(b) Waveform of PAF current, SAF voltage with harmonic.

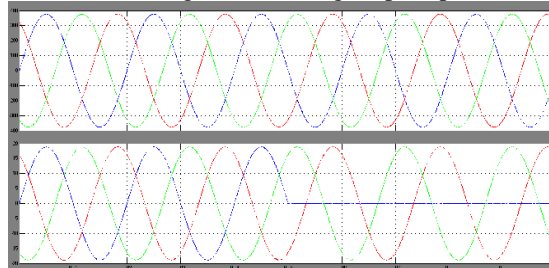
International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 4, April 2015

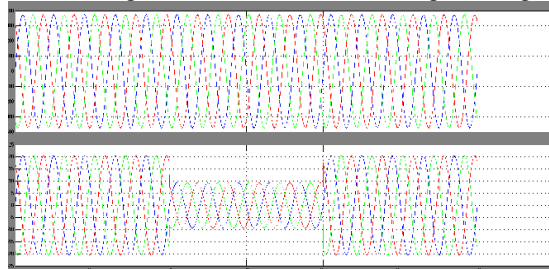


(a) Waveform of three phase source voltages with voltage dip in phase A and load voltage with FLC.

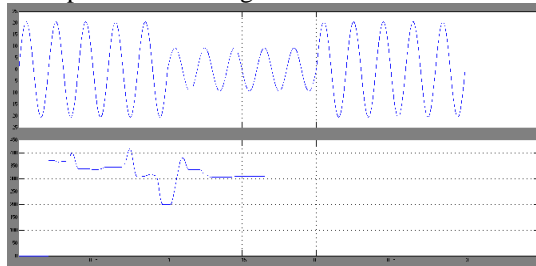


(b) Waveform of three phase load current and source currents with voltage dip in phase A with FLC.

Fig.16. (a) Waveform of three phase source voltages and load voltages during a voltage dip in phase A with FLC. (b) Waveform of three phase load voltage and source currents during a voltage dip in phase A with FLC.



(a) Waveform of three phase load voltages and load currents: -Vabcl, Iabcl with FLC.



(b) Waveform of three phase load current Iabcl with DC link voltages with discrete RMS with FLC.

Fig.17. (a) Waveform of three phase load voltages and load current during a load step from 100% to 50% and 50% to 100% with FLC. (b) Waveform of DC link voltages and load current during a load step from 100% to 50% with FLC.

VIII. CONCLUSION

The results is through with iUPQC using Fuzzy Logic Controller and design with Matlab Simulation Technique in ABC reference frame and using series active filter and parallel active to compensate the harmonics from nonlinear load current. A fuzzy code designed to control something, which may be a software or hardware is used from small circuits to large mainframes. First create the membership values (fuzzify) and specify the rule table and also determine your procedure for defuzzifying the result. A proposed scheme of iUPQC using fuzzy controller in ABC reference frame of both the active filters and their control loops are generated by a digital signal processor (DSP) and to related to other proposed controls its utilization is better for a sinusoidal reference and to eliminate the harmonic from source to load.



International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 4, April 2015

Both the active filters from source to load are dip by the RMS voltage in phase "A" to eliminate the harmonics from grid source voltage to load current using fuzzy controller. Thus the result is validated and its proposed scheme of ABC reference of iUPQC using fuzzy control method is used in synchronized sinusoidal reference.

REFERENCES

- [1] Hamid Reza Mohammadi, Ali Yazdian Varjani, and Hossein Mokhtari, "Multiconverter Unified Power-Quality Conditioning System: MC-UPQC" IEEE TRANSACTIONS ON POWER DELIVERY, VOL. 24, NO. 3, JULY 2009.
- [2] R.Rezaei pour and A.Kazemi, "Review of Novel control strategies for UPQC" Internal Journal of Electric and power Engineering 2(4) 241-247, 2008.
- [3] S. Ravi Kumar and S.Siva Nagaraju " Simulation of DSTATCOM and DVR in power systems" Vol. 2, No. 3, June 2007 ISSN 1819-6608 ARPN Journal of Engineering and Applied Sciences.
- [4] M.V.Kasuni Perera" Control of a Dynamic Voltage Restorer to compensate single phase voltage sags" Master of Science Thesis Stockholm, Sweden 2007.
- [5] M. Basu, S. P. Das, and G. K. Dubey, "Comparative evaluation of two models of UPQC for suitable interface to enhancement power quality," Elect.Power Syst. Res., pp. 821– 830, 2007.
- [6] A. K. Jindal, A. Ghosh, and A. Joshi, "Interline unified power quality conditioner," IEEE Trans. Power Del. vol. 22, no. 1, pp.364–372, Jan. 2007.
- [7] P.Hoang, K.Tomosovic, "Design and an analysis an adaptive fuzzy power system stabilizer", Vol. 11, No. 2, June 1996.
- [8] Momoh, X. W. Ma, "Overview and Literature survey of Fuzzy set theory in power systems", IEEE Trans.on Power Systems, Vol. 10, No.3, Aug. 1995. pp. 1676-1690.
- [9] M. Basu, S. Das, and G. Dubey, "Investigation on the performance of UPQC-Q for voltage sag mitigation and power quality improvement at a critical load point," IET Gen. Transmiss. Distrib., vol. 2, no. 3, pp. 414–423, May 2008.
- [10] V. Khadkikar and A. Chandra, "A new control philosophy for a unified power quality conditioner (UPQC) to coordinate load-reactive power demand between shunt and series inverters," IEEE Trans. Power Del., vol. 23, no. 4, pp.2522–2534, Oct. 2008.
- [11] M. Aredes and R. Fernandes, "A dual topology of unified power quality conditioner: The iUPQC," in Proc. 13th Eur.Conf. Power Electron. Appl., Sep. 2009, pp. 1–10.
- [12] M. Brenna, R. Faranda, and E. Tironi, "A new proposal for power quality and custom power improvement: OPEN UPQC," IEEE Trans. Power Del., vol. 24, no. 4, pp. 2107–2116, Oct. 2009.
- [13] V. Khadkikar and A. Chandra, "A novel structure for three- phase four-wire distribution system utilizing unified power quality conditioner (UPQC)," IEEE Trans. Ind. Appl., vol. 45, no. 5, pp. 1897–1902, Sep./Oct. 2009.
- [14] K. H. Kwan, Y. C. Chu, and P. L. So, "Model-based H_∞ control of a unified power quality conditioner," IEEE Trans. Ind. Electron., vol. 56, no. 7, pp. 2493–2504, Jul. 2009.
- [15] J. Munoz, J. Espinoza, L. Moran, and C. Baier, "Design of a modular UPQC configuration integrating a components economical analysis," IEEE Trans. Power Del., vol. 24, no.4 pp. 1763–1772, Oct. 2009.