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Low Power Pass Transistor Logic Flip Flop

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ABSTRACT: In this brief, a low-power flip-flop (FF) design PTLFF: Pass Transistor Logic Flip Flop is presented. The pro-posed design successfully adopts two measures to overcome the problems associated with existing P-FF designs. The first one is reducing the number of nMOS transistors stacked in the discharging path. The second one is supporting a mechanism to conditionally enhance the pull down strength when input data is "1." long discharging path problem in conventional explicit type pulse-triggered FF (P-FF) designs and achieves better speed and power performance. Based on post-layout simulation results using TSMC CMOS 90-nm technology, the proposed design outperforms the conventional P-FF design by using only 17 transistors. The average power delay is reduced to 3.57 μW.

KEYWORDS*:* Flip-flop (FF), low power, pulse-triggered.

I. INTRODUCTION

Flip-flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. In particular, digital designs now a-days often adopt intensive pipelining techniques and employ many FF-rich modules such as register file, shift register, and first in-first out. It is also estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is as high as 50% of the total system power. FFs thus contribute a significant portion of the chip area and power consumption to the overall system design [1], [2].

Pulse-triggered FF (P-FF), because of its single-latch structure, is more popular than the conventional transmission gate (TG) and master–slave based FFs in high-speed applications. Besides the speed advantage, its circuit simplicity lowers the power consumption of the clock tree system. A P-FF consists of a pulse generator for strobe signals and a latch for data storage. If the triggering pulses are sufficiently narrow, the latch acts like an edge-triggered FF. Since only one latch, as opposed to two in the conventional master–slave configuration, is needed, a P-FF is simpler in circuit complexity. This leads to a higher toggle rate for high-speed operations [3]–[8]. P-FFs also allow time borrowing across clock cycle boundaries and feature a zero or even negative setup time. Despite these advantages, pulse generation circuitry requires delicate pulse width control to cope with possible variations in process technology and signal distribution network. In [9], a statistical design framework is developed to take these factors into account. To obtain balanced performance among power, delay, and area, design space exploration is also a widely used technique [10]–[13].

The proposed design, as shown in Fig. 2.2, adopts two measures to overcome the problems associated with existing P-FF designs. The first one is reducing the number of nMOS transistors stacked in the discharging path. The second one is supporting a mechanism to conditionally enhance the pull down strength when input data is "1." Refer to Fig. 2.2, As opposed to the transistor stacking design in Fig.2.1(a),(b),(c),(d) and (e), this PFF design discharging path using PTL.Transistor N2, in conjunction with an additional transistor N3, forms a two-input pass transistor logic (PTL)-based AND gate to control the discharge of transistor N1. Since the two
inputs to the AND logic are mostly complementary (except during the transition edges of the clock), the output node Z is kept at zero most of the time. When both input signals equal to "0" (during the falling edges of the clock),temporary floating at node Z is basically harmless. At the rising edges of the clock, both transistors N2 and N3 are turned on and collaborate to pass a weak logic high to node Z, which then turns on transistor N1 by a time span defined by the delay inverter I1. The switching power at nodeZ can be reduced due to a diminished voltage swing. Unlike the MHLLF design , where the discharge control signal is driven by a single transistor, parallel conduction of two nMOS transistors

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(N2 and N3) speeds up the operations of pulse generation.With this design measure, the number of stacked transistors along the discharging path is reduced and the sizes of transistors N1-N3 can be reduced also.

II. CONVENTIONAL P-FF DESIGNS

PF-FFs, in terms of pulse generation, can be classified as an implicit or an explicit type. In an implicit type P-FF, the pulse generator is part of the latch design and no explicit pulse signals are generated. In an explicit type P-FF, the pulse generator and the latch are separate . Without generating pulse signals explicitly, implicit type P-FFs is in general more power-economical. However, they suffer from a longer discharging path, which leads to inferior timing characteristics. Explicit pulse generation, on the contrary, incurs more power consumption but the logic separation from the latch design gives the FF design a unique speed advantage. Its power consumption and the circuit complexity can be effectively reduced if one pulse generator is shares a group of FFs (e.g., an *n*-bit register). In this brief, we will thus focus on the explicit type P-FF designs only.

2.1(a).EP-DCO: explicit -Data closed to output Flip-Flop

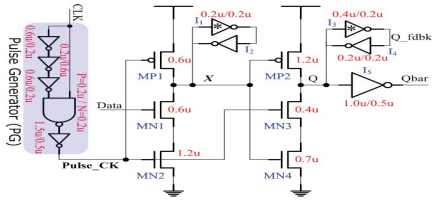

Fig.2.1(a) EP-DCO

To provide a comparison, some existing P-FF designs are reviewed first. Fig. 2.1(a) shows a classic explicit P-FF design, named data-closet- to- output (ep-DCO) . It contains a NAND-logic-based pulse generator and a semidynamic true-single-phase-clock (TSPC) structured latch design. In this P-FF design, inverters I3 and I4 are used to latch data, and inverters I1 and I2 are used to hold the internal node *X*. The pulse width is determined by the delay of three inverters. This design suffers from a serious drawback, i.e., the internal node *X* is discharged on every rising edge of the clock in spite of the presence of a static input "1." This gives rise to large switching power dissipation. To overcome this problem, many remedial measures such as conditional capture, conditional precharge, conditional discharge, and conditional pulse enhancement scheme have been proposed .

2.1.(b)CDFF: conditional discharged Flip- Flop

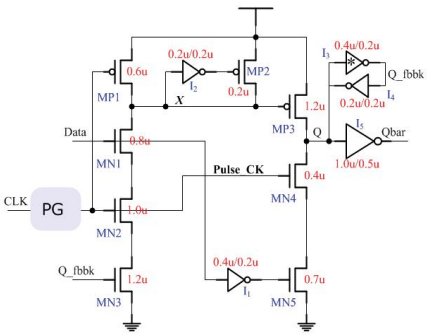

Fig.2.1(b)CDFF

Fig. 2.1(b) shows a conditional discharged (CD) technique .An extra nMOS transistor MN3 controlled by the output signal Q_fdbk is employed so that no discharge occurs if the input data remains "1." In addition, the keeper logic for the internal node *X* is simplified and consists of an inverter plus a pull-up pMOS transistor only.

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2.1.(c).SCDFF: Static- conditional discharged Flip-Flop

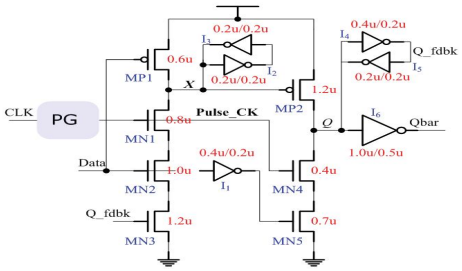

Fig.2.1(c) SCDFF

Fig. 2.1(c) shows a similar P-FF design (SCDFF) using a static conditional discharge technique . It differs from the CDFF design in using a static latch structure. Node *X* is thus exempted from periodical precharges. It exhibits a longer data-to-Q (D-to-Q) delay than the CDFF design. Both designs face a worst case delay caused by a discharging path consisting of three stacked transistors, i.e., MN1–MN3. To overcome this delay for better speed performance, a powerful pull-down circuitry is needed, which causes extra layout area and power consumption. The modified hybrid latch flip-flop (MHLFF).

2.1.(d).MHLFF: Modified hybrid latch flip flop

Fig. 2.1(d) also uses a static latch. The keeper logic at node *X* is removed. A weak pull-up transistor MP1 controlled by the output signal Q maintains the level of node *X* when Q equals 0. Despite its circuit simplicity, the MHLFF design encounters two drawbacks. First, since node *X* is not predischarged, a prolonged 0 to 1 delay is expected. The delay deteriorates further, because a level-degraded clock pulse (deviated by one VT) is applied to the discharging transistor MN3. Second, node *X* becomes floating in certain cases and its value may drift causing extra dc power.

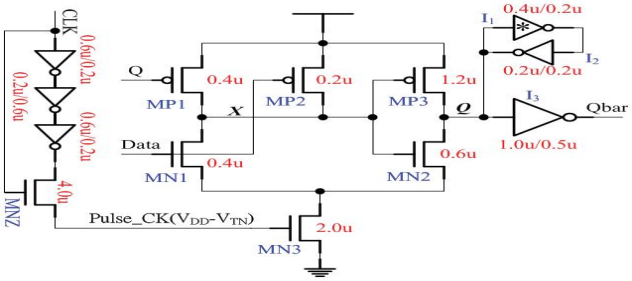

Fig.2.1(d) MHLFF

2.1.(e) TSPCFF: True-single-phase-clock Flip Flop

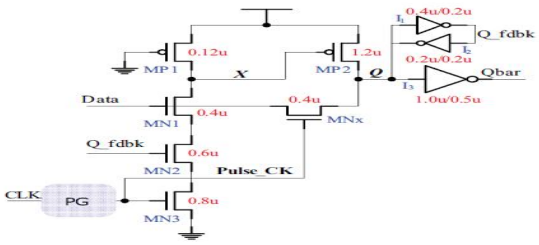

Fig.2.1(e)TSPCFF

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A weak pull-up pMOS transistor MP1 with gate connected to the ground is used in the first stage of the TSPC latch. This gives rise to a pseudo-nMOS logic style design, and the charge keeper circuit for the internal node *X* can be saved.In addition to the circuit simplicity, this approach also reduces the load capacitance of node *X* . Second, a pass transistor MNx controlled by the pulse clock is included so that input data can drive node Q of the latch directly (the signal feed-through scheme).Along with the pull-up transistor MP2 at the second stage inverter of the TSPC latch, this extra passage facilitates auxiliary signal driving from the input source to node Q. The node level can thus be quickly pulled up to shorten the data transition delay. Third, the pull-down network of the second stage inverter is completely removed. Instead,the newly employed pass transistor MNx provides a discharging path. The role played by MNx is thus twofold, i.e., providing extra driving to node Q during 0 to 1 data transitions, and discharging node Q during "1" to "0" data transitions. Compared with the latch structure used in SCDFF design, the circuit savings of the proposed design include a charge keeper (two inverters), a pull-down network (two nMOS transistors), and a control inverter. The only extra component introduced is an nMOS pass transistor to support signal feedthrough. This scheme actually improves the "0" to "1" delay and thus reduces the disparity between the rise time and the fall time delays.

2.2 Proposed P-FF design: PTLFF: Pass Transistor Logic Flip Flop

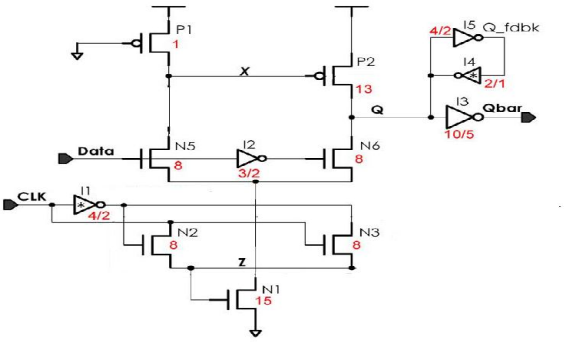

Fig.2.2 proposed P-FF design

The proposed design, as shown in Fig. 2.2, adopts two measures to overcome the problems associated with existing P-FF designs. The first one is reducing the number of nMOS transistors stacked in the discharging path. The second one is supporting a mechanism to conditionally enhance the pull down strength when input data is "1." Refer to Fig. 2.2, As opposed to the transistor stacking design in Fig.2.1(a),(b),(c),(d) and (e), this PFF design discharging path using PTL.Transistor N2, in conjunction with an additional transistor N3, forms a two-input pass transistor logic (PTL)-based AND gate to control the discharge of transistor N1. Since the two inputs to the AND logic are mostly complementary (except during the transition edges of the clock), the output node Z is kept at zero most of the time. When both input signals equal to "0" (during the falling edges of the clock),temporary floating at node Z is basically harmless. At the rising edges of the clock, both transistors N2 and N3 are turned on and collaborate to pass a weak logic high to node Z, which then turns on transistor N1 by a time span defined by the delay inverter I1. The switching power at nodeZ can be reduced due to a diminished voltage swing. Unlike the MHLLF design , where the discharge control signal is driven by a single transistor, parallel conduction of two nMOS transistors (N2 and N3) speeds up the operations of pulse generation.With this design measure, the number of stacked transistors along the discharging path is reduced and the sizes of transistors N1-N3 can be reduced also.

In this design, the longest discharging path is formed when input data is "1" while the Qbar output is "1." It steps in when node X is discharged V_{TP} below the V_{DD}. This provides additional boost to node Z (from V_{DD}-V_{TH} to V_{DD}). The generated pulse is taller, which enhances the pull-down strength of transistor N1.

After the rising edge of the clock, the delay inverter I1 drives node Z back to zero through transistor N3 to shut down the discharging path.. This means to create a pulse with sufficient width for correct data capturing, a bulky delay inverter design, which constitutes most of the power consumption in pulse generation logic, is no longer needed. It should be noted that this conditional pulse enhancement technique takes effects only when the FF output Q is subject to a data change from 0 to 1. The leads to a better power performance than those schemes using an indiscriminate pulse width enhancement approach. Another benefit of this conditional pulse enhancement scheme is the reduction in leakage power due to shrunken transistors in the critical discharging path and in the delay inverter.

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III.SCHEMATIC CIRCUITS AND LAYOUTS

3.1.Conventional P-FF designs:

3.1(a)EP-DCO: explicit -Data closed to output Flip-Flop

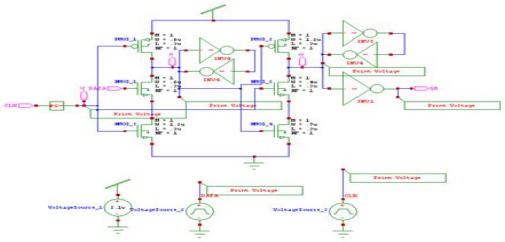

Fig. 3(a) – EP-DCO Schematic using In Tanner Tool

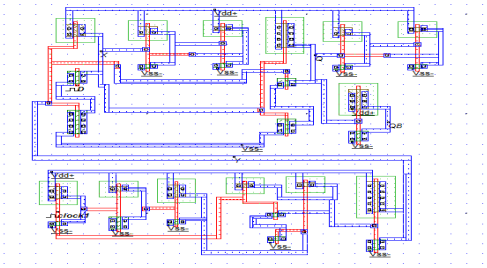

Fig .3(b) EP-DCO layout using in Microwind tool

3.1(b)SCDFF: Static- conditional discharged Flip-Flop

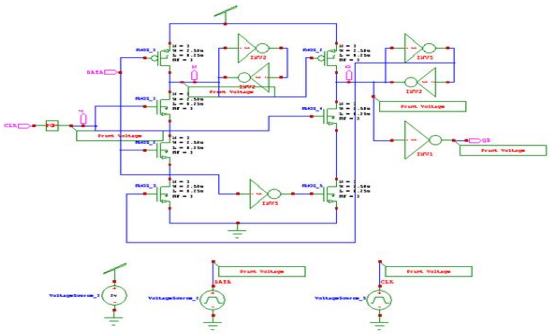

Fig. 3(c) – SCDFF Schematic using In Tanner Tool.

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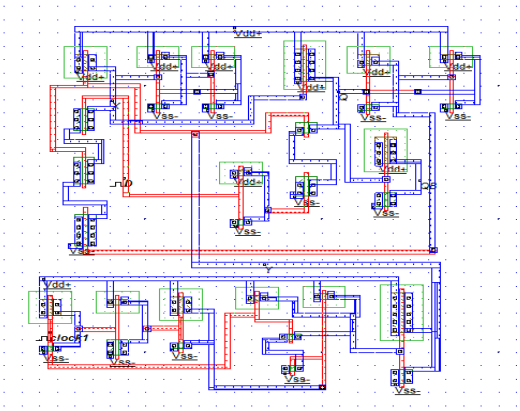

Fig .3(d) SCDFF layout using in Microwind tool

3.1(c)CDFF: conditional discharged Flip- Flop

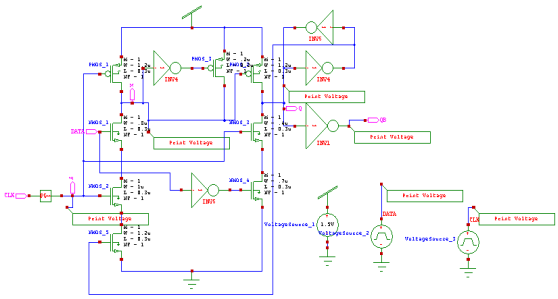

Fig. 3(e) CDFF Schematic using In Tanner Tool.

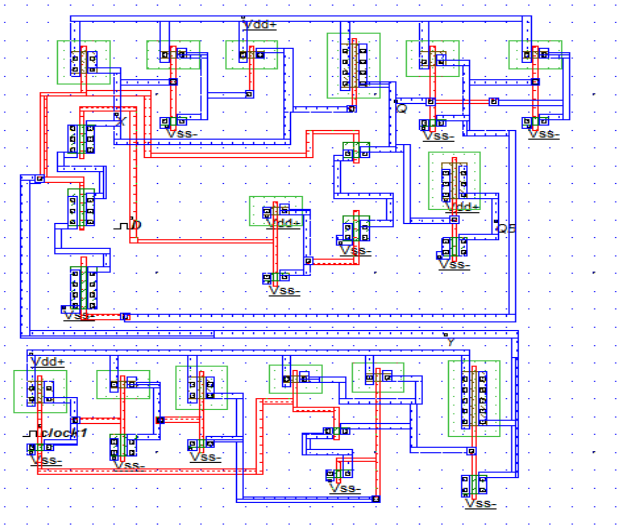

Fig .3(f) CDFF layout using in Microwind tool

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3.1(d).MHLFF: Modified hybrid latch flip flop

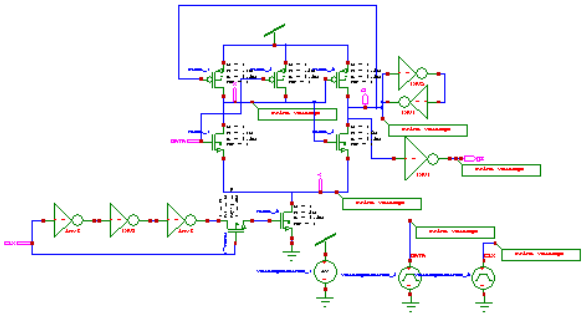

Fig. 3(g) MHLFF Schematic using In Tanner Tool.

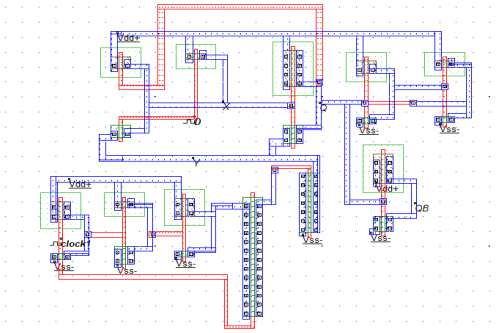

Fig 3(h) MHLFF layout using in Microwind tool

3.1(e).TSPCFF: True-single-phase-clock Flip Flop.

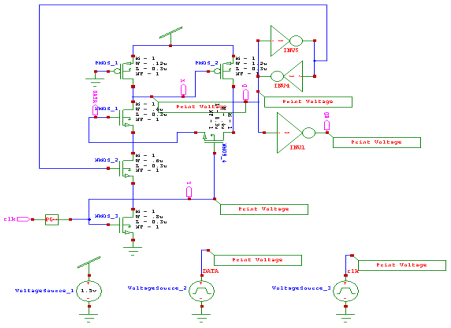

Fig. 3(i) TSPCFF Schematic using In Tanner Tool.

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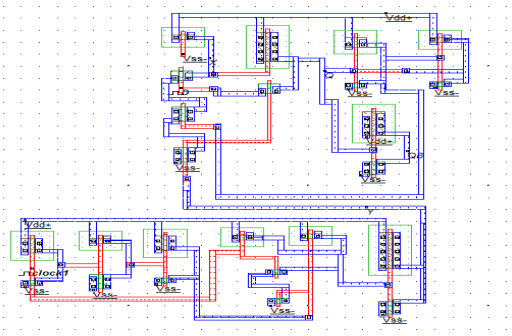

Fig 3(j) TSPCFF layout using in Microwind tool

3.2. Proposed:

3.2.(a)PTLFF: Pass Transistor Logic Flip Flop

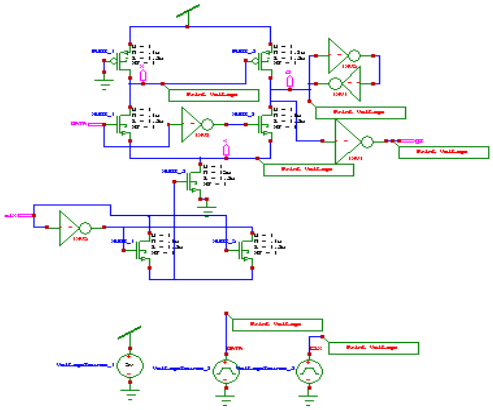

Fig .3.2(a) PTLFF Schematic using In Tanner Tool.

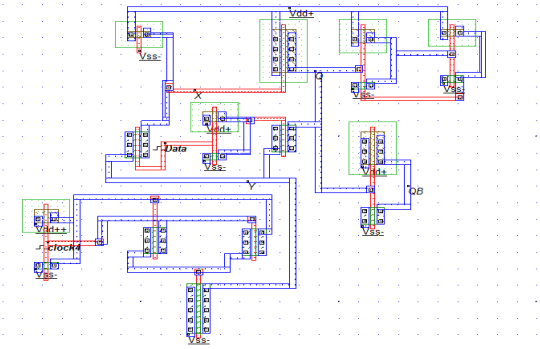

Fig 3.2(b) PTLFF layout using in Microwind tool

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IV.RESULTS

SIMULATION OUTPUTS:

The simulation results of above designs are shown below in the Fig. 4(a) to Fig. 4(l). A simulation window appears with inputs and output. The power consumption is also shown on the right bottom portion of the window. If you are unable to meet the specifications of the circuit change the transistor sizes. Generate the layout again and run the simulations till you achieve your target delays. Depending on the input sequences assigned at the input the output is observed in the simulation.

To demonstrate post layout simulations on various P-FF designs were conducted to obtain their performance figures. These designs include the 6 P-FF designs shown in Fig. 3.1(b)EP-DCO, Fig. 3.1(d) SCDFF, Fig. 3.1(f)CDFF,3.1(h)MHLFF,3.2(b) to the correctness of data capturing as well as the power consumption. All designs are further optimized subject to the tradeoffs between power and D-to-Q delay.

EP-DCO:

Figure 4(a)-Simulation output EP-DCO using Tanner Tool.

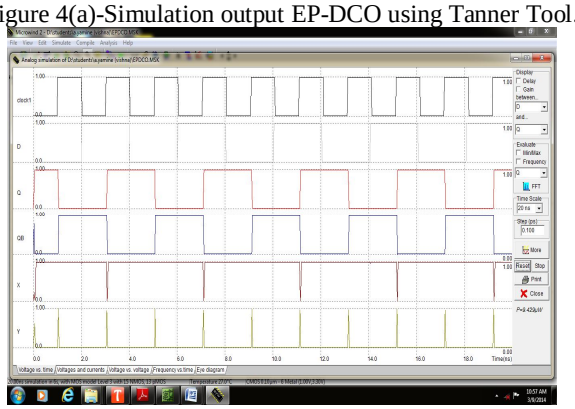

Figure 4(b) Power consumed by EP-DCO using in Microwind tool in 90nm.

SCDFF:

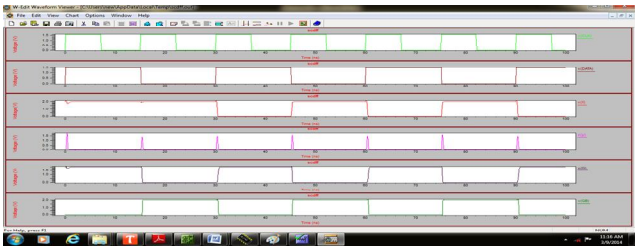

Figure 4(c)Simulation output SCDFF using Tanner Tool.

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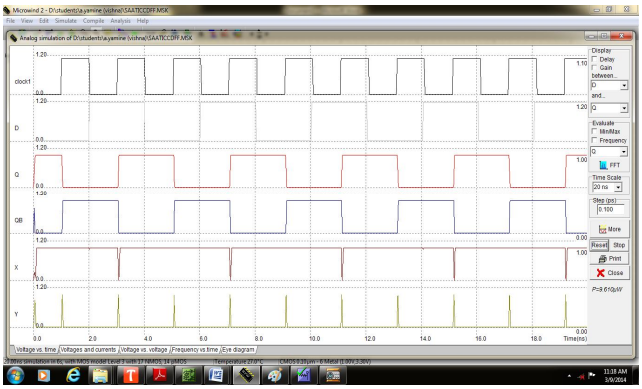

Figure 4 (d) Power consumed by SCDFF using in Microwind tool in 90nm.

CDFF:

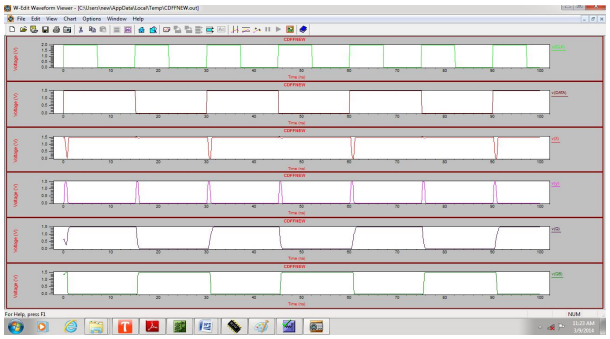

Figure 4(e)-Simulation output CDFF using Tanner Tool.

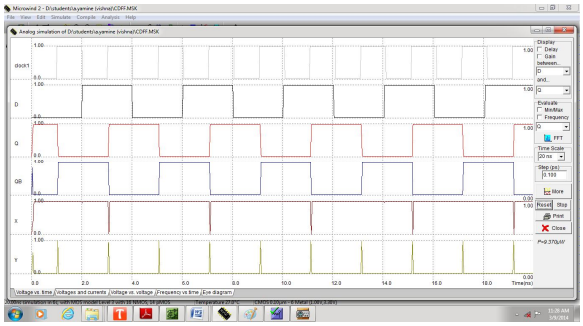

Figure 4(f)-Power consumed by CDFF using in Microwind tool in 90nm.

MHLFF:

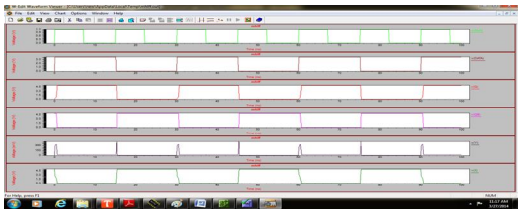

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Figure 4(g)-Simulation output MHLFF using Tanner Tool.

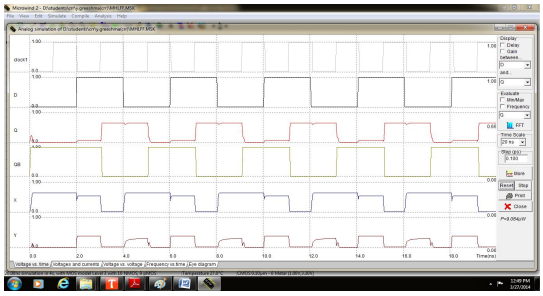

Figure 4 (h)Power consumed by MHLFF using in Microwind tool in 90nm.

TSPCFF:

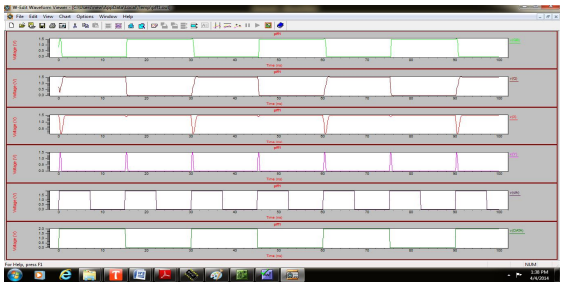

Figure 4(i)Simulation outputTSPCFF using Tanner Tool.

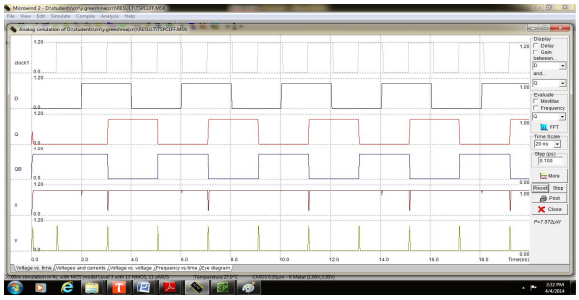

Figure 4 (j)Power consumed by TSPCFF using in Microwind tool in 90nm.

PTLFF:

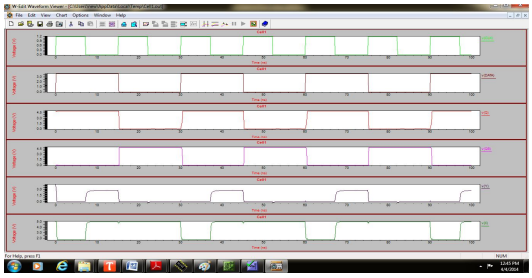

Figure 4(k)Simulation output PTLFF using Tanner Tool.

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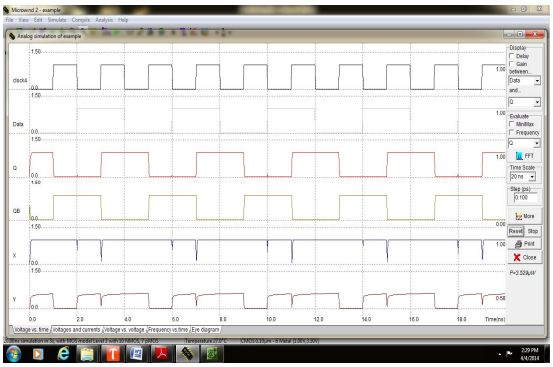

Figure 4 (l)-Power consumed by PTLFF using in Microwind tool in 90nm.

Table 1. Comparison of various P-FF designs

P-FF (Pulse Trigger Flip Flop)	EP-DCO	SCDFF	CDFF	MHLFF	TSPCFF	Proposed PTLFF
No. of transistors	**28**	**31**	**30**	**19**	**24**	**17**
Area μm^2 UMC CMOS-90nm	**159.3**	**174**	**173.4**	**128.4**	**163.2**	**117.6**
Avg. Power (µW) Using UMC CMOS-90nm Technology.(µW).	**9.42**	**9.61**	**9.37**	**9.27**	**7.57**	**3.57**
Delay(ps)	**1530**	**711.69**	**853.8**	**615**	**520**	**508**

V.CONCLUSION

In this Paper, the various Flip flop design like, EP-DCO, MHLLF, SCDFF, CDFF,TSPC based P-FF &Proposed NEW P-FF are discussed. The Pass Transistor logic Flip Flop (PTLFF) design by employing two new design measures. The first one successfully reduces the number of transistors stacked along the discharging path by incorporating a PTL-based AND logic. The second one supports conditional enhancement to the height and width of the discharging pulse so that the size of the transistors in the pulse generation circuit can be kept minimum. These were been also designed in Tanner Tool& Micro wind Tool those result waveforms are also discussed. The comparison table also added to verify the designed methods using UMC CMOS 90-nm technology. With these all results Proposed PTLFF performed speed or power better than EP-DCO, MHLLF, SCDFF, CDFF and TSPCFF designs.

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