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Power optimization of EPC Class-1 Gen-RFID Sensory Tags

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ABSTRACT: RFID is a technology that uses radio waves to transfer data from an electronic tag, called RFID tag or label, attached to an object, through a reader for the purpose of identifying and tracking objects. In addition sensory tag adds the additional external sensed data details in to the tag memory. Power consumption is one of the major issues in the RFID system. In passive tag, entire power for operation is drawn from the RFID reader as radio waves hence high power consumption of RFID tag reduce the reading range of the RFID system and hence performance degrades. Processor is the major component that consumes power. In existing system entire processor block is powered at all the time but it is not necessary. The proposed work targets on the digital section of the RFID tag processor based on EPC Class-1 Gen-2 protocol. Clock-Gating and Clock-management are the two hard-ware-level techniques for power saving in digital section. These techniques are employed via hardware circuit in the gen-2 processor to enable and disable the necessary operating blocks in the processor which minimize the power consumption of the processor and hence the RFID tag.

KEYWORDS*:* Clock Gating, Clock Management, Electronic product code (EPC) class-1 Generation-2 (Gen-2) protocol, ISO-18000-6C, Low power design, RFID, Sensory Tag.

I. INTRODUCTION

Radio frequency identification (RFID) is a generic term that is used to describe a system that transmits the identity (in the form of a unique serial number) of an object or person wirelessly, using radio waves [1,2]. It's grouped under the broad category of automatic identification technologies. In addition, RFID is increasingly used with biometric technologies for security. Unlike ubiquitous UPC barcode technology, RFID technology does not require contact or line of sight for communication. RFID data can be read through the human body, clothing and non-metallic materials. RFID communications use a master-slave configuration formed by a reader and a set of tags [3,4]. Each tag has a unique identification number stored in a non-volatile memory, which is addressed by the reader to establish the communication link. Upon the commands sent by the reader, the selected tag delivers the requested information. In the so-called sensory tags, such information might not only consist on identification data but also contain environmental readouts (e.g., temperature, pressure, optical or chemical variables) obtained from an embedded sensor interface. Tags are classified into active or passive depending on how energy is supplied to the device. Passive tags have no internal power source available, as in the case of active transponders, but they are remotely biased by the reader by means of an on-chip RF-to-DC conversion stage [5]. Because of the scarce supplying conditions, power consumption minimization is a priority for passive tags. This paper focuses on the design of the digital section a passive UHF RFID sensory tag implementing clock gating and clock management techniques. The EPC Class-l Generation-2 (Gen2) protocol which is briefly reviewed in Section II. The architecture of the baseband processor under Gen-2 specification are presented in section III. Next, section IV shows the simulation and experimental results. Finally, section V concludes the paper.

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II. EPC CLASS-1 GENERATION-2 UHF RFID PROTOCOL

This specification [6] defines the physical and logical requirements for a passive-backscatter, Interrogator-talks-first (ITF), radio-frequency identification (RFID) system operating in the 860 MHz – 960 MHz frequency range. The system comprises Interrogators, also known as Readers, and Tags, also known as Labels. An Interrogator transmits information to a Tag by modulating an RF signal in the 860 MHz – 960 MHz frequency range.

The Tag receives both information and operating energy from this RF signal. Tags are passive, meaning that they receive all of their operating energy from the Interrogator's

RF waveform. An Interrogator receives information from a Tag by transmitting a continuous-wave (CW) RF signal to the Tag, the Tag responds by modulating the reflection coefficient of its antenna, thereby backscattering an information signal to the Interrogator.

The system is ITF, meaning that a Tag modulates its antenna reflection coefficient with an information signal only after being directed to do so by an Interrogator. Interrogators and Tags are not required to talk simultaneously rather, communications are half-duplex, meaning that Interrogators talk and Tags listen, or vice versa.

A. Physical Layer Specification

The Physical layer specification for the RFID communications are explained in the following tables (table1 and table2) with respect to interrogator to tag and vice versa.

Operating frequency	890-960 MHZ
Modulation	DSB-ASK,SSB-ASK, or PP-ASK
Modulation depth	90% normal
Duty cycle	48% - 82.3%
Data coding	PIE
Bit rate	26.7kbps to 128 kbps
Bit transmission order	MSB is transmitted first

Table1: Interrogator to Tag

Operating frequency	860-960 MHZ
Modulation	ASK and/or PSK modulation(selected by tag)
Sub carrier frequency	40 KHZ to 60 KHZ
Sub carrier modulation	Miller, at the data rate
Bit transfer order	MSB is transmitted first

Table2: Tag to Interrogator

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B. Managing Tag Population

Interrogators manage Tag populations using the three basic operations. Each of these operations comprises one or more commands.

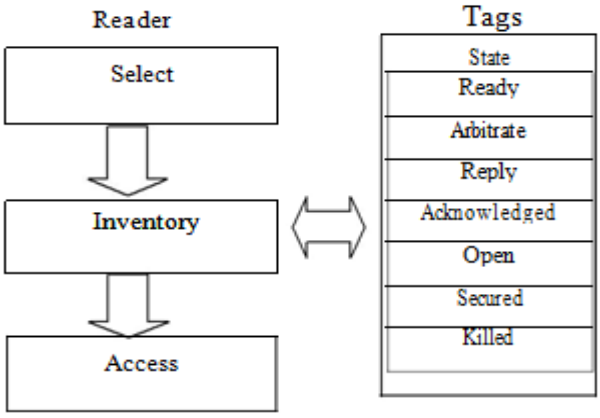

Fig 1: Managing Tag Population

The operations are defined as follows:

a) Select: The process by which an Interrogator selects a Tag population for inventory and access. Interrogators may use one or more *Select* commands to select a particular Tag population prior to inventory.

b) Inventory: The process by which an Interrogator identifies Tags. An Interrogator begins an inventory round by transmitting a *Query* command in one of four sessions. One or more tags may reply. The Interrogator detects a single Tag reply and requests the PC word, optional XPC word or words, EPC, and CRC-16 from the Tag. An inventory round operates in one and only one session at a time.

c) Access: The process by which an Interrogator transacts with (reads from or writes to) individual Tags. An individual Tag must be uniquely identified prior to access. Access comprises multiple commands, some of which employ one-time-pad based cover-coding of the R=>T link.

In Gen-2 protocol there are twelve possible commands (see table3) from RFID reader according to the command tag will response by changing tag's state according to the command.

Category	Command	Cmd_id
Query	Query rep	0001
	Query	0011
	Query adjust	0100
Inventory	Ack	0010
	Nak	0101
Select	Select	0110
Access	Request RN	0111
	Read	1000
	Write	1001
	Kill	1010
	Lock	1011
	Access	1100

Table3:Gen-2 reader commands

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III. GEN - 2 BASEBAND PROCESSOR

A. Power Consumption Methodologies

Clock Gating and Clock management:
Clock gating is the power saving strategy for the digital circuits by activating minimum number of blocks [7]. In RFID tag digital section, if the system is not completely interpreted a received command, there is no need to activate those blocks required for backward link communications. It is done by enabling blocks when necessary and disabling blocks when they are dispensable [8]. This can be simply done by and-combining the clock or trigger pulses which activate the block with an enable flag and corresponding command received from the reader.
In Clock managing technique, depending on the RFID tag processor state, only Pie_decoder block, FSM_core block, FSM_Tx and Tx block need to run at full speed. The rest of the blocks can be clocked at a fraction of the master frequency to save power. The lower limit of the dedicated clock frequencies is determined by the time interval between two rising edge of the demodulated input signal [14].

B. Processor Architecture

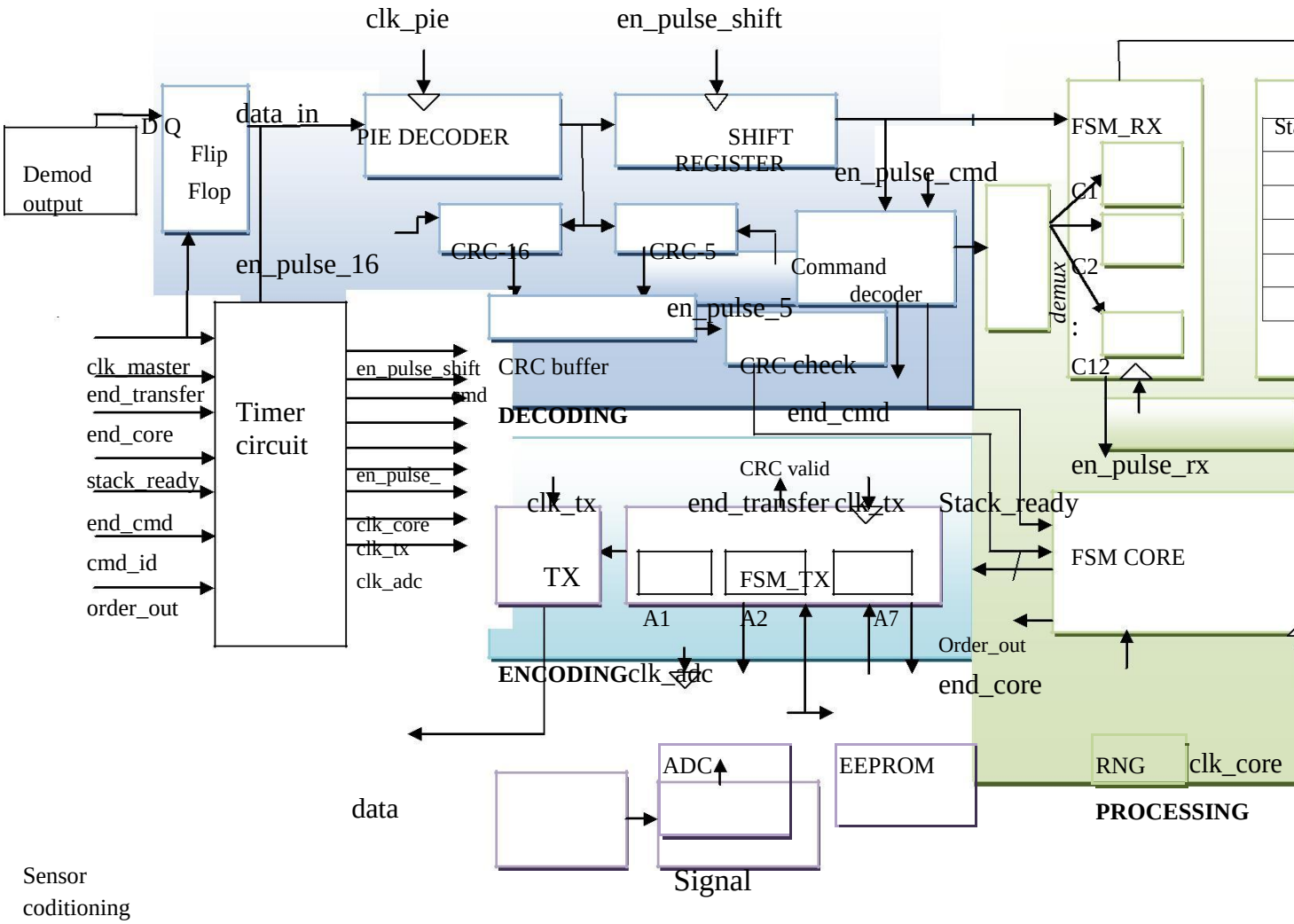

Fig 2: Baseband processor for Gen-2 specification

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In Fig 2 Baseband processor for Gen-2 specification implementing Clock managing technique, depending on the RFID tag processor state, only Pie_decoder block, FSM_core block, FSM_Tx and Tx block need to run at full speed. The rest of the blocks can be clocked at a fraction of the master frequency to save power [9-10]. The lower limit of the dedicated clock frequencies is determined by the time interval between two rising edge of the demodulated input signal. In the decoding section, a edge triggered flip-flop is used to synchronize the demodulated signal coming from the analog front-end of the RFID, demodulated output, to the master clock signal. Reader to tag communications use Pulse-Interval Encoding (PIE) format and, therefore, the resulting digitized forward link, data_in, must be converted into binary format. This is accomplished in the PIE Decoder block whose output is sequentially stored in a 16-bit Shift Register block at a rate defined by the trigger pulses, en_pulse_shift [12]. Next, the Command Decoder block evaluates the data stored in the register to identify which instruction has been sent by the reader. Operation of the Command Decoder block is controlled by the trigger signal enpulse_cmd, a delayed version of en_pulse_shift, to allow a more uniform distribution of current consumption over time. When the command received is identified, the Command Decoder sets on the end_cmd flag and codifies the instruction in a 4-bit vector, cmdID. Besides filling Shift Register, the output of the PIE Decoder block is also transferred to a cyclic redundancy check (CRC) unit for transmission error detection. The EPC Gen 2 protocol uses two types of CRCs they are CRC-5 and CRC-16 [13]. The former is used by Query commands, whereas the latter is used by Select and Access commands. Inventory commands are unprotected. Once the Command Decoder identifies the type of instruction that it is being received, it disables the useless CRC block(s) for power saving. The

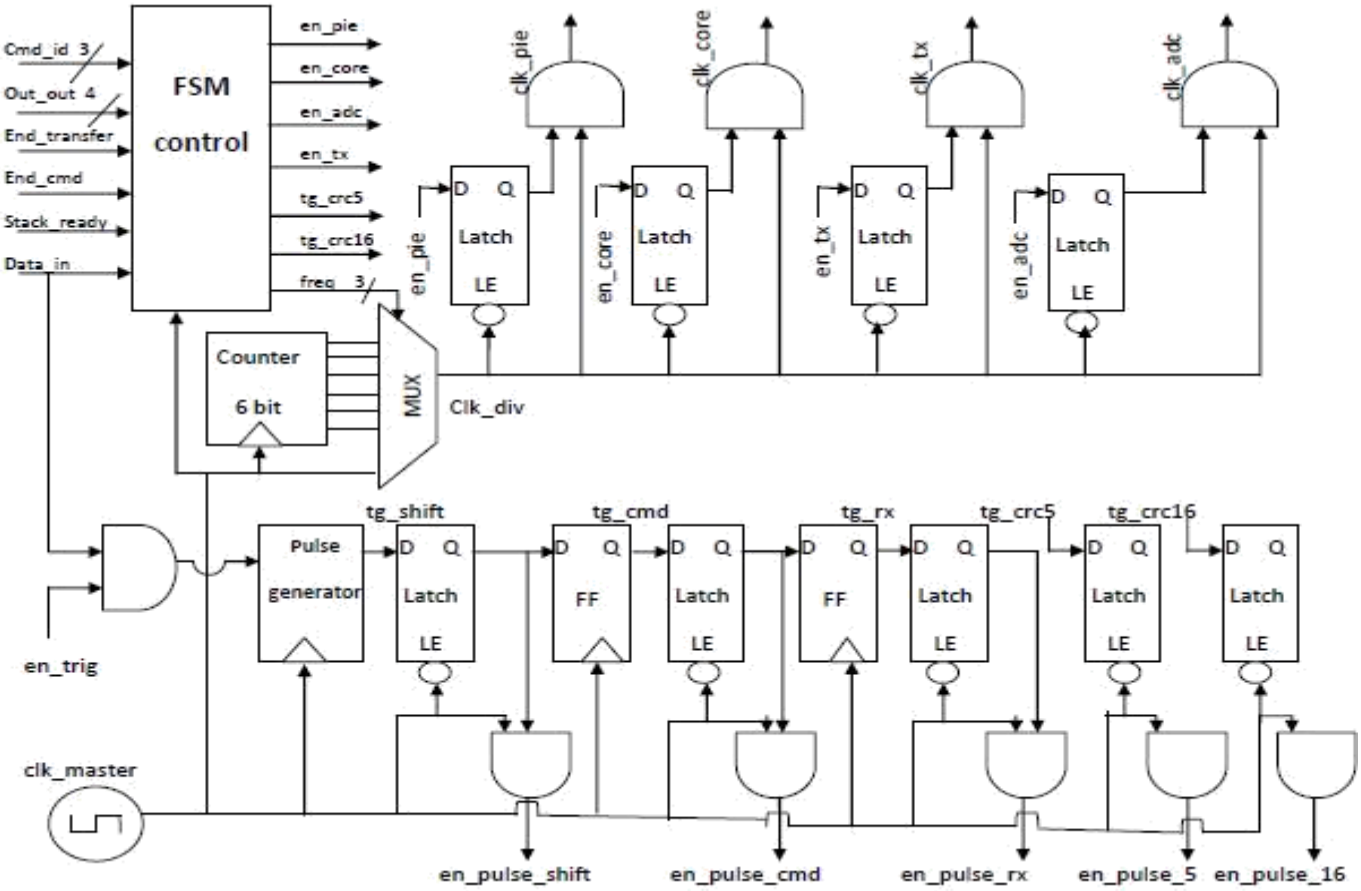

Fig 3: Timer circuit for power control in Baseband processing

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Vol. 3, Issue 12, December 2014

results of the CRC computations are stored in buffers and these values are used by a Check CRC block to assess their validity. The CRC blocks, CRC-5 or CRC-16 are enabled each rising edge of data _in, employing pulses enpulse_5 and enyulse_I6, respectively. Once the command is identified, the Command Decoder passes cmd ID to the FSM Rx block, inside the processing section. This block is controlled by the trigger pulses en_pulse_rx, a delayed version of signal enpulse_cmd, and it is formed by a set of Finite State Machines (FSM), one per Gen2 command. Only that FSM addressed by the Command decoder is active the others are disabled [11]. The active FSM sequentially stores the command parameters in the registers of the Stack block. Only that register which is being addressed by the FSM Rx block is active, the others remain off. The FSM Rx block notifies the Timing Unit by means of the stack_ready flag when the reception is finished and then the trigger pulses of the CRC modules and the PIE Decoder block are disabled.
The FSM Core block decides the tag's state, performs the required state transitions, read the parameters stored in the Stack by the FSM Rx, and triggers the FSM Tx block according to the command that has been received. When operations at FSM Core are concluded a non-zero 5-bit vector, order_out, is transmitted to the Processing FSM Tx block and FSM Core is disabled by the Timing Unit. At the encoding section, the FSM Tx block performs the actions requested by the reader such as write/read the EEPROM, gather parameters or information. data format to be transmitted or the operation to be executed by the Encoding section of the baseband-processor. There is one FSM for each possible action type, and, as before, only one FSM is enabled at a time. The former is used to adapt the sensory information to the signal range of the ADC. The ADC is clocked by the Timing Unit block through the signal clk_adc, and its operation is controlled by the FSM Tx block.

Timing Unit:
Fig3 is the additional circuit which employs clock gating and clock management techniques for power saving. It is responsible for generating clock pulse and trigger pulses for enabling and disabling blocks[9].

IV. SIMULATIONS AND EXPERIMENTAL RESULTS

The clock gating and clock management techniques for power saving is realized via timing circuit. Timing circuit corresponding to the working of EPC class-1 Gen-2 baseband processor was designed and the same is verified using Xilinx Spartan 3E. Clk1 is externally triggered to see the state changes in the same simulation which is shown in the figure which corresponds to the enable flag as per the working
processor. As mentioned in the timer circuit as shown in fig.3 State changes occur at every trigger pulse which may be the output of certain blocks of a processor.

In the initial state dedicated clock pulse clk_pie is on and all the delay pulse en_pulse_shift, en_pulse_cmd, en_pulse_rx and pulse for CRC block i.e., en_pulse_5, en_pulse_16 is on. When end_cmd flag is on which is generated when the completion of command decoder block when the command is decoded then the four bit command id is send to the timer circuit. Once the command is identified it disables the useless CRC block which is realized by the state change. When the stack_ready flag is on which is generated when the completion of FSM_RX block. In this block Gen-2 protocol addressed by the protocol parameter is active one per each command. It disables the enabling pulse of CRC modules and clk_pie and enables the clk_core which is achieved by state change. In the next state clk_core is disabled and two pulses are enabled i.e., FSM_Tx and ADC for encoding. The figure5, 6, 7 shows the simulation result of the timer circuit in which Query rep, Ack command, lock command is analyzed. Clk1 is externally triggered to show the state changes at the positive edge of the clock. For entire operation for state change is realized in the single window all the trigger pulse is made on and corresponding working of timer circuit with respect to state change is realized. The schematic diagram for timer circuit is shown in the figure4.

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Fig 4:Schematic diagram of the timing circuit

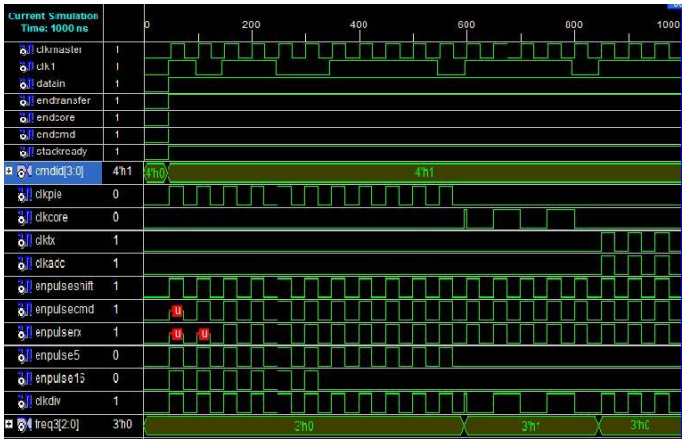

Fig 5: Result for Query Rep command

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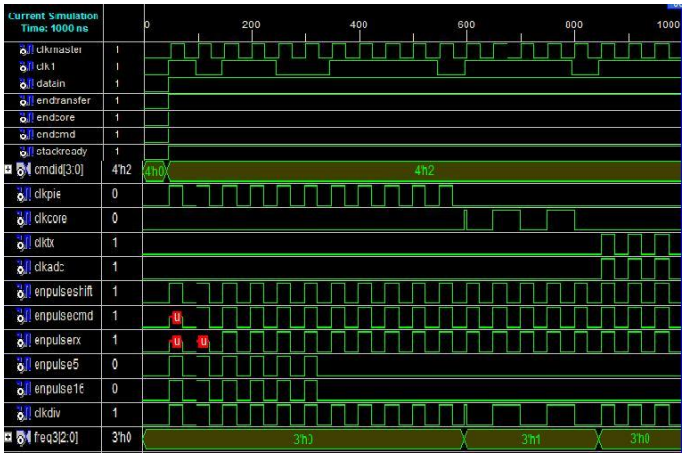

Fig 6: Result for ACK command

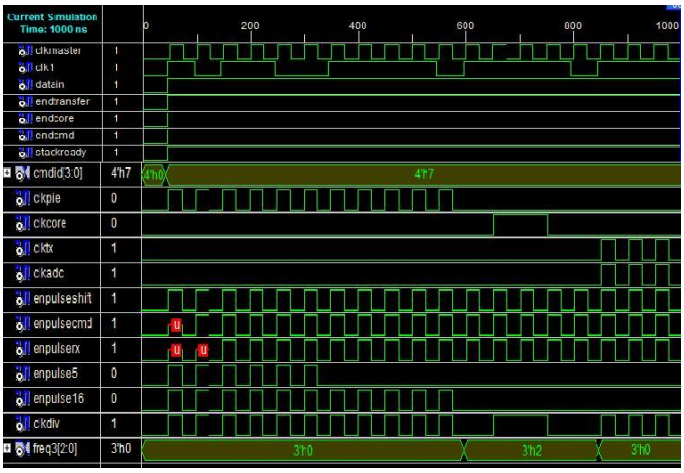

Fig 7: Result for Req RN command

V. CONCLUSIONS

In this work, clock gating and clock management is realized via timing circuit corresponds to the EPC class-1 Gen-2 tag baseband processor and the working is realized using simulation and the design is validated in Xilinx Spartan 3E FPGA.

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