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EBG Structure with Mendered Bridge For

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ABSTRAT*:* A meandered EBG structure operating over a large bandwidth has been proposed for UWB applications. The structure includes a meandered bridge which increases the inductance effect, which in turn increases the effective bandwidth of the EBG structure.The proposed EBG structure helps to suppress noise in integrated circuits over Ultra Wide Band. The EBG structure operates over 46 Mhz to 10 Ghz. The structure has been designed using CST 2012.

KEYWORDS-EBG(Electromagneticbandgap structure,UWB(Ultra wideband),GBN(Ground Bounce Noise)

I. INTRODUCTION

In recent years current packaging technologies, data, video, voice sensing and other function modules such as digital, analog, RF, memory devices, sensors, etc. are required to be integrated into one pack known as 'system on package'. It is Used in communication systems like phones.

The forthcoming generation of processors will have several parts of chipsets integrated in the same package thus resulting in complex integrated circuits.**G**round Bounce Noise[1] (GBN) on the power/ground planes is becoming one of the major concerns for the high-speed digital computer systems due to fast edge rates, using high clock frequencies, and low voltage levels. Because of the parallel-plate waveguide structure between power and ground planes in the high-speed packages, the resonance modes of the parallel-plate waveguide can be excited by the GBN. The resonance noise propagating between the power and ground planes not only causes signal integrity (SI) problems for the circuits , but also results in significant radiation or electromagnetic interference (EMI) issues.[2] Simultaneous switching noise (SSN)[3], also known as ground bounce noise[1], or delta-I noise, on the power/ground buses have become one of the major concerns during the design because of high-speed digital combinations systems with even faster edge rates, lower voltage levels, and higher integrations.In the current scenario, PCB design level it's major bottleneck for designers to mitigate noise in power plane resonance while suppressing the propagation of waves generated noise by the switching devices .Many Methods introduced in past works, in order to eliminate ground bounce noise, all try to reduce the resonance effects of the cavity-like structure. The most widely used and effective of them include the use of decoupling capacitors[4] , and capacitors , the use of dissipative and lossy components along the PCB and at its edges , dividing power planes in power islands , and via stitching[5]

The use of decoupling capacitors is the most wide spread method and it consists of placing large capacitors around the sources of noise to disrupt high-frequency fluctuations on the power planes by creating a low-impedance path between the planes at these frequency. Other methods try to overcome this frequency limitation, in one way or another. Embedded capacitors and capacitances try to minimize the length of the problematic leads. Power islanding is also widely used, but its applicability is limited to applications in which isolation is the goal such that the source of noise and the susceptible components are kept on different power islands.

EBG is one of the most promising solution to suppressed noise in mixed signal circuits. Earlier days Mushroom structure[6] are first proposed. this structure is specially designed via is inserted between power and ground planes, which make the fabrication cost is more effective. Later many planar structure is designed because of cost effective and fabrications cost is less. EBG planar structures proposed over the past few years have inherent features that make them important in EMI applications in mixed Signal Circuits. It's Create High Impedance surface(HIS).This is primarily due to the fact that EBG structures suppress the propagation of surface

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waves over a specific frequency band that directly depends on the dimensions and type of the constitutive elements within the EBG structures

This paper proposed a novel structure to widen the band gap of EBG by introducing Meandered bridge instead of L-shaped bridges proposed in [7] and compared the results of existing uniplanar compact EBG structure and modified structure by indroducing meandered bridge will reduce the lower edge of the bandgap to attain wide isolation bandwidth of the proposed structure

Table 1. Valid switching states of the proposed voltage source inverter output voltage

St	S_{a1}	S_{a2}	S_b	S_{b2}	V_{an}	V_{bn}	V_{ab}
1	1	1	0	0	V_{dc}	0	V_{dc}
2	1	0	0	0	$V_{dc}/2$	0	$V_{dc}/2$
3	0	1	0	0	$V_{dc}/2$	0	$V_{dc}/2$
4	0	0	0	0	0	0	0
5	1	1	1	1	V_{dc}	V_{dc}	0
6	1	0	1	1	$V_{dc}/2$	V_{dc}	$-V_{dc}/2$
7	0	1	1	1	$V_{dc}/2$	V_{dc}	$-V_{dc}/2$
8	0	0	1	1	0	V_{dc}	$-V_{dc}$

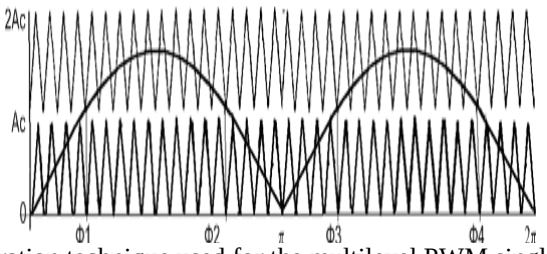

Fig.2 PWM generation technique used for the multilevel PWM single phase inverter.

The parameters of the modulation process are shown in Fig.2 and defined as following:

1) The modulation index is defined as:

$$\mathrm{Ma} = \frac{\mathrm{Am}}{2\mathrm{Ac}}$$

Where Am is peak value of sinusoidal wave and Ac is the peak is the carrier peak-peak value.

2) The frequency modulation index:

$$\mathrm{Mf} = \frac{fc}{fm}$$

Where the frequency of the carrier is wave and is the frequency of the sinusoidal wave.

3) The angle of displacement existing between the sinusoidal wave and the first positive carrier wave can be defined as following:

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$$Am.Sin(\phi 1) = Ac$$

$$\phi 1 = Sin^{-1}\left(\frac{Ac}{Am}\right)$$

$$\phi 2 = \pi - \phi 1$$

$$\phi 3 = \pi + \phi 1$$

$$\phi 4 = 2\pi - \phi 1$$

II. PWM GENERATION USING XILINX FPGA

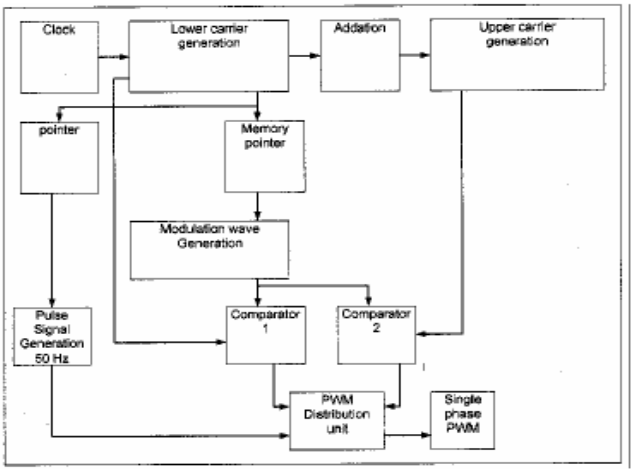

Fig.3 The block diagram of single phase PWM generator in XILINX FPGA

The upper and lower carrier waves (1800 Hz) are compared with the sinusoidal wave (50 Hz). In same time a pulse signal has frequency of (50 Hz) is generated and inverted to get its inverse pulse signal [8], [12].

There are only three control signals S6, S5 and S2 will be needed to derive, another three S3, S1, and S4 are simply generated in method of the logical inverse of S6, S5, and S2 respectively as shown in fig.4.

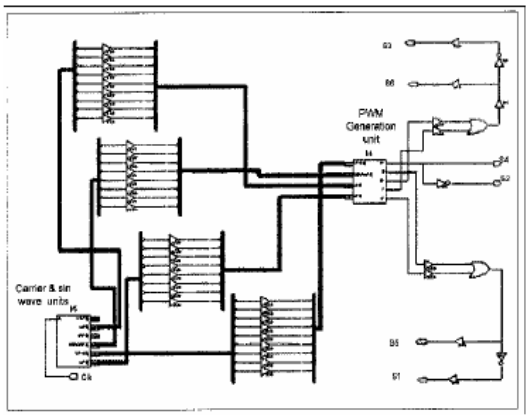

Fig.4 Single phase PWM scheme generator in XILINX FPGA

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3.1 Sinusoidal Wave Generation

The schematic diagram of the sine wave consists of a memory Pointer unit and schematic block includes a VHDL program for sine wave data as shown in Fig.3. The VHDL program includes 19 sine wave data calculated at every 5° degrees, these data cover quarter cycle of sine wave 90° degrees [6-7].
As the modulation index depends on the modulation wave amplitude, the sine wave data can be changed to achieve the required modulation index and thus the required output voltage [13-15].

3.2 Carrier Wave Generation

An 8-bit up-down counter is clocked at 918 KHz to produce 1800Hz carrier frequency and VHDL program includes a simple addition process is also written and converted into schematic block (addition unit) to generate two types of carrier (upper and lower) waves. The main clock frequency is determined by the following formula:

$$fclk = fc\left(2^{n} - 1\right)^{2}$$

Where is the main clock frequency, is the carrier (upper and lower) wave frequencies and n is the bit size of the up-down counter [9].

3.3 Pulse Signal 50Hz Generation

Two inverse pulse signals have same frequency (50Hz) need to be generated; their frequencies are similar to the sinusoidal wave and the output frequency [10]. Pointer unit consists of an 8 bit counter, some logic gates and VHDL program developed to store data in term of condition statements are the main structure of the pulse signal (50 Hz). These two signals have two functions, first as a switching signal for switches S4 and S2, second to involve with the resultant signals produced from comparators to generate the appropriate switching signals for switches S6, S3, S5 and S1 [11].

3.4 PWM Distribution Unit

This unit is used to distribute the PWM output pattern to the switches (S1, S2, S3, S4, S5 and S4). The distribution unit consists of a few logic gates (AND, OR, and NOT) deal with the three main signals produced from comparators and pulse signals 50 Hz generation unit to form the final PWM as shown in Fig.4.

III. SIMULATION RESULTS

The proposed capacitor clamped inverter is simulated using software package PSIM 6. The main components of proposed inverter are: C_1=2200µF, C_2=330µF, C_o=18uF, L_o=1mH and V_o, rms=110V/60Hz. The capacitor voltage V_2 equals 100V. The dc bus voltage is 200V. The triangular carrier frequency is 20 kHz. The figure 6.1 shows the simulated circuit diagram of the proposed inverter.

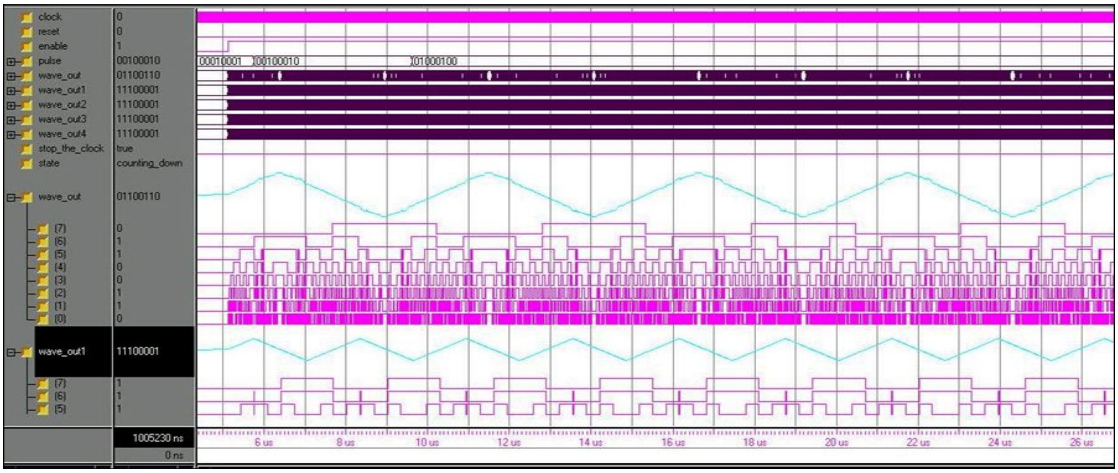

Fig.5 simulation result for triangular wave generation

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Fig.6 Simulation result for PWM generation.

VI. CONCLUSION

A single-phase voltage source inverter based on capacitor clamped configuration is proposed to provide a sinusoidal voltage to the output load. Three-level PWM scheme is used in the proposed inverter to reduce voltage harmonics on the ac side and reduce the voltage stress of the power semiconductors. The voltage stress of power devices is clamped to half the dc-link voltage.

Power switches in the one leg of inverter are operated at low switching frequency to generate two voltage levels on the voltage. Power switches in another leg of inverter are operated at high switching frequency to generate three voltage levels on the ac side voltage. Five voltage levels are achieved on the ac line output voltage.

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