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Smart-Receptionist: A Visitor Guidance Kit with Touch Screen Panel

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ABSTRACT: Our project, smart-receptionist is an automated reception system that takes the role of a receptionist and guides the incoming visitors by queuing them to their respective destinations or officials by showing route maps with the help of touch screen color panel and voice generation. It is also capable of recording the employee signature and does real time signature verification to maintain a digital attendance book.

KEYWORDS: ARM Cortex-M3, MIWI P2P Wireless Protocol, Four-wire touch screen.

I.INTRODUCTION

Designing and implementing a system for educational institutions, public banks and conference halls which can intelligently guide visitors to their destinations.In present human receptionists are guiding the visitors but they need to be trained, might look dull and must be provided wages. Human behaviors are unpredictable and they can go wrong in guiding a visitor with their punctuality and politeness. After this process, the kit will present a list of names (ex: principal, chairman, etc..,) whom the visitor want to meet or a list of places (medical dispensary, seminar room etc..,) where the visitor want to go. It asks the user to touch their choice. Once the user chooses the right option on the screen, the system will acknowledge with voice and it shows a route map of that building for the user to reach his destination spot or the place where the respective official would be normally available. Before this process more importantly it sends the visitor request through a wireless network to other slave units fixed near the official persons that will display the visitor name and his purpose. The official can communicate with the kit (call or hold) using the push buttons on his device and the kit will announce the visitor ID audibly and manage them in the reception. Pressing a button on the kit will cause the system to show the signature employee names along with the corresponding time. The kit is also able to handle multiple languages and the user will be guided in his language of choice.

BLOCK DIAGRAM

Our system consists of two main units. They are Reception Unit-Master & Visitor alert Unit-Slave

A. Working of Reception Unit-Master

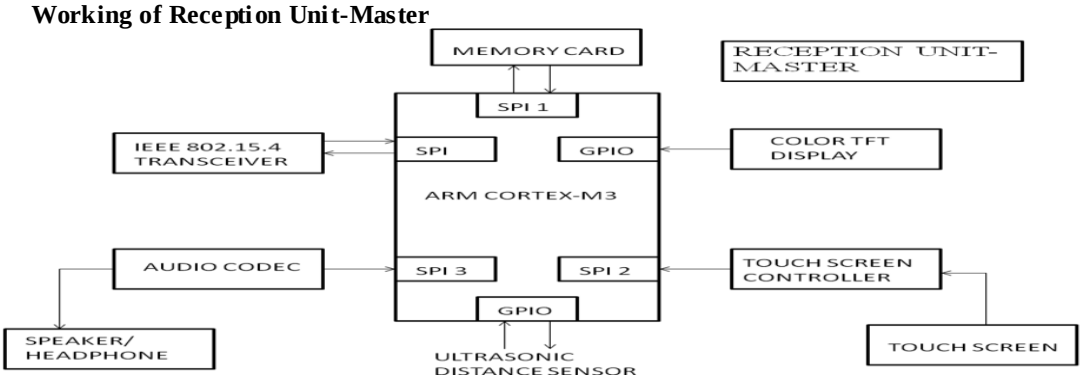

Fig 2.1 Block Diagram of Reception Unit

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The details of the employees are already configured and it is stored in the external memory provided by the SD memory card. The ultrasonic distance sensor senses when a person stands before it. The unit welcomes him and suggests using the Touch screen panel. It enquires him whether he is an employee or the visitor. If employee is opted then his arrival is being registered with arrival time. If visitor is opted then he is asked to select his destination. The respective destinations are guided with its route map on the touch screen. When he wants to meet the Principal then the information is passed to the visitor alert unit in the Principal's room to check whether the Principal wants to meet him or not.

B. Working of Visitor alert Unit-Slave

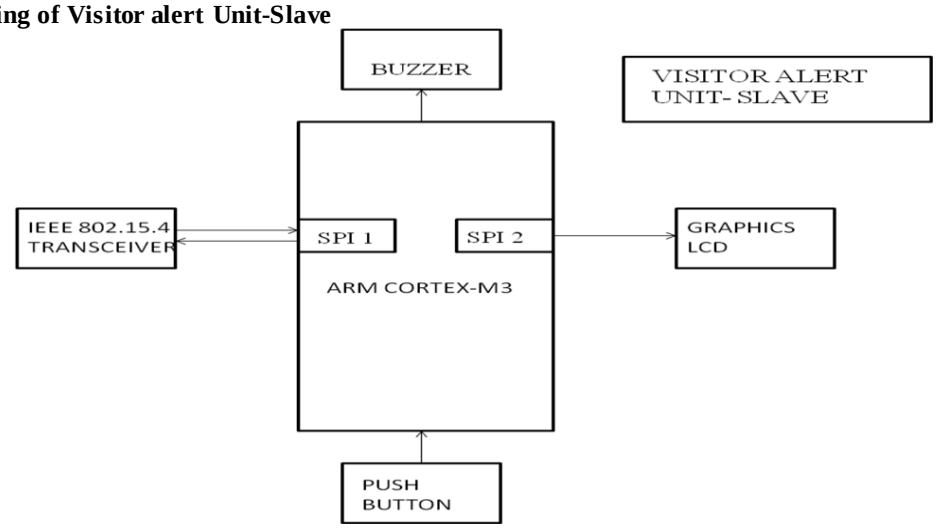

Fig 2.2 Block Diagram of Visitor Alert Unit

When the visitor unit in the Principal's room receives the information, the Buzzer sounds and alert the Principal that the person wants to meet him and his name is displayed in the LCD display. The person is made to be in queue or allowed to see the Principal immediately depending upon his choice of pressing the button. This information is send to the Reception Unit which either allots the ID number or displays the route to reach the Principal's room. If either of the buttons is not pressed by the Principal then the Reception Unit considers that the Principal is unavailable.

ARM Cortex-M3

Overview

The ARM Cortex™-M3 processor is the industry-leading 32-bit processor for highly deterministic real-time applications and has been specifically developed to enable partners to develop high-performance low-cost platforms for a broad range of devices including microcontrollers, automotive body systems, industrial control systems and wireless networking and sensors.

Features

a. Performance and Energy Efficiency

With high performance and low dynamic power consumption the Cortex-M3 processor delivers leading power efficiency 12.5 DMIPS/mW based on 90nmG. Coupled with integrated sleep modes and optional state retention capabilities the Cortex-M3 processor ensures there is no compromise for applications requiring low power and excellent performance.

b. Full featured

The processor executes Thumb®-2 instruction set for optimal performance and code size, including hardware division, single cycle multiply, and bit-field manipulation. The Cortex-M3 NVIC is highly configurable at design time to deliver up to 240 system interrupts with individual priorities, dynamic reprioritization and integrated system clock.

c. **Rich connectivity**

The combination of features and performance enables Cortex-M3 based devices to efficiently handle with multiple I/O channels and protocol standards.

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C LPC1313

General Description

The LPC1313 are ARM Cortex-M3 based microcontrollers for embedded applications featuring a high level of integration and low power consumption. The ARM Cortex-M3 is a next generation core that offers system enhancements such as enhanced debug features and a higher level of support block integration. The LPC1313 operate at CPU frequencies of up to 72 MHz. The ARM Cortex-M3 CPU incorporates a 3-stage pipeline and uses Harvard architecture with separate local instruction and data buses as well as a third bus for peripherals.

Features

1. ARM Cortex-M3 processor, running at frequencies of up to 72 MHz.
2. ARM Cortex-M3 built-in Nested Vectored Interrupt Controller (NVIC).
3. Selectable boot-up: UART or USB (USB on LPC134x only).
4. On-chip boot loader drivers for MSC and HID (LPC134x only).
5. Serial interfaces:

a. I2C-bus interface supporting full I2C-bus specification and Fast-mode plus with a data rate of 1 Mbit/s with multiple address recognition and monitor mode.

6. Other peripherals:

a. Up to 42 General Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors.

7. Integrated PMU (Power Management Unit) to minimize power consumption during Sleep, Deep-sleep, and Deep power-down modes.
8. Processor wake-up from Deep-sleep mode via a dedicated start logic using up to 40 of the functional pins.
9. Brownout detect with four separate thresholds for interrupt and one threshold for forced reset.
10. Power-On Reset (POR).
11. Unique device serial number for identification.

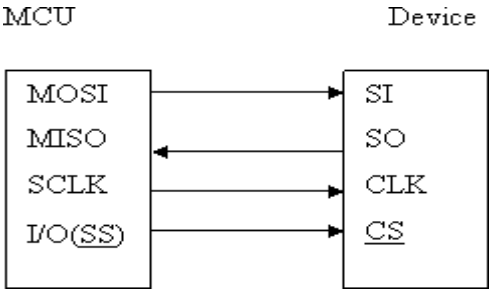
SERIAL PERIPHERAL INTERFACE

Overview

Serial Peripheral Interface is a simple interface which enables to communicate microcontroller and peripheral chips or intercommunicate between two or more microcontrollers. Serial Peripheral Interface bus sometimes called four wire interfaces may be used to interface such chips or devices like: LCD, sensors, memories, ADC, RTC. The range of usage is huge.

Description

SPI bus consists of four signal wires:



Data Transfer

Data transfer is organized by using Shift register in both: master and slave. While master shifts register value out through MOSI line then slave shifts data in to its shift register. If there is full duplex used, then send and receive is performed at the same time:

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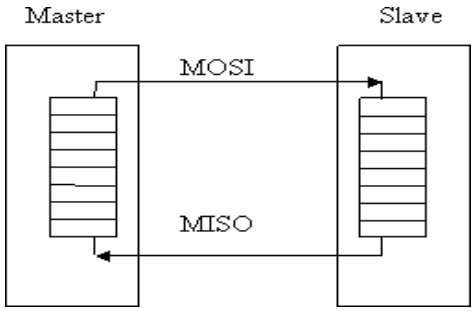

TOUCH SCREEN

Resistive touch screen:

A resistive touch screen works by applying a voltage across a resistor network and measuring the change in resistance at a given point on the matrix where a screen is touched by an input stylus, pen, or finger. The change in the resistance ratio marks the location on the touch screen.The device requires an external reference and an external clock. It operates from a single supply of 2.7V to 5.25V. The external reference can be any voltage between 1V and +VCC. The value of the reference voltage directly sets the input range of the converter.

Single-Ended Mode:

In single-ended mode, when a touch on the touch panel is detected, the processor that controls the ADS7843 will send a control byte to instruct the ADS7843 to perform a conversion.

Differential mode:

The operation of differential mode is similar to single-ended mode except that the internal FET switches will continue to be ON from the start of the acquisition period to the end of the conversion period.

MIWI P2P WIRELESS PROTOCOL

Overview

The Microchip MiWi™ P2P Wireless Protocol is a variation of IEEE 802.15.4, using Microchip's MRF24J40MA 2.4 GHz transceiver and any Microchip 8, 16 or 32-bit microcontroller with a Inter Integrated Circuit (I2C). The protocol provides reliable direct wireless communication via an easy-to-use programming interface. It has a rich feature set that can be compiled in and out of the stack to meet a wide range of customer

SUPPORTED TOPOLOGIES:

IEEE 802.15.4 and the MiWi P2P stack support two topologies: Star and Peer-to-Peer.

Star Topology

From a device role perspective, the topology has one Personal Area Network (PAN) coordinator that initiates communications and accepts connections from other devices. It has several end devices that join the communication

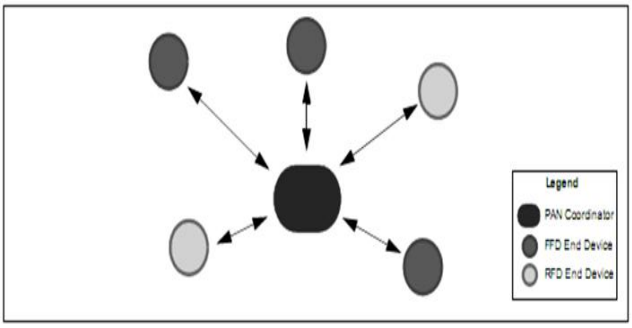

Fig 7.1 Star Topology

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Pin Diagram of MRF24J40MA

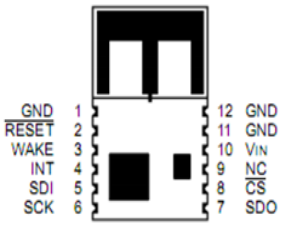

Fig 7.3 Pin Diagram of MRF24J40MA

Pin Description of MRF24J40MA

Table 7.1 Pin Description of MRF24J40MA

Pin	Symbol	Type	Description
1	GND	Power	Ground
2	$\overline{\text{RESET}}$	DI	Global hardware Reset pin
3	WAKE	DI	External wake-up trigger
4	INT	DO	Interrupt pin to microcontroller
5	SDI	DI	Serial interface data input
6	SCK	DI	Serial interface clock
7	SDO	DO	Serial interface data output from MRF24J40
8	$\overline{\text{CS}}$	DI	Serial interface enable
9	NC	—	No connection (allow pin to float; do not connect signal)
10	VIN	Power	Power supply
11	GND	Ground	Ground
12	GND	Ground	Ground

Microcontroller to MRF24J40MA Interface:

I2C PROTOCOL

Overview

I²C is a multi-master serial computer bus that is used to attach low-speed peripherals to a motherboard, embedded system, or cell phone. The name stands for **Inter-Integrated Circuit** and is pronounced I-squared-c.

I2C in PIC Microcontroller

The MSSP module in I2C mode fully implements all master and slave functions (including general call support) and provides interrupts on Start and Stop bits in hardware to determine a free bus (multi-master function).
Two pins are used for data transfer:

1. Serial clock (SCL) – RC3/SCK/SCL
2. Serial data (SDA) – RC4/SDI/SDA

I2C MASTER MODE TRANSMISSION

a. BF Status Flag

In Transmit mode, the BF bit (SSPSTAT<0>) is set when the CPU writes to SSPBUF and is cleared when all eight bits are shifted out.

b. WCOL Status Flag

If the user writes the SSPBUF when a transmit is already in progress (i.e., SSPSR is still shifting out a data byte), the WCOL is set and the contents of the buffer are unchanged (the write doesn't occur). WCOL must be cleared in software.

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c. ACKSTAT Status Flag

In Transmit mode, the ACKSTAT bit (SSPCON2<6>) is cleared when the slave has sent an Acknowledge (ACK = 0) and is set when the slave does Not Acknowledge (ACK = 1).

I2C MASTER MODE RECEPTION

a. BF Status Flag

In receive operation, the BF bit is set when an address or data byte is loaded into SSPBUF from SSPSR. It is cleared when the SSPBUF register is read.

b. SSPOV Status Flag

In receive operation, the SSPOV bit is set when 8 bits are received into the SSPSR and the BF flag bit is already set from a previous reception.

c. **WCOL Status Flag**

If the user writes the SSPBUF when a receive is already in progress (i.e., SSPSR is still shifting in a data byte), the WCOL bit is set and the contents of the buffer are unchanged (the write doesn't occur).

ULTRASONIC SENSOR

Overview

The HC-SR04 ultrasonic sensor uses sonar to determine distance to an object like bats or dolphins do. It offers excellent non-contact range detection with high accuracy and stable readings in an easy-to-use package. It's operation is not affected by sunlight or black material like Sharp rangefinders.

Layout of Sensor

VCC = +5VDC

Trig = Trigger input of Sensor

Echo = Echo output of Sensor

GND = GND

Fig 10.1 Layout of Sensor

Operation

To start measurement, Trig of SR04 must receive a pulse of high (5V) for at least 10us, this will initiate the sensor will transmit out 8 cycle of ultrasonic burst

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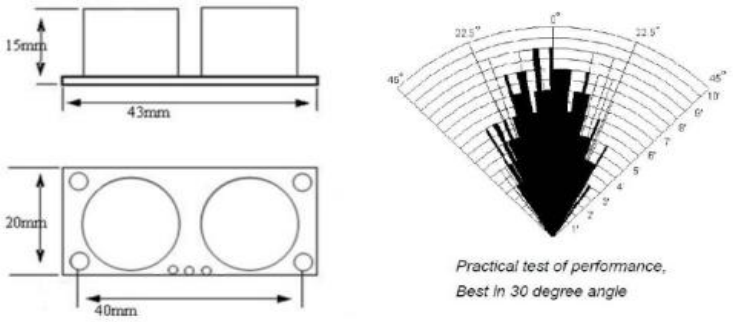
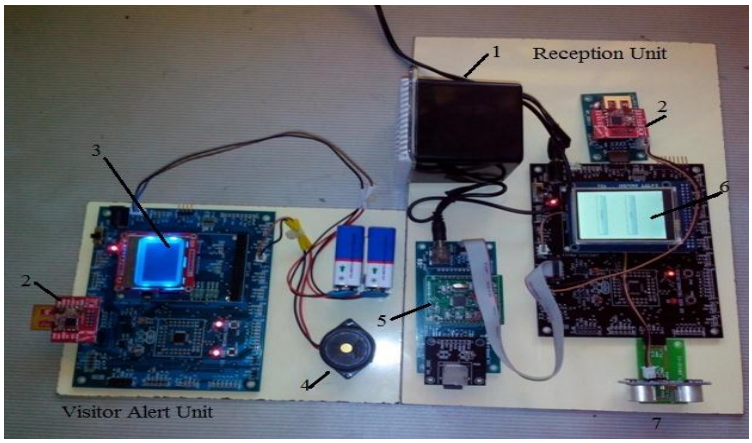


at 40kHz and wait for the reflected ultrasonic burst. When the sensor detected ultrasonic from receiver, it will set the Echo pin to high (5V) and delay for a period (width) which proportion to distance. To obtain the distance, measure the width(Ton) of Echo pin.

Time = Width of Echo pulse, in uS (micro second)

1. Distance in centimeters = Time / 58
2. Distance in inches = Time / 148
3. Or we can utilize the speed of sound, which is 340m/s

HARDWARE VIEW



CONCLUSION

Thus, we designed and implemented the smart reception kit that takes the role of a receptionist and guides the incoming visitors by queuing them in a systematic way and directs them to their respective destinations or officials by showing route maps with the help of touch screen color panel andvoice generation. The human effort is much reduced. With research and development this project can be extended to multilingual voice generation and wide range of network area. In future with enhanced technology our project will be a boon to this world.

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