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Comparative study of THD in Asymmetrical Cascaded H-Bridge Multilevel Inverter in different levels

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ABSTRACT – Cascaded H-Bridge multilevel inverter is a promising topology and built to synthesize a desired ac voltage from several levels of dc voltages with better harmonic spectrum and are suitable for high voltage and high power applications. A small total harmonic distortion is the most important feature of these inverters. This paper compares the total harmonic distortion in 5, 7, 9 and 11 levels of Asymmetrical Cascaded H-Bridge Multilevel inverter employing multicarrier pulse width modulation control technique. Multicarrier pulse width modulation control technique is adopted in the firing circuit to provide an acceptable control in the inverter output voltage. Hence we could achieve the improved efficiency of the system . The analysis has been simulated using MATLAB/SIMULINK. The simulated output shows very favorable result.

KEYWORDS: Multilevel inverter, Cascaded H-Bridge inverter, Total Harmonic Distortion, Multicarrier pulse width modulation

I.INTRODUCTION

The importance of multilevel inverters has been increased since last few decades. These new types of inverters are suitable for high voltage and high power application due to their ability to synthesize waveforms with better harmonic spectrum and with less THD. Numerous topologies have been introduced and widely studied for utility of non conventional sources and also for drive applications. Amongst these topologies, the multilevel cascaded inverter was introduced in Static VAR compensation and in drive systems[1].

The multilevel inverter [MLI] is a promising inverter topology for high voltage and high power applications. This inverter synthesizes several different levels of DC voltages to produce a stepped AC output that approaches the pure sine waveform. It has the advantages like high power quality waveforms, lower voltage ratings of devices, lower harmonic distortion, lower switching frequency and switching losses, higher efficiency, reduction of dv/dt stresses etc. It gives the possibility of working with low speed semiconductors in comparison with the two-level inverters.[2]-[4] Numerous of MLI topologies and modulation techniques have been introduced. But most popular MLI topology is Diode Clamp, Flying Capacitor and Cascaded Multilevel Inverter (CMLI).[5]

In this paper we are using a CMLI that consist of several H-Bridge inverters and with un-equal DC sources named as Asymmetrical type Cascaded Multilevel Inverter (ACMLI) and these inverters are more modular and simple in construction. There are many modulation techniques to control this inverter, such as Selected Harmonics Elimination, Space Vector PWM (SVPWM) and Carrier-Based PWM (CBPWM), Symmetrical step control, Optimization angle control techniques.[6] Multicarrier pulse width modulation control technique is adopted in the firing circuit to provide an acceptable control in the inverter output voltage

II. ASYMMETRICAL CASCADED H-BRIDGE INVERTER

This method eliminates the excessively large number of bulky transformers required by conventional multi level inverters, the clamping diodes required by diode clamped multilevel inverters and the bulky capacitors required by flying capacitor multilevel inverters. Figure 1 shows the cascaded h-bridge multilevel inverter with unequal dc sources.

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This method consists of a series connection of multiple H bridge inverters. Each H-bridge inverter has the same configuration as a typical single-phase full-bridge inverter. This method introduces the idea of using separate DC sources to produce an AC voltage waveform which is nearly sinusoidal. Each H bridge inverter is connected to its own DC source. By cascading the output voltage of each H-bridge inverter, a stepped voltage waveform is produced. If the number of H-bridges is N, the voltage output is obtained by summing the output voltage of bridges as shown in equation. If ACMLI has N no. Of H-Bridges, The output voltage could be expressed as ; $Vo\ (t) = Vo1\ (t) + Vo2\ (t) + ... + Vo\ N\ (t)$ (1) Where, $Vo1\ (t)$,$Vo2\ (t)$, ... $Vo\ N\ (t)$ are the output of individual H-bridge. In ACMLI DC voltage with ratio binary and ternary are the most popular. In binary progression within H-Bridge inverters , the DC voltages having ratio 1: 2: 4: 8. . : 2N and the maximum voltage output would be (2N-1) V dc and the voltage levels will be (2N+1-1). While in the ternary progression the amplitude of DC voltages having ratio 1: 3: 9: 27. . : 3N and the maximum output voltage reaches to ((3N- 1)/2) V dc and the voltage levels will be(3N) .[7]

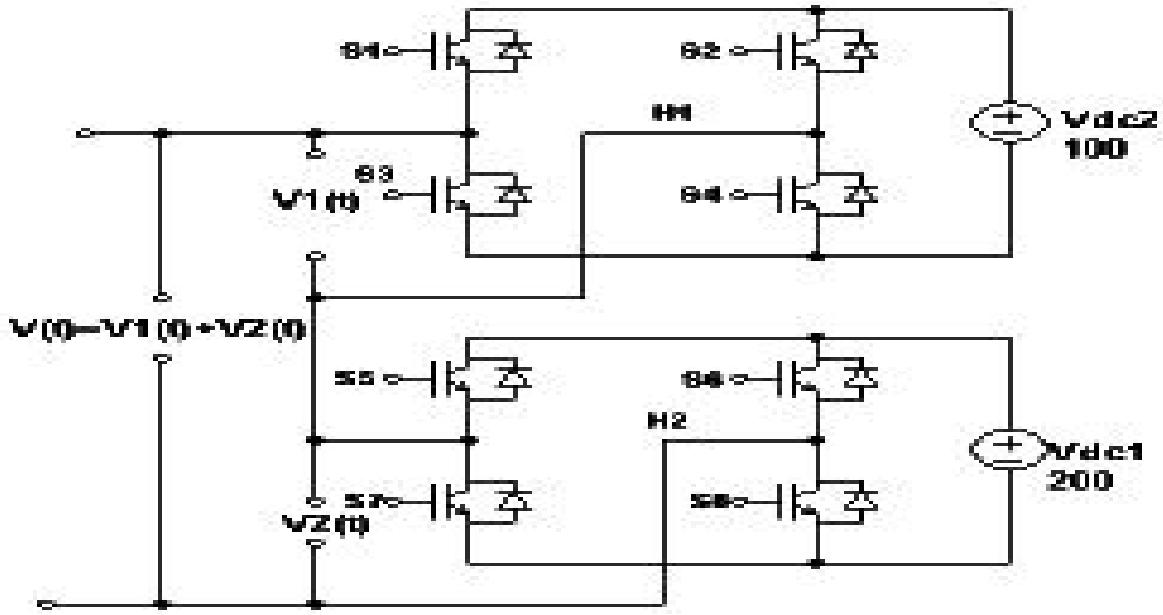

Fig.1.Cascaded MLI with unequal dc sources.

III. PWM FOR HARMONICS REDUCTION

Several modulation strategies have been developed for multilevel inverters. The most commonly used is the multi carrier PWM technique. The principle of the multicarrier PWM is based on a comparison of a sinusoidal reference waveform with triangular carrier waveforms. m-1 carriers are required to generate m levels. The carriers are in continuous bands around the reference zero. They have the same amplitude Ac and the same frequency fc. The sine reference waveform has a frequency fr and Ar is the peak to peak value of the reference waveform. At each instant, the result of the comparison is 1 if the triangular carrier is greater than the reference signal and 0 otherwise. The output of the modulator is the sum of the different comparisons which represents the voltage level. The strategy is therefore characterized by the two following parameters called amplitude modulation index ma and frequency modulation index mf .[8]

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IV. SIMULATION RESULTS

In this paper, the simulation model is developed with MATLAB/SIMULINK. The Simulink model of the asymmetrical eleven level inverter and THD analysis are shown in figure 2 and 3. The Simulink model of the asymmetrical nine level inverter and THD analysis are shown in figure 4 and 5. The Simulink model of the asymmetrical seven level inverter and THD analysis are shown in figure 6 and 7. The Simulink model of the asymmetrical five level inverter and THD analysis are shown in figure 9 and 8. The circuit needs independent dc source from photovoltaic cell.

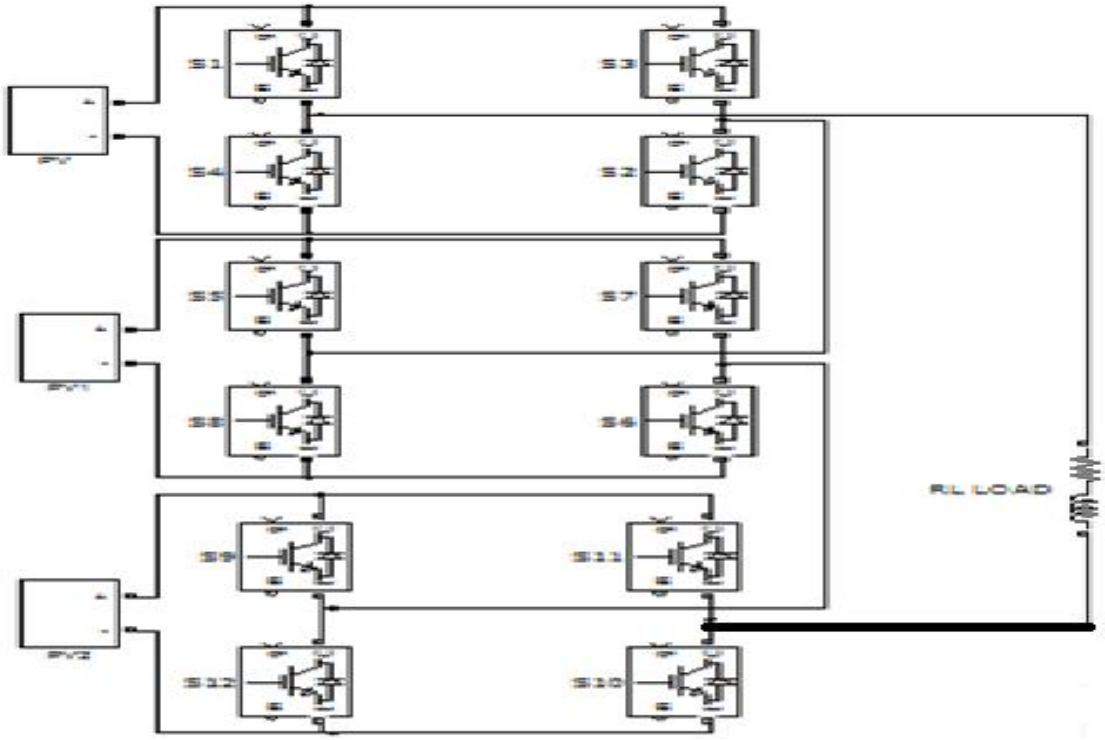

Fig.2 Simulink model of eleven level inverter

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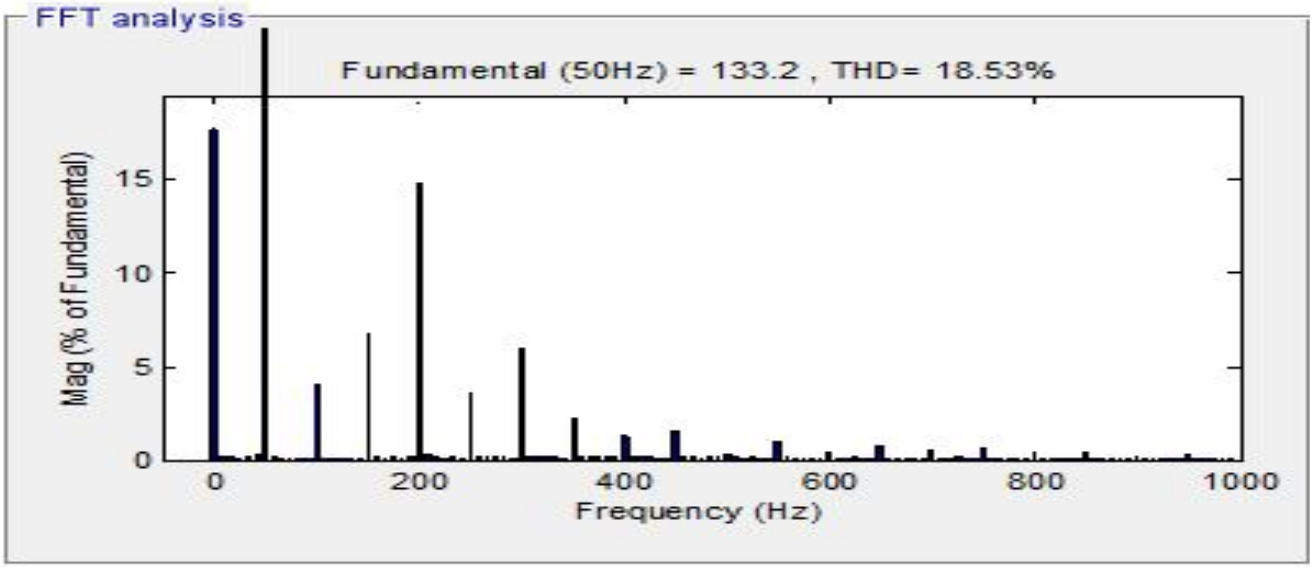

Fig. 3 FFT Analysis for eleven level inverter

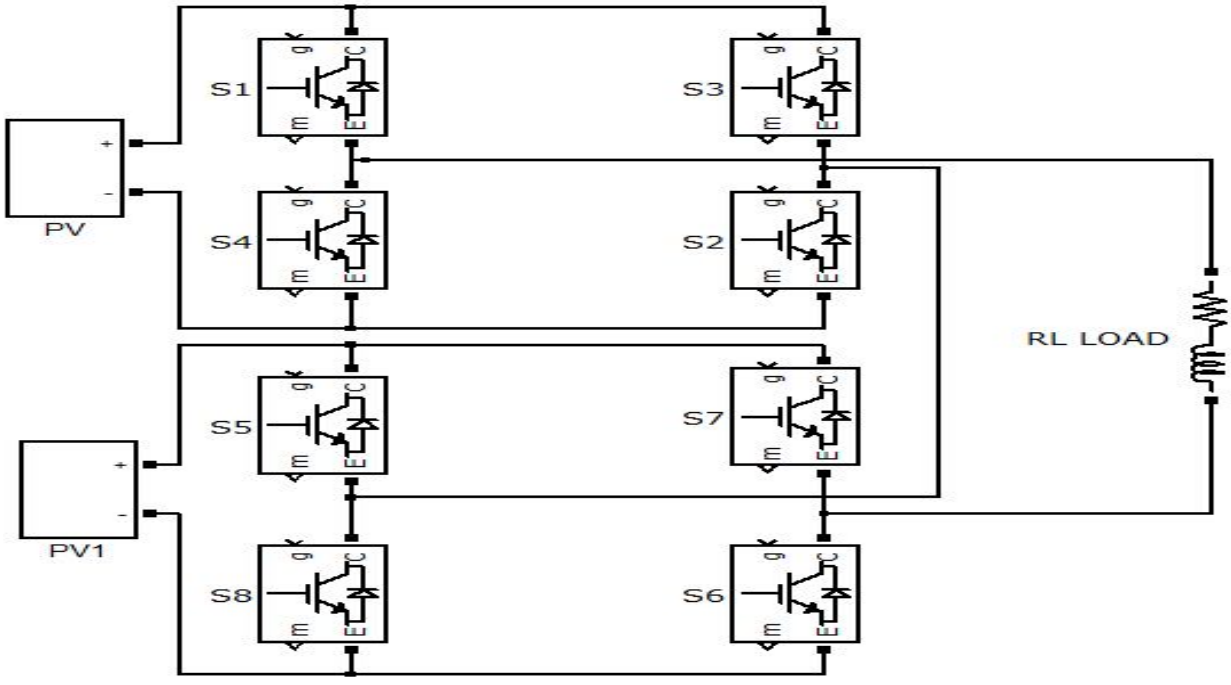

Fig.4 Simulink model of nine level inverter

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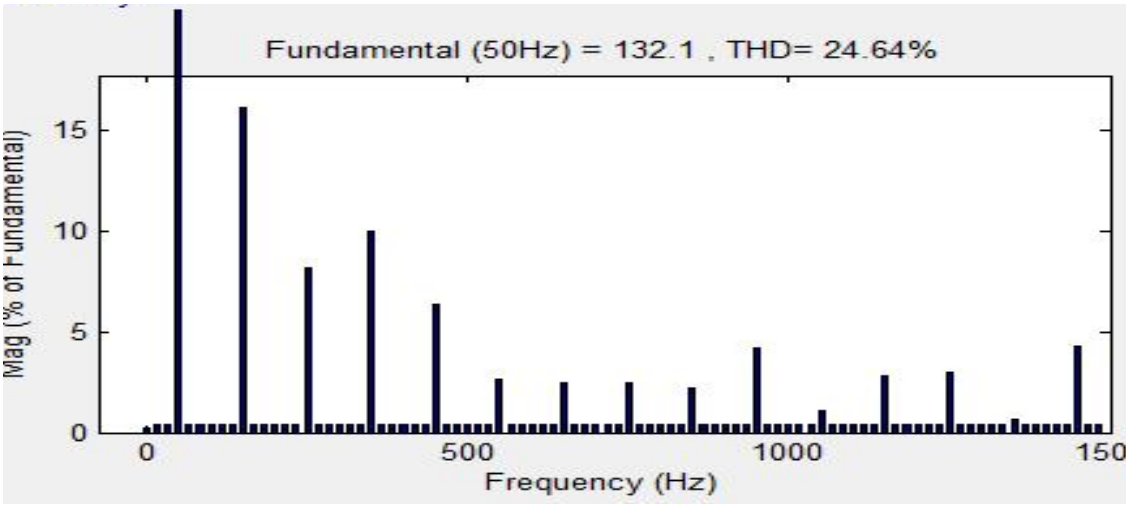

Fig. 5 FFT Analysis for nine level inverter

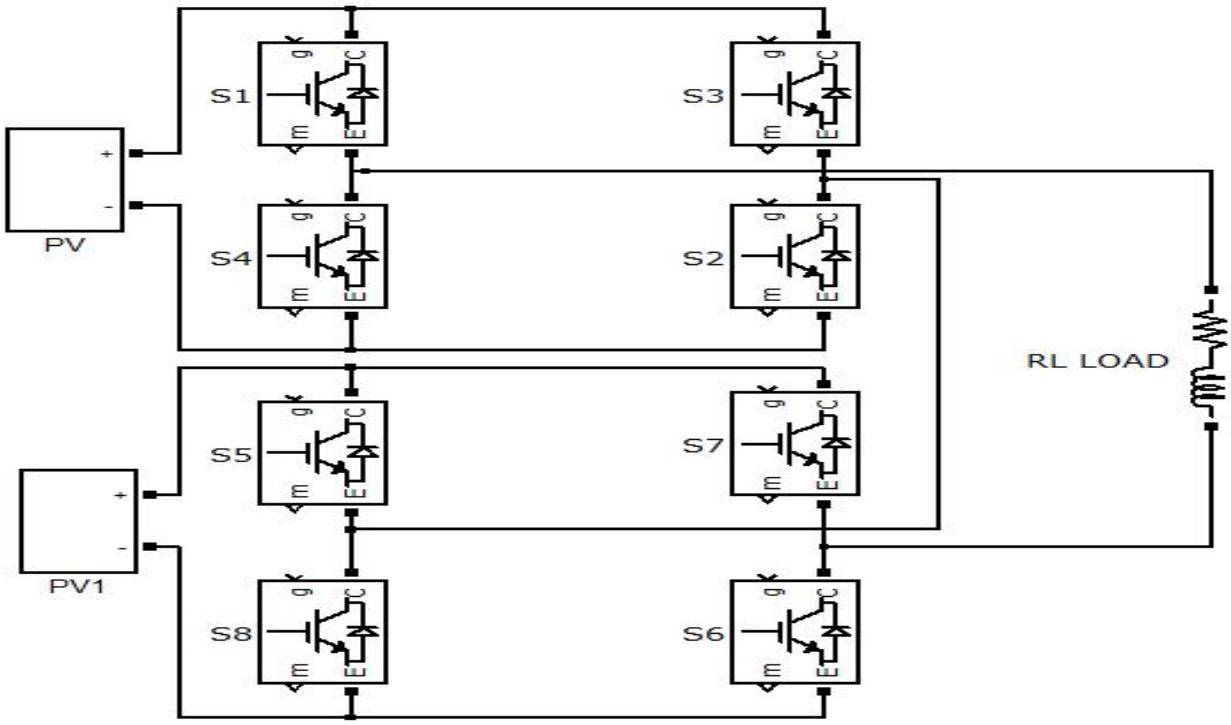

Fig.6 Simulink model of seven level inverter

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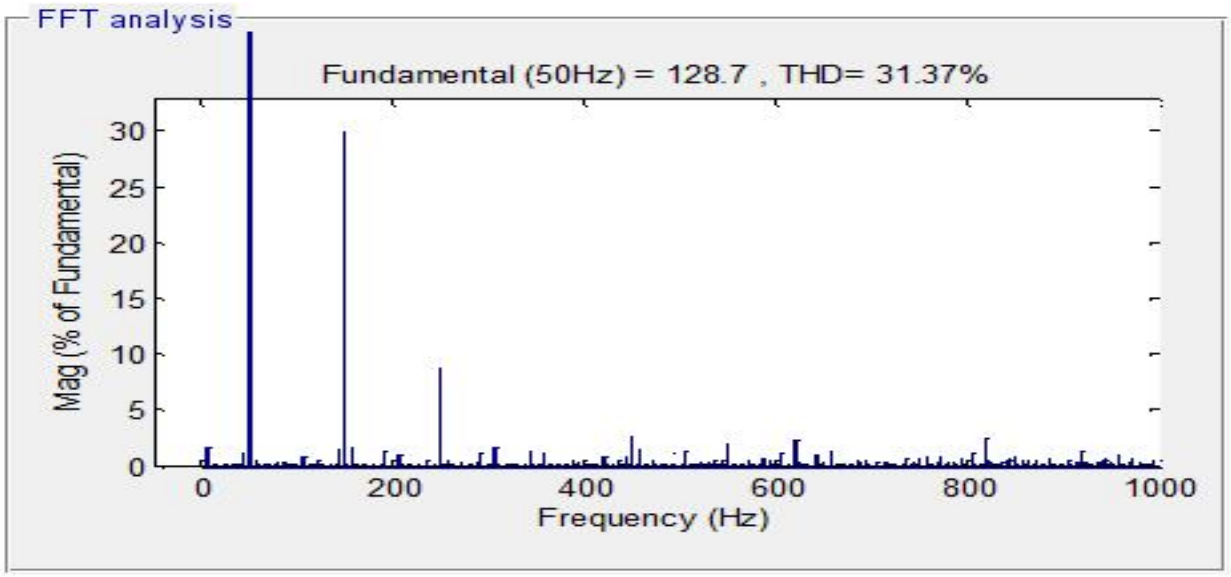

Fig. 7 FFT Analysis for seven level inverter

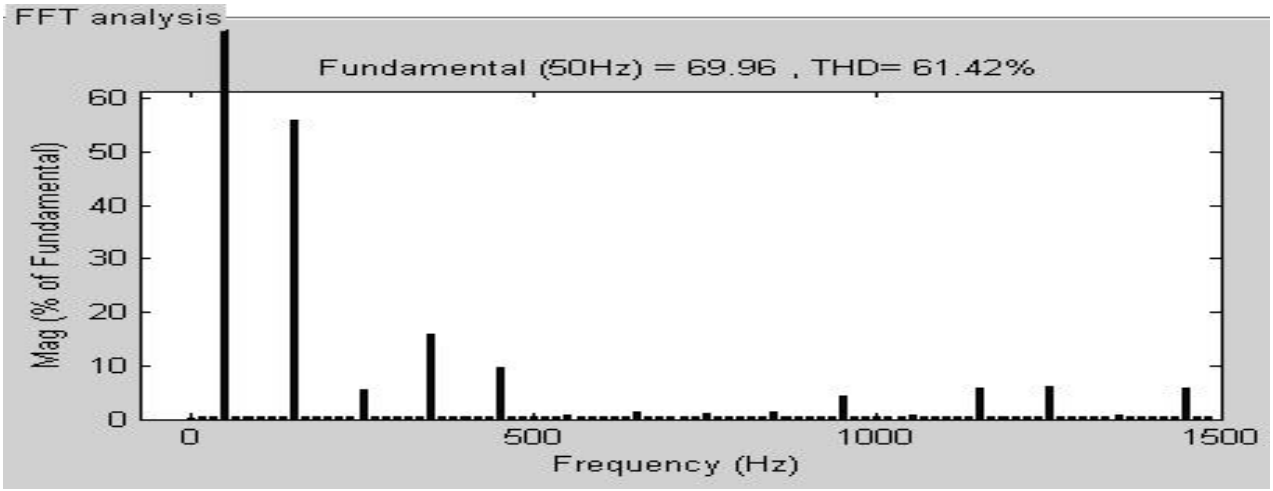

Fig. 8 FFT Analysis for five level inverter

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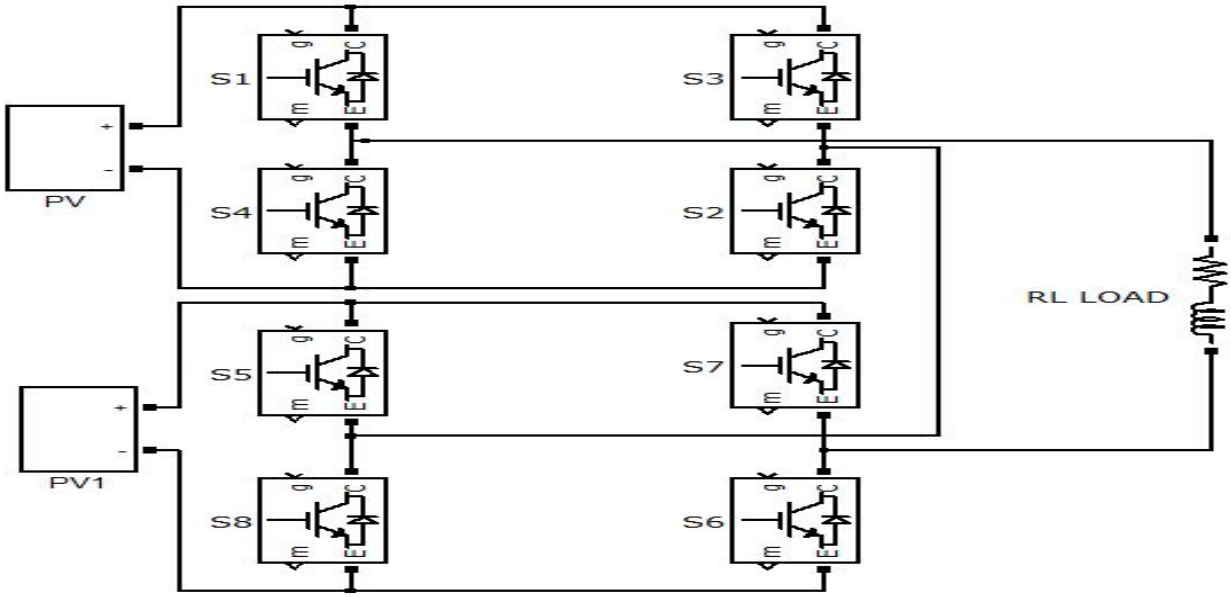

Fig.9 Simulink model of five level inverter

Table I shows the comparison of THD performance in different levels of asymmetrical cascaded h-bridge inverter.

Table .I Comparison of THD performance in different levels

Cascaded H-Bridge Inverter in different levels	THD(%)	Switches
5	61.42	8
7	31.37	8
9	24.64	8
11	18.53	12

VII. CONCLUSION

In the present work, performance of asymmetrical cascaded h-bridge inverter in different levels with photovoltaic cell as its input source by using multicarrier pwm technique has been analyzed by the MATLAB/Simulink From the simulated analysis , as number of level increases, the THD content approaches to small value as expected. Also it uses least number of devices to produce higher voltage level. Hence the future work may be focused on implementing closed loop control to achieve better performance of the inverter.

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