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Delay Locked Loop Using Glitch Free Nand-Based DCDL

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ABSTRACT: A delay locked loop (DLL) is used to synchronize the external and internal clock. This is used to reduce the clock-deskew problem. The main block in DLL is delay line. Digitally controlled delay lines (DCDL) exhibits a glitching problem. This glitching problem is reduced by using NAND-Based DCDL. Sense amplifier based driving circuit is used to control the control bits in DCDL. The proposed DCDL is adopted in the DLL in order to reduce the power and delay time.

KEYWORDS: DLL, PLL, Phase comparator, DCDL and Shift register.

I.INTRODUCTION

In electronics, a delay-locked loop (DLL) is a digital circuit similar to a phase-locked loop (PLL), but internal voltage-controlled oscillator is not present in the DLL as like PLL. The clock rise-to-data output valid timing characteristic of integrated circuit is enhanced by DLL. DLL is also used for clock recovery (CDR). A DLL can be seen as a negative-delay gate placed in the clock path of a digital circuit. The main key block of a DLL is a delay chain. DLL provides high-bandwidth data transmission rates between devices. DLL transmissions doesn't have low clock skew between output clock signals, propagation delay and advanced clock domain control. A DLL is fed by a reference clock. A DLL tries to determine the period of that reference clock by adjusting a feedback look via the delay line. The loop is considered locked when the delayed clock signal matches the incoming clock signal.

Reducing the clock skew can not only further increase system clock frequency but also avoid system malfunction. Phase-locked loops (PLL's) and delay-locked loops (DLL's) have been widely adopted to solve the clock-skew problem. Such kinds of circuits are called clock-deskew buffers. A DLL consists of a phase detector (PD) or a phase comparator (PC), a variable delay line, and a shift register to convert the PD's output signal to a control signal for the delay line. It detects the phase error between the input clock and its output clock and automatically tunes the delay line to insert an optimal delay time between them for clock synchronization.

II. EXISTING DLL

The DLL has delay line, phase comparator and shift register as the components. Figure.1 shows the block diagram of the register-controlled DLL (RDLL). The feedback clock signal is the delayed version of the input clock signal, and the shift register controls the amount of the delay time. The PC compares the phases of the input clock signal and the output clock signal. The output of the PC is used to control the shift register. The input clock signal is a common input for every delay stage.

At any time, only one bit of the shift register is active to select a point of entry of the delay line for the input clock signal. The number of the delay stages which the input clock signal goes through determines total amount of delay. Under this circumstance, the loop is locked and will not alter until the phase error exceeds the unit delay again. The resolution of the RDLL is determined by the unit delay of the delay line and the total delay time of the delay line

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determines the DLL's deskew range and the lowest operation frequency. Wider deskew range or lower operation frequency can be achieved by adding more delay stages in the delay line.

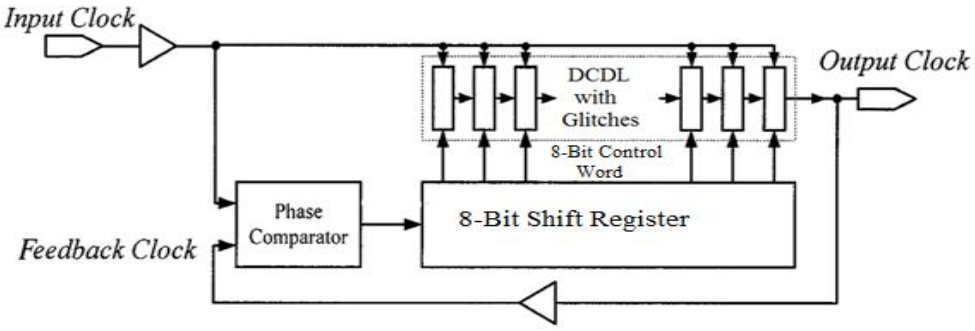

Figure.1. DLL with glitching DCDL

A phase detector or phase comparator is a logic gate that generates a voltage signal which represents the difference in phase between two signal inputs. It is an essential element of the phase-locked loop (PLL). Detecting phase difference is very important in many applications, such as radar and telecommunication systems, servo mechanisms, and demodulators.

A.DLL WITH GLITCH FREE NAND-BASED DCDL

In the glitching DCDL circuit [8], only one control bit is used. When there is a sudden switching takes place in the control bit, glitches are generated. Figure 2 represents DLL with
glitch free NAND-Based DCDL.

Figure 3 represents the glitch free NAND-Based DCDL. This uses two control bits S_i and T_i. In this figure "A" denotes the fast input of each NAND gate. Gates marked with "D" represents dummy cells added for load balancing. When Si=0 and Ti=1 the NAND "3" output is equal to 1 and the NAND "4" allows the signal propagation in the lower NAND gates chain. And if Si=1 and Ti=1, the state is turn state. In this state the upper input of the DE is passed to the output of NAND "3". If Si=1 and Ti=0 the state is post-turn state. In this DE the output of the NAND "4" is stuck-at 1, by allowing the propagation, in the previous DE (which is in turn-state), of the output of NAND "3" through NAND "4". The circuit of figure.3 is an inverting DCDL. In this circuit the first DE is never in post-turn state, therefore T0 is always 1.

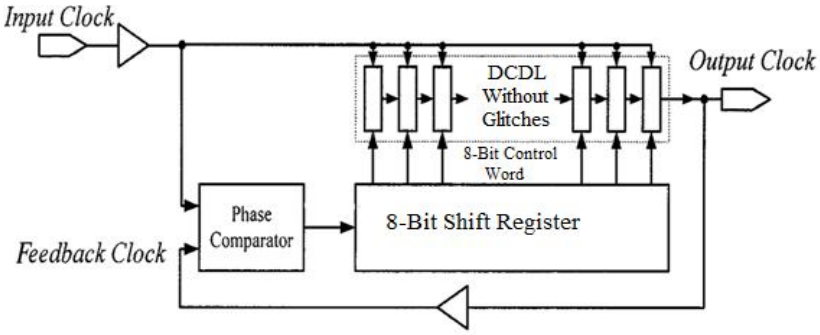

Figure.2. DLL with glitch free NAND-Based DCDL

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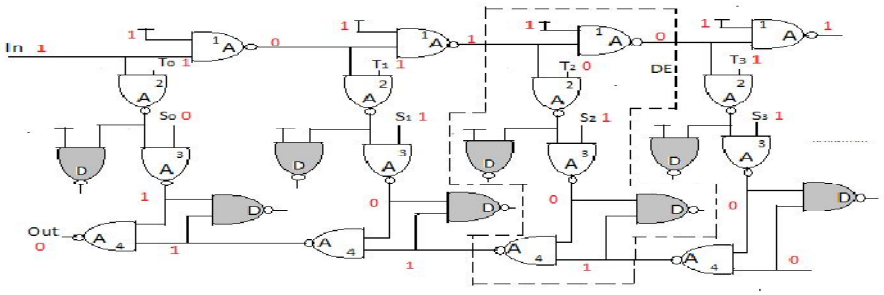

Figure.3. Glitch free NAND-Based DCDL

B.DRIVING CIRCUIT

Driving circuit can be used to generate the control-bits of the DCDL. By analysing, it can be noted that S_i signals have to be delayed with respect to T_i signals and that it could be useful to have a different delay for LH and HL transitions. The existing DCDL uses dual edge triggered flip-flop as the driving circuit. This consumes more power. When this is adopted in the DLL, this power consumption is also high. In figure 4 driving circuit is shown with DCDL.

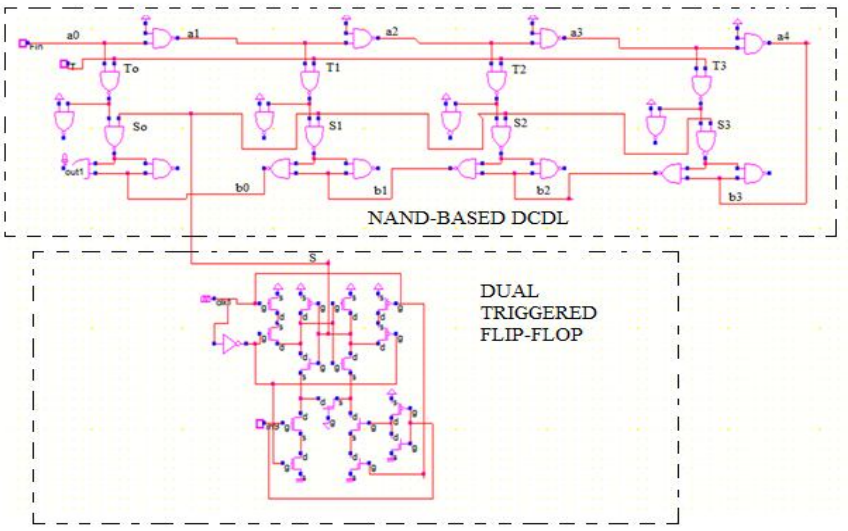

Figure.4.glitch free NAND-Based DCDL with driving circuit (dual edge triggered flip-flop)

III. PROPOSED DLL

A.DLL WITH PROPOSED GLITCH FREE NAND-BASED DCDL

Proposed DLL uses proposed glitch free DCDL .by using this DLL power and delay time is reduced.

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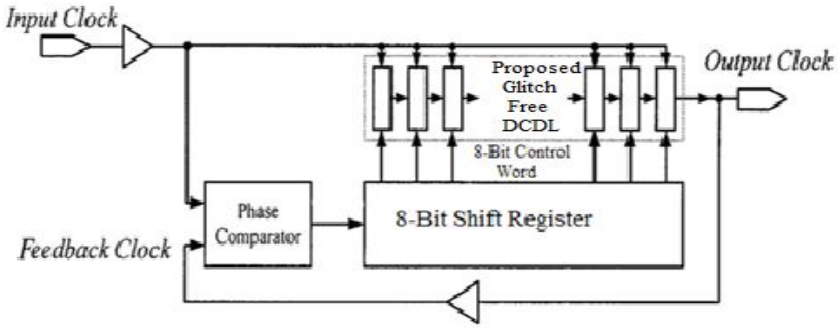

Figure.5.DLL with Proposed Glitch Free NAND-Based DCDL

B.PROPOSED DCDL

Proposed DCDL uses dual edge triggered sense amplifier flip-flop as a driving circuit. This is shown in figure 6. By using this proposed driving circuit, the power and delay time of existing glitch free NAND-Based DCDL is reduced. The sense amplifier based dual triggered flip-flop in figure 6 consists of three stages. Those are pulse generating, sensing and latching stages. First stage is used to generate the pulses, second stage is used to sense the pulses and third stage is used to produce the output during the rising and falling edges.

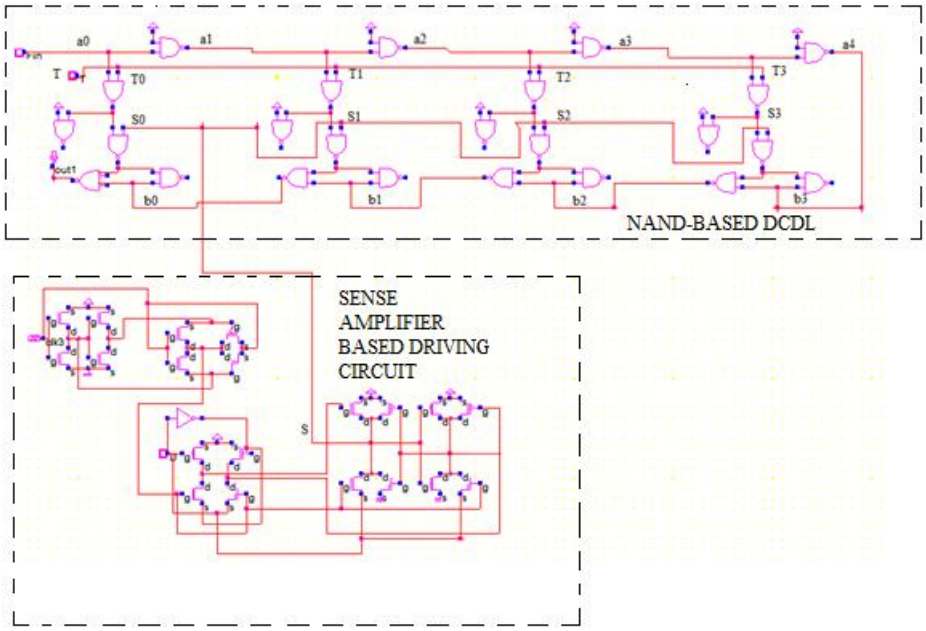

Figure.6. NAND-Based DCDL with Sense Amplifier Driving Circuit

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IV.SIMULATION RESULTS AND DISCUSSION

1. DLL with Glitching NAND-Based DCDL

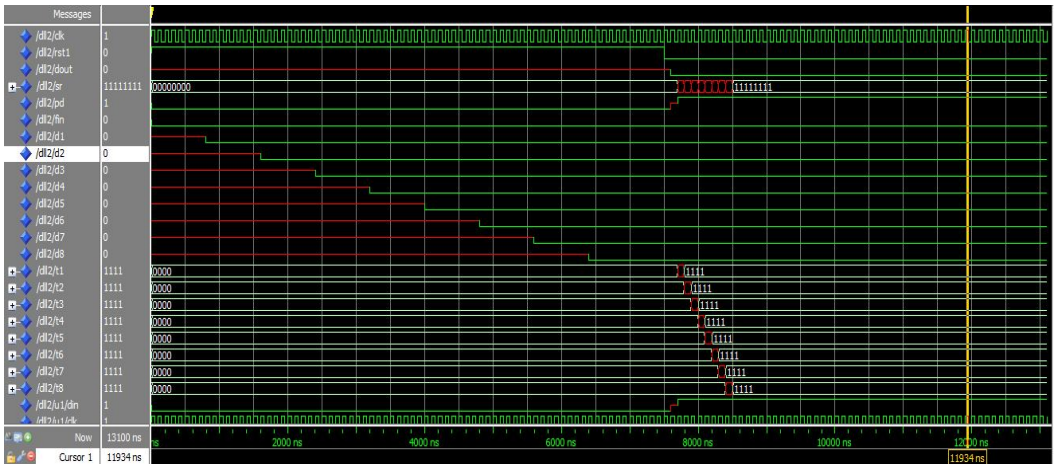

Figure.7 DLL with Glitching NAND-Based DCDL

The above figure shows that DLL with glitching NAND-Based DCDL.

2. Simulation Result of DLL with existing glitch free DCDL

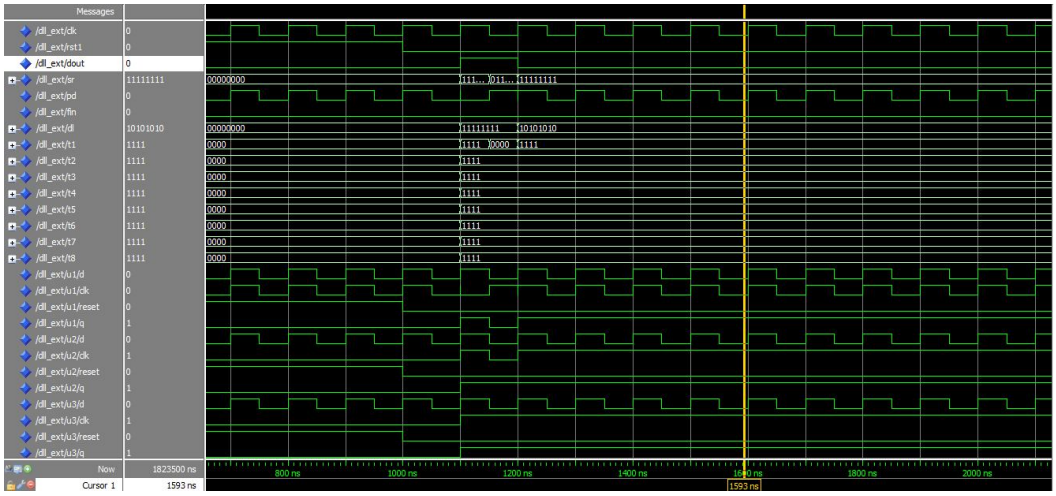

Figure.8 Simulation result of DLL with existing glitch free NAND-Based DCDL

The figure.8 shows that Delay Locked Loop with existing glitch free NAND-Based DCDL.

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3. Simulation Result of DLL with Proposed Glitch Free NAND-Based DCDL

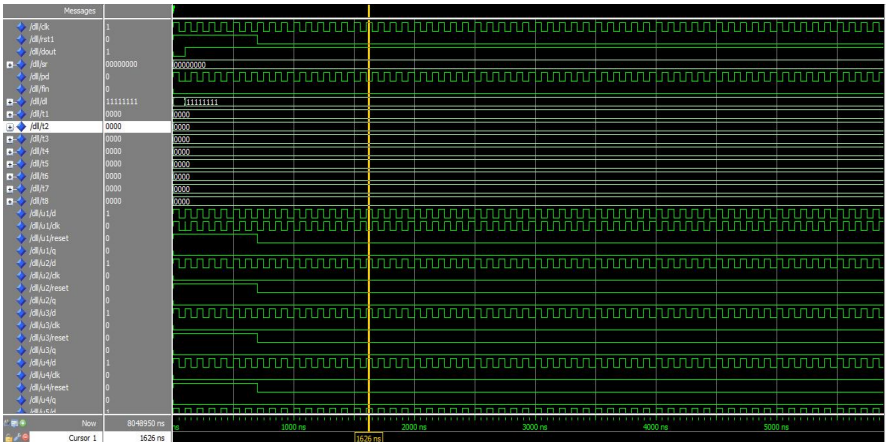
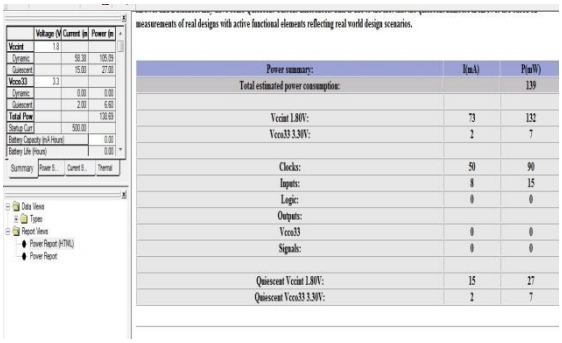


Figure.9 Simulation of DLL with Proposed Glitch Free NAND-Based DCDL

The figure.9 shows that simulation of DLL with Proposed Glitch Free NAND-Based DCDL.

4. Existing DLL Power Analysis



Power summary:	I(mA)	P(mW)
Total estimated power consumption:		139
Vccint 1.80V:	73	132
Vcco33 3.30V:	2	7
Clocks:	50	90
Inputs:	8	15
Logic:	0	0
Outputs:		
Vcco33	0	0
Signals:	0	0
Quiescent Vccint 1.80V:	15	27
Quiescent Vcco33 3.30V:	2	7

Figure.10 Existing DLL Power Analysis

5. Proposed DLL Power Analysis

Figure.11 Proposed DLL Power Analysis

5. Delay Time Analysis of Existing DLL

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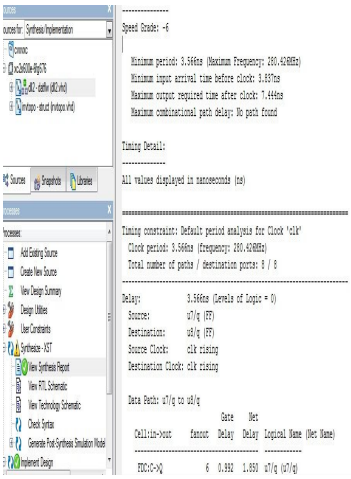

Figure 3.11 Delay Time Analysis of Existing DLL

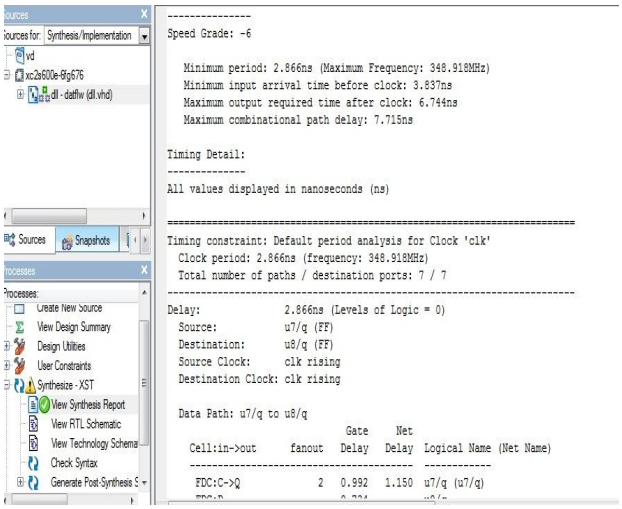

Figure 3.12 Delay Time Analysis of Proposed DLL

6. Delay Time Analysis of Proposed DLL

7. COMPARISON OF POWER AND AREA

Comparison Chart for Power

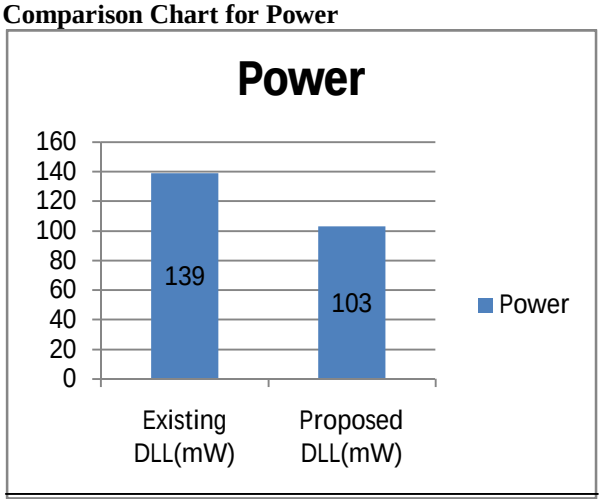

Figure 3.13 Comparison chart for power

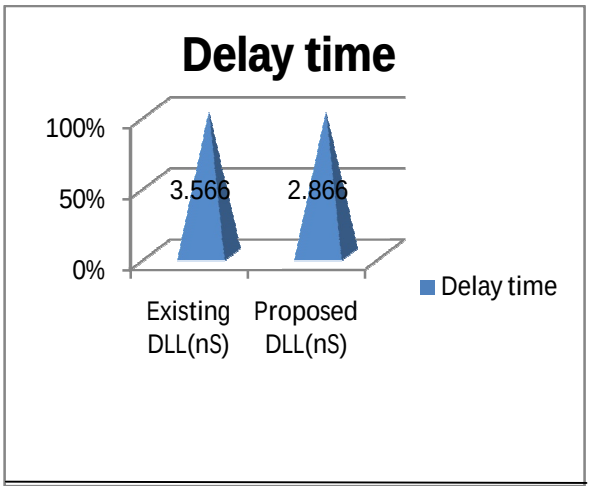

Figure 3.14 Comparison chart for Delay time

Comparison Chart for Delay Time

V.CONCLUSION

A Delay Locked Loop with glitch free NAND-Based DCDL has been presented. Digitally Controlled Delay Lines plays an important role in DLL and the drawback is glitches. A NAND-based DCDL is used to reduce the glitches with dual edge triggered sense amplifier flip-flop as driving circuit. The DCDL circuit consumes low power. The DLL uses the proposed DCDL circuit in order to reduce the power, area and delay time. The comparison of existing and proposed DLL has been presented. The output is shown by using FPGA kit. The simulation results confirm the correctness of developed model and show that proposed solutions improve the resolution with respect to previous approaches.

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REFERENCES

[1] B.W. Garlepp, K.S. Donnelly, Jun Kim, P.S. Chau, J.L.Zerbe, Charless Huang, C.V. Tran, C.L.Portmann, Donald Stark, Yin-Fai Chan, T.H.Lee and M.A. Horowitz, "A Portable Digital DLL for High-Speed CMOS Interface Circuits," JSSC, 34(5):632-644, May 1999.

[2] B. M. Moon, Y. J. Park, and D. K. Jeong, "Monotonic wide-range Digitally controlled oscillator compensated for supply voltage variation", IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 55, no. 10, pp.1036–1040, Oct 2008.

[3] T. M. Matano, Y.Takai, T.Takahashi, Y.Sakito, I.Fujii, Y.Takaishi, H.Fujisawa, S.Kubouchi, S.Narui, K.Arai, M.Morino, M.Nakamura, S.Miyatake, T.Sekiguchi and K.Koyama, " A 1-Gb/s/pin 512-Mb DDRII SDRAM using a digital DLL and a slew-rate-controlled output buffer", IEEE J. Solid-State Circuits, vol. 38, no. 5, pp. 762–768. May 2003.

[4] R. J. Yang and S. I. Liu, "A 40–550 MHz harmonic-free all digital Delay locked loop using a variable SAR algorithm", IEEE J. Solid-State Circuits, vol.42, no. 2, pp. 361–373. Feb 2007.

[5] R. J. Yang and S. I. Liu, "A 2.5 GHz all digital delay locked loop in 0.13 mm CMOS technology", IEEE J. Solid-State Circuits, vol. 42, no.11, pp. 2338–2347. Nov 2007.

[6] L. Wang, L. Liu, and H. Chen, "An implementation of fast-locking And wide-range 11-bit reversible SAR DLL", IEEE Trans.Circuits Syst. II,Exp. Briefs, vol. 57, no. 6, pp. 421–425. Jun 2010.

[7] Guang-Kaai Dehng, June-Ming Hsu, Ching-Yuan Yang, and Shen-Iuan Liu(2000), "Clock-Deskew Buffer Using a SAR-Controlled Delay-Locked Loop," IEEE J.Solid-state circuits vol. 35, no. 8.

[8] David De Caro, "Glitch Free NAND-Based Digitally Controlled Delay Lines", IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 21, no. 1, Jan 2013.

[9] A. G. M. Strollo, D. De Caro, E. Napoli, and N. Petra, "A novel high speed sense amplifier based flip-flop", IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 13, no. 11, pp. 1266–1274, Nov. 2005.

[10] D. D. Caro, C.A.Romani, N.Petra, A.G.M.Strollo and C.Parrella, " A 1.27 GHz, all digital spread spectrum clock generator/synthesizer in 65 nm CMOS", IEEE J. Solid-State Circuits, vol. 45, no. 5, pp. 1048–1060.May 2010.