



Power and Delay Analysis of Double Edge Triggered D-Flip Flop based Shift Registers in 16nm MOSFET Technology

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ABSTRACT: Flip-Flop is an electronic circuit that stores a logical state of one or more data input signals in response to a clock pulse. During recurring clock intervals to receive and maintain data for a limited time period sufficient for other circuits within a system to further process data. Power dissipation is an important parameter in the design of VLSI circuits, and the clock network is responsible for a substantial part of it (up to 50%). When the supply voltage is decreased the speed of the logic circuits might be diminished due to reduction in effective input voltage to the transistors. The optimal supply voltage for CMOS logic in terms of Energy-Delay-Product (EDP) is close to the threshold voltage of the nMOS transistor V_{tn} for the actual process, assuming that the threshold voltage of the pMOS transistor V_{tp} is approximately equal to $-V_{tn}$. The famous Moore's law states that the number of transistors that are to be integrated on a single die gets doubled for every 18 months and which proves that area of the design is also a major concern. Hence in this paper all the three major concerns of VLSI world, the power consumed, speed and area consumption are concentrated.

KEYWORDS: Double Edge Triggered D-Flip Flop, Shift Registers, MOSFET, Power, and Delay.

I.INTRODUCTION

Low Power digital CMOS becomes more and more interesting, due to the general advances in process technology and new low power applications. The advancements in the field of CMOS technology have promoted a continuous increase in the density of integration as well as in the frequency of operation of the VLSI ICs. As technology advances push for smaller devices and faster operations, power consumption and noise become severe problems when designing high-speed ICs. These challenging concerns are mainly due to the excessive switching activity. In this paper a new Double Edge Triggered D Flip Flop is proposed by comprehensive modelling of the existing design. The D-FF is then designed in 16nm MOSFET technology using the 16nm MOSFET PTM model. Shift registers including Serial in Serial Out (SISO), Serial In Parallel Out (SIPO), Parallel in Serial Out (PISO) and Parallel in Parallel Out (PIPO) are designed using the existing and proposed D-FF and performance parameters like Power and Delay and analysed and compared for all the designs.

II.DESCRPTION OF D - FLIP FLOPS

The working of D flip flop is similar to the D latch except that the output of D Flip Flop takes the state of the D input at the moment of a positive edge at the clock pin (or negative edge if the clock input is active low) and delays it by one clock cycle. That's why, it is commonly known as a delay flip flop. The D FlipFlop can be interpreted as a delay line or zero order hold. The advantage of the D flip-flop over the D-type "transparent latch" is that the signal on the D input pin is captured the moment the flip-flop is clocked, and subsequent changes on the D input will be ignored until the next clock event. When a circuit is edge triggered the output can change only on the rising or falling edge of the clock. But in the case of level-clocked, the output can change when the clock is high (or low). In edge triggering output can change only at one instant during the lock cycle; with level clocking output can change during an entire half cycle of the clock. This operation is clearly explained diagrammatically. The basic structure or description of DFF and its timing diagram responses are explained below.

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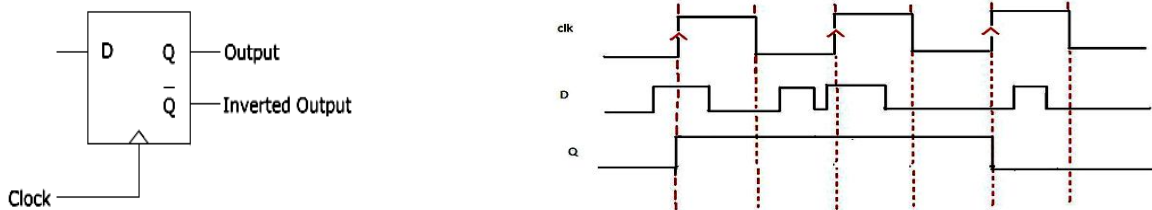


Fig. 1 Description of D – Flip Flop with its timing diagram

The conventional D – Flip flop is the very basic design of DFF. Latches are often called level-sensitive because their output follows their inputs as long as they are enabled. They are transparent during this entire time when the enable signal is asserted. There are situations when it is more useful to have the output change only at the rising or falling edge of the enable signal. This enable signal is usually the controlling clock signal. Thus, we can have all changes synchronized to the rising or falling edge of the clock. An edge triggered DFF achieves this by combining in series a pair of latches. The first latch is called the master latch. The master latch is enabled when $Clk = 0$ and follows the primary input D. When Clk is a 1, the master latch is disabled but the second latch, called the slave latch, is enabled so that the output from the master latch is transferred to the slave latch. The slave latch is enabled all the while that $Clk = 1$, but its content changes only at the beginning of the cycle, that is, only at the rising edge of the signal because once Clk is 1, the master latch is disabled and so the input to the slave latch will not change. . The conventional DFF constructed with NAND gates is given below. It has four NAND gates altogether and an inverter.

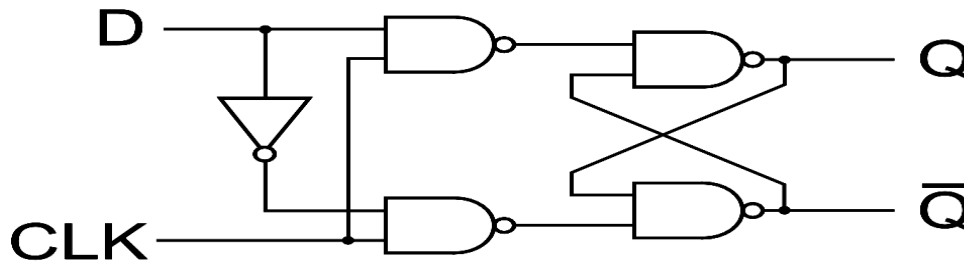


Fig. 2 Description of conventional D – Flip Flop constructed with NAND gates

III.DOUBLE EDGE TRIGGERED D – FLIP FLOP DESIGNS

There are several ways to implement a Double Edge Triggered Flip Flop. In general they can be categorized into two ways. The first idea is to insert additional circuitry to generate internal pulse signals on each clock edge. The second idea is to duplicate the pathway to enable the flip-flop to sample data on every clock edge.

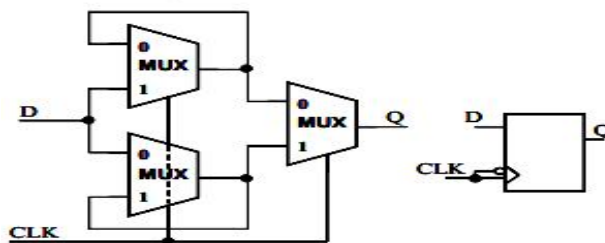


Fig. 3 Description of basic Double edge triggered D – Flip Flop

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The same data throughput can be achieved with half of the clock frequency by using DETFF. In other words double edge clocking can be used to save half of the power on the clock distribution network. The major advantage of double edge triggered flip-flops compared to single edge triggered flip flop is that the delay can be optimized to greater extents and can be used for very high speed applications. Reducing the number of clocked transistors in the designs will automatically reduce the power consumption and delay. The area is also reduced in this case. The MUX can be realized with two CMOS transmission gates, therefore, the logic structure can be easily used to design the CMOS DET flip-flop . Note that two inverters are inserted in the feedback path to restore the level in two latches. Besides, all three MUXs are simply composed of a pair of MOS transistors for reducing number of transistors.

IV.SHIFT REGISTERS

1. Serial In Serial Out Shift Register (SISO) : The serial in/serial out shift register accepts data serially that is, one bit at a time on a single line. It produces the stored information on its output also in serial form. Diagrammatically it is explained below. It is nothing but the series of Flip Flops connected together where the output of the first DFF is fed as the input to the second and second to third and keep going. All the DFF's are set and reset by a single clock signal.

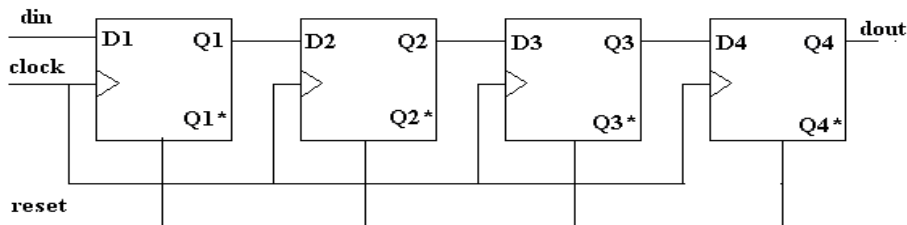


Fig. 4 Serial In Serial Out Shift Register (SISO)

2. Serial In Parallel Out Shift Register (SIPO) : This configuration allows conversion from serial to parallel format. Data is input serially, as described in the SISO section above. Once the data has been input, it may be either read off at each output simultaneously, or it can be shifted out and replaced. Serial in parallel out diagram is shown in fig.5 For this kind of register, data bits are entered serially in the same manner as discussed in the last section. The difference is the way in which the data bits are taken out of the register.

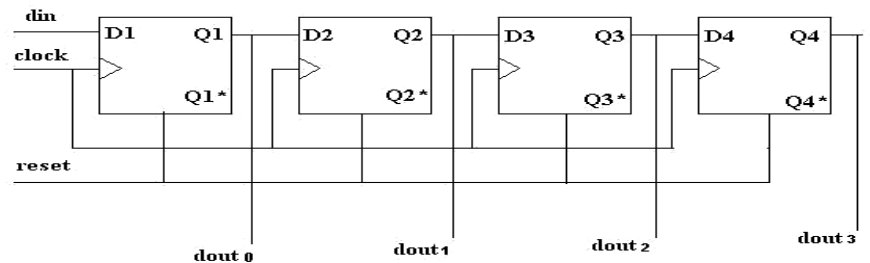


Fig. 5 Serial In Parallel Out Shift Register (SIPO)

3. Parallel In Serial Out Shift Register (PISO) : This configuration has the data input on lines d1 through d4 in parallel format. To write the data to the register, the write/shift control line must be held low. To shift the data, the w/s control line is brought high and the registers are clocked. The arrangement now acts as a PISO shift register, with d1 as the data input. However, as long as the number of clock cycles is not more than the length of the data-string, the data output, q, will be the parallel data read off in order as shown in Fig.6.

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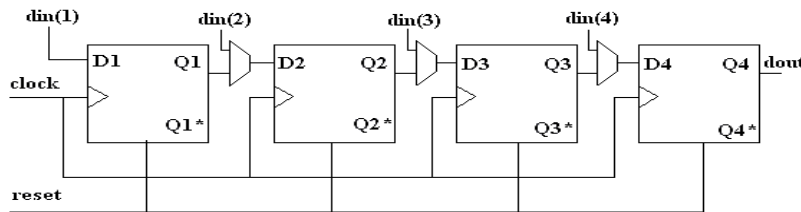


Fig. 6 Parallel In Serial Out Shift Register (PISO)

3. Parallel In Parallel Out Shift Register (PIPO) : For parallel in parallel out shift registers, all data bits appear on the parallel outputs immediately following the simultaneous entry of the data bits. The following circuit is a four-bit parallel in - parallel out shift register constructed by d flip-flops and shown in fig 7. Both the inputs as well as the outputs perform the parallel operation. A global clock is given to activate all the flip flops connected as shown below. The D's are the parallel inputs and the Q's are the parallel outputs. Once the register is clocked, all the data at the d inputs appear at the corresponding q outputs simultaneously.

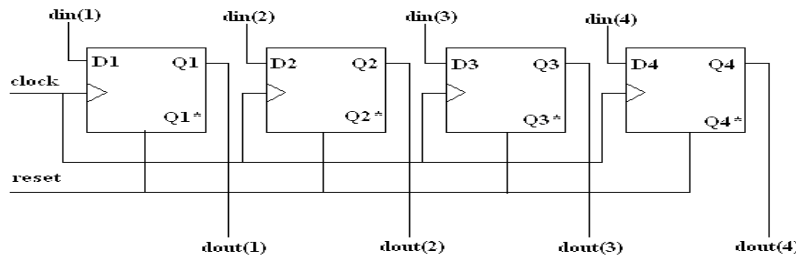


Fig. 7 Parallel In Parallel Out Shift Register (PIPO)

V.EXISTING DESIGNS

1. Conventional Double Edge Triggered D – Flip Flop : The DET flip flop given in [1] is shown in figure 1. This flip-flop is basically a Master Slave flip-flop structure and has two data paths. The upper data path consists of a Single Edge Triggered flip-flop (SETFF) implemented using transmission gates. It employs positive edge. The lower data path consists of a negative edge triggered flip-flop implemented using transmission gates. Both the data paths have feedback loops connected such that whenever the clock is stopped, the logic level at the output is retained. This flip flop has 26 transistors. In this 12 transistors are clocked transistors. The figure 1 shows a pair of parallel loops. When the clock pulse changes from low to high, the upper loop holds data and the down loop samples data. But when the clock pulse changes from high to low, the top loop switches to sample data and then the down loop switches to hold data.

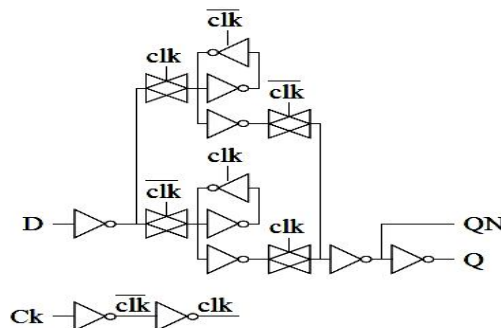


Fig. 8 Conventional Double Edge Triggered D – Flip Flop

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2. Existing design 1 and 2 : The concept of Tristate buffer is incorporated in the conventional design and two inverters are reduced and a new double edge triggered DFF is obtained. The diagrammatic description of this tristate buffer based double edge triggered DFF is clearly explained below as follows. This design altogether reduces four transistors but the number of clocked transistors remains the same. This design is further enhanced by eliminating the concept of tristate buffer. The circuit is redrawn as a normal double edge triggered DFF and is clearly explained below. The number of transistors required to perform the action is 22 here.

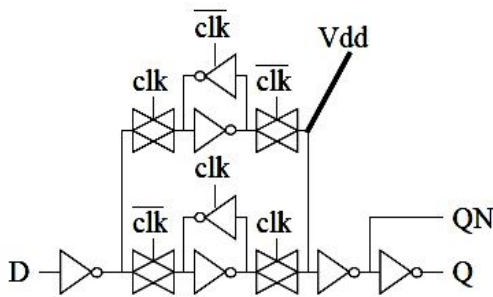


Fig. 9 Existing Design 1

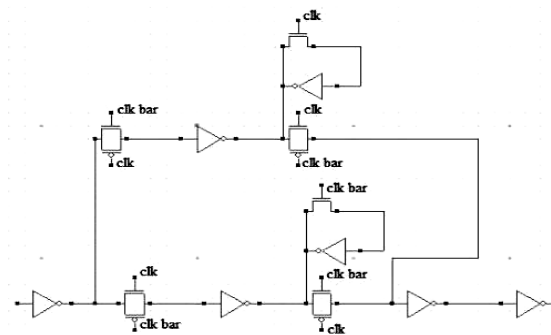


Fig. 10 Existing Design 2

VI. PROPOSED DESIGN

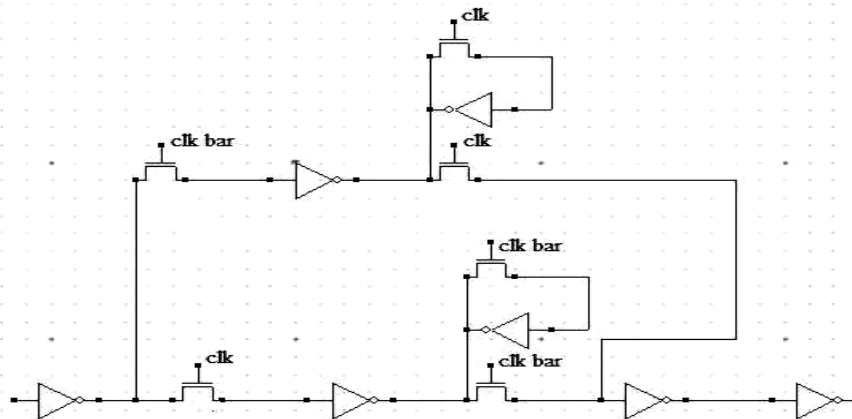


Fig. 11 Proposed Double Edge Triggered D – Flip Flop

The above described is the proposed design. The new design is proposed by replacing all the transmission gate by the n pass transistors in the Existing 2 design. This proper modelling does not affect the operation of the double edge triggering. The number of transistor is reduced to 18 where the clocked transistor are only 6 transistors involved here. So minimizing the number of clocked transistors actively reduces the power consumption and also the speed of the design got increased. Therefore all the performance parameters including Power consumption, Delay and area are enhanced and the design is best suitable for high speed and low power applications. All the shift registers are designed using this proposed and existing DFF's and the transient and performance analysis are compared.

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VII. TRANSIENT ANALYSIS

As explained above the Existing double edge triggered DFF, Proposed double edge triggered DFF and the existing and proposed DETFF based Shift Registers are designed in 16nm MOSFET technology. 16nm Predictive Technology Model (PTM MODEL) is used to design the 16 nm designs. The below shown transient analysis clearly explains about the inputs and outputs of all the designs

Technology	16nm cMOS
MOSFET MODEL	16nm cMOS PTM Model
Nominal conditions	$V_{dd} = 0.7 \text{ V}$, Temperature = 25°C
Clock frequency	1GHz
Tool used	Synopsys Hspice

Table. 1 Explanation of Specifications

The above mentioned table explains about the various parameters included in designing the DFF and shift registers.

1. Transient analysis of Existing and Proposed Double Edge Triggered D – Flip Flop

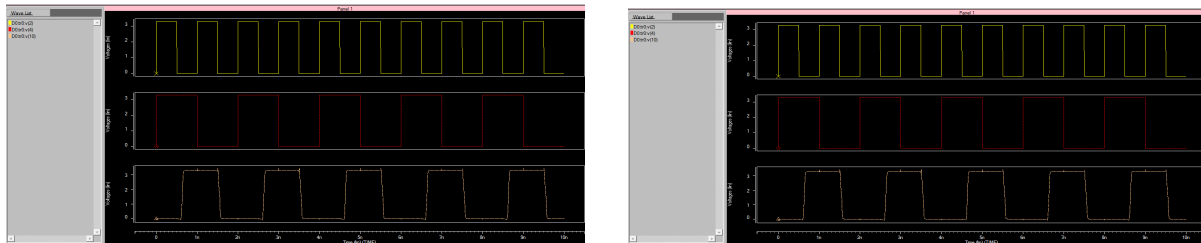


Fig. 12 Transient analysis of Existing and Proposed Double Edge Triggered D – Flip Flop

In the above mentioned diagram the first signal displays the clock signal, second one describes the input given and the last describes the delayed output.

2. Transient analysis of Existing and Proposed SISO shift register

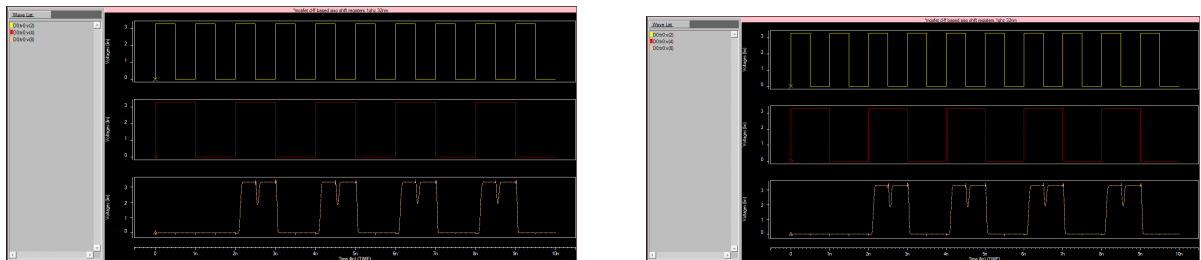


Fig. 13 Transient analysis of Existing and Proposed SISO shift register

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In the above mentioned diagram the first signal displays the clock signal, second one describes the input given and the last describes the serially shifted data signal.

3. Transient analysis of Existing and Proposed SIPO shift register

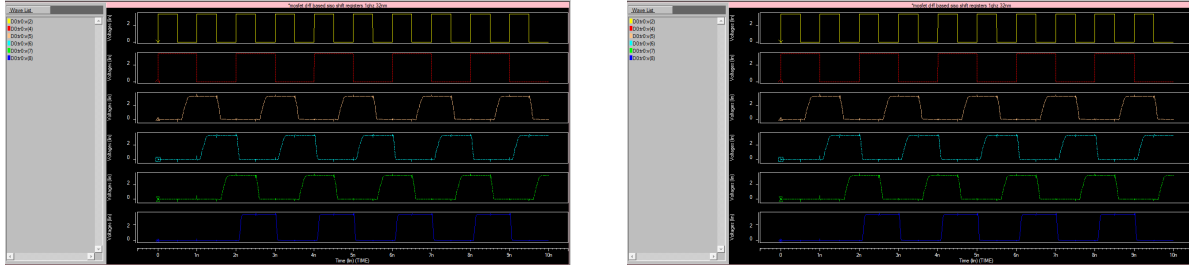


Fig. 14 Transient analysis of Existing and Proposed SIPO shift register

In the above mentioned diagram the first signal displays the clock signal, second one describes the input given and the last describes the parallel shifted data signal.

4. Transient analysis of Existing and Proposed PISO shift register

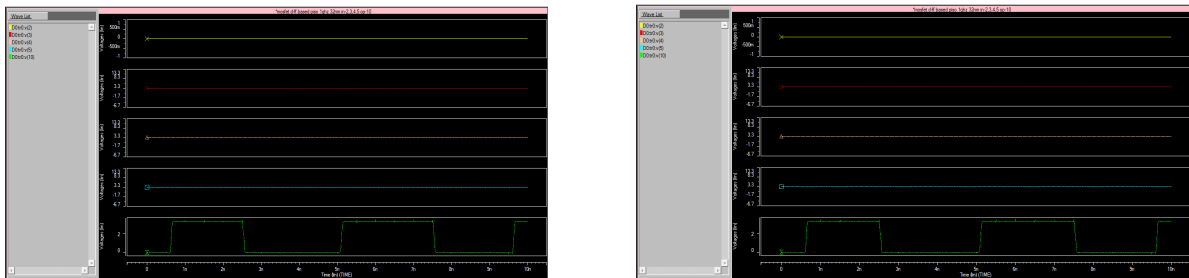


Fig. 15 Transient analysis of Existing and Proposed PISO shift register

In the above shown diagrammatic description, the first four signals represents the parallel inputs given to the design and the final signal represents the serially shifted output signal.

5. Transient analysis of Existing and Proposed PIPO shift register

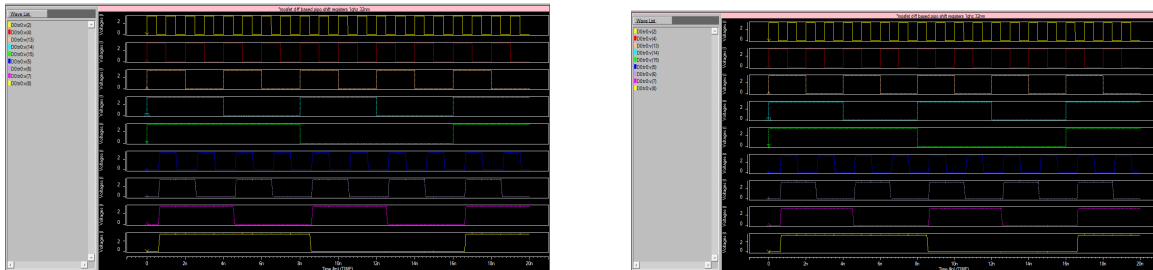


Fig. 16 Transient analysis of Existing and Proposed PIPO shift register



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VIII.PERFORMANCE ANALYSIS

Existing Design	Power	Delay	PDP	Proposed Design	Power	Delay	PDP
DFF	3.680e-04	15.032p	0.1146f	DFF	1.239e-04	11.418p	0.0516f
SISO	1.526e-03	3.0334n	126.09f	SISO	0.658e-03	3.0244n	62.574f
SIPO	1.526e-03	41.318p 1.0328n 2.0325n 3.0344n	1.717f 42.933f 84.49f 126.09f	SIPO	0.658e-03	21.258p 1.0240n 2.0243n 3.0244n	0.439f 21.186f 41.88f 62.57f
PISO	1.605e-03	39.742p	0.2234f	PISO	0.586e-03	32.8167p	0.00772f
PIPO	1.483e-03	1.0213n	14.788f	PIPO	0.748e-03	1.0135n	7.3874f

Table 2 : Performance of Existing and Proposed Designs

The above drawn table clearly explains the Power consumption, Delay and Power Delay Product of the existing and the proposed designs in 16nm MOSFET technology operated at a frequency of 1GHz in 0.7v.

IX.CONCLUSIONS

Thus the paper clearly describes the fundamentals of Flip Flops and shift registers. Double Edge Triggered Flip Flop Structures are clearly described. Conventional and Existing Double Edge Triggered Flip Flop Structures are clearly described. From the existing design a new Double Edge Triggered Flip Flop was proposed. For the enhanced functioning, circuits are designed in 16nm PTM MOSFET model. The performance parameters including Power consumption, Delay and Power Delay Product are analysed and compared. From the results obtained it's been evident that the Proposed Double Edge Triggered D – Flip Flop and DFF based Shift Registers are best suitable for low power and high speed real time applications.

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BIOGRAPHY



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