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Experimental Analysis of Single-Phase Non-Transformer Photovoltaic Inverter with Optimum Efficiency

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Abstract---This paper analyses a new transformer less, single-phase PV inverter topology generates no common-mode voltage, exhibits a high efficiency. Grid-connected PV systems include a line transformer in the power-conversion stage, for galvanic isolation between the grid and the PV system, thus providing personal protection. Furthermore, it strongly reduces the leakage currents. But the efficiency is largely decreased due to the power losses and the line transformer is large, heavy and expensive. In this paper, a new topology, based on the H-bridge with a new ac bypass circuit consisting of a diode rectifier and a switch with clamping to the dc midpoint, is proposed. The topology is simulated and experimentally validated, and a comparison with other existing topologies is performed. High conversion efficiency and low leakage current are demonstrated.

Key words: PV Inverter, H-bridge, HERIC Topology

I. INTRODUCTION

PHOTOVOLTAIC (PV) inverters become more and more widespread within both private and commercial circles. These grid-connected inverters convert the available direct current supplied by the PV panels and feed it into the utility grid. According to the latest report on installed PV power, during 2007, there has been a total of 2.25 GW of installed PV systems, out of which the majority (90%) has been installed in Germany, Spain, U.S., and Japan. At the end of 2007, the total installed PV capacity has reached 7.9 GW of which around 92% is grid Connected.

There are two main topology groups used in the case of grid-connected PV systems, namely, with and without galvanic isolation. Galvanic isolation can be on the dc side in the form of a high-frequency dc–dc transformer or on the grid side in the form of a big bulky ac transformer. Both of these solutions offer the safety and advantage of galvanic isolation, but the efficiency of the whole system is decreased due to power losses in these extra components. In case the transformer is omitted, the efficiency of the whole PV system can be increased with an extra 1%–2%. The most important advantages of transformer-less PV systems are higher efficiency and smaller size and weight compared to the PV systems that have galvanic isolation (either on the dc or ac side). Transformer-less PV inverters use different solutions to minimize the leakage ground current and improve the efficiency of the whole system, an issue that has previously been treated in many papers. In order to minimize the ground leakage current through the parasitic capacitance of the PV array, several techniques have been used.

II. COMMON-MODE CURRENTS IN TRANSFORMER-LESS PV SYSTEMS

When no transformer is used, a galvanic connection between the ground of the grid and the PV array exists. As a consequence a common-mode resonant circuit appears, consisting of the stray capacity between the PV modules and the ground, the dc and ac filter elements, and the grid impedance (Fig. 1). A varying common-mode voltage can excite this resonant circuit and generate a common-mode current. Due to the large surface of the PV generator, its stray capacity with respect to the ground reaches values that can be even higher than 200 nF/kWp in damp environments or on rainy days. These high values can generate ground currents with amplitudes well above the permissible levels, such as those concerning the standards. The currents can cause severe (conducted and radiated) electromagnetic interferences, distortion in the grid current and additional losses in the system. These leakage currents can be avoided, or at least limited, by including damping passive components in the resonant circuit. Obviously, additional losses will

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appear in the damping elements, thus decreasing the conversion stage efficiency. The use of conversion topologies with a constant common mode voltage is another option. The instantaneous common mode voltage Vcm in the full-bridge inverter of Fig. 1 can be calculated from the voltage of the two mid-points of legs, VAO and VBO as

$Vcm = (VAO + VBO)/2$..... (1)

To avoid leakage currents, the common-mode voltage must be kept constant during all commutation states, that is

$Vcm = VAO + VBO$

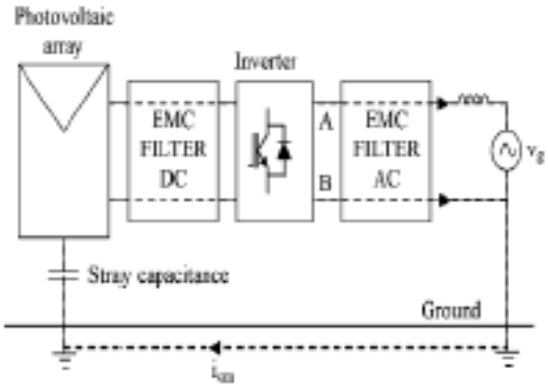

Fig.1 Common-modes currents in transformer-less conversion stage

In order to minimize the ground leakage current through the parasitic capacitance of the PV array, several techniques have been used.

One of them is to connect the midpoint of the dc-link capacitors to the neutral of the grid, like the half-bridge, neutral point clamped (NPC), or three-phase full bridge with a split capacitor topology, thereby continuously clamping the PV array to the neutral connector of the utility grid. Half-bridge and NPC type of converters have very high efficiency, above 97%, as shown in. Furthermore, the topology proposed in reduces the dc current injection, which is an important issue in the case of transformer-less topologies and is limited by different standards. The non-injection of dc current into the grid is topologically guaranteed by adding a second capacitive divider to which the neutral terminal of the grid is connected. An extra control loop is introduced that compensates for any dc current injection, by controlling the voltage of both capacitive dividers to be equal. A disadvantage of half-bridge and NPC type of converters is that, for single-phase grid connection, they need a 700-V dc link.

Another solution is to disconnect the PV array from the grid, in the case of H-bridge (HB) inverters, when the zero vectors is applied to the load (grid). This disconnection can be done either on the dc side of the inverter and H5 topology from Solar Technologies or on the ac side like the Highly Efficient and Reliable Inverter Concept HERIC)topology from Sunways.

In this paper, a new topology called HB zero-voltage state rectifier (HB-ZVR) is proposed where the midpoint of the dc link is clamped to the inverter only during the zero-state period by means of a diode rectifier and one switch. In Section II, a comparison of know transformer-less topology and the HB-ZVR is performed using simulation, focusing on the voltage to earth and ground leakage current. In Section III, experimental results are shown, confirming the simulations. Section IV presents the efficiency curve of the Compared topologies.

II. TRANSFORMER-LESS TOPOLOGY ANALYSIS

As discussed in previous above], the common-mode voltage generated by a topology and modulation strategy can greatly influence the ground leakage current that flows through the parasitic capacitance of the PV array. Generally, the utility grid does not influence the common-mode behaviour of the system, so it can be concluded that the generated common mode voltage of a certain inverter topology and modulation strategy can be shown using a simple resistor as

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load. Therefore, in the case of simulations, only a resistive load is used, and the common-mode voltage is measured between the dc+ terminal of the dc source and the grounded middle point of the resistor as shown in Fig. 2. In the following, simulation results obtained using Mat lab. Simulink with the PLECS toolbox are shown. The simulation step size is 0.1 μs, with an 8-kHz switching frequency.

Simulation parameters:

Lf = 1.8 mH filter inductance;

Cf = 2 μF filter capacitance;

R = 7.5 Ω load resistance;

*V*dc = 350 V input dc voltage;

*C*dc = 250 μF dc-link capacitance;

*C*G−PV = 100 nF parasitic capacitance of PV array;

*F*sw = 8 kHz switching frequency for all cases except that the switching frequency for unipolar pulse width modulation (PWM) has been chosen to be *F*sw = 4 kHz, so the output voltage of the inverter has the same frequency for all cases.

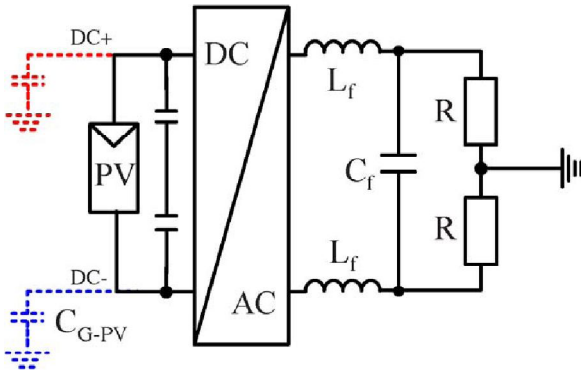

Fig.2. Test setup used for common-mode voltage measurement.

A. HALF BRIDGE TOPOLOGY WITH UNIPOLAR SWITCHING

Most single-phase HB inverters use unipolar switching in order to improve the injected current quality of the inverter, which is done by modulating the output voltage to have three levels with twice the switching frequency. Moreover, this type of modulation reduces the stress on the output filter and decreases the losses in the inverter. The positive active vector is applied to the load by turning on S1 and S4, as shown in Fig. 3.

The negative active vector is done similarly, but in this case, S2 and S3 are turned on.
As shown in Fig. 3, the zero-voltage state is achieved by short circuiting the output of the inverter for the case of the unipolar switching pattern. The waveforms for this case are detailed in Fig. 4, and it can be seen that the output voltage has three levels:

+V, 0, and −V due to the unipolar switching pattern. As shown in Fig. 6, in the case of a transformer-less PV system using this type of topology and modulation, the high frequency common-mode voltage, measured across *C*G−PV, will lead to a very high leakage ground current, making it unsafe and therefore not usable (recommended) for transformer-less PV applications.

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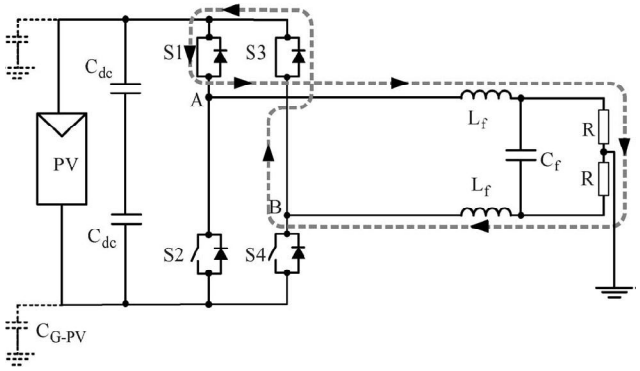

Fig. 3. HB-Unipolar topology: Zero vector applied to load, using S1 and S3 for positive voltage.

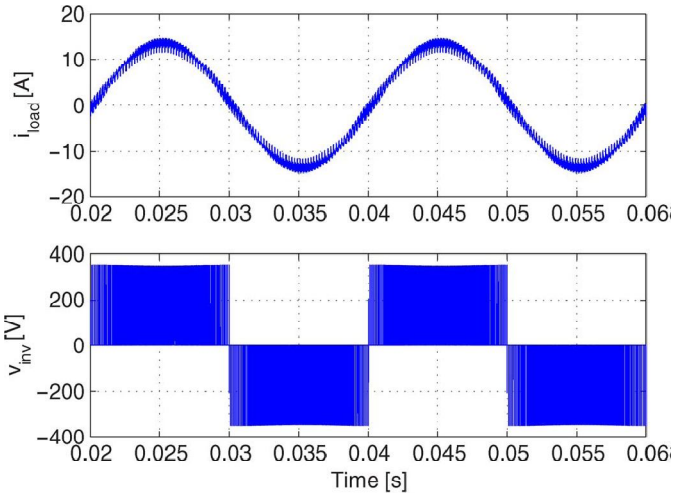

Fig.4. HB-Unip topology: Voltage to ground and ground leakage current

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B. HERIC TOPOLOGY

This topology, shown in Fig. 5, combines the advantages of the three-level output voltage of the unipolar modulation with the reduced common-mode voltage, as in the case of bipolar modulation. This way, the efficiency of the inverter is increased, without compromising the common-mode behaviour of the whole system. The zero-voltage state is realized using a bidirectional switch shown with a gray background in Fig.5.

This bidirectional switch is made up of two insulated-gate bipolar transistors (IGBTs) and two diodes (S5 and S6). During the positive half wave of the load (grid) voltage, S6 is switched on and is used during the freewheeling period of S1 and S4. On the other hand, during the negative half-wave, S5 is switched on and is used during the freewheeling period of S2 and S3. This way, using S5 or S6 as shown in Fig. 6, the zero-voltage state is realized by short-circuiting the output of the inverter, during which period the PV is separated from the grid, because S1–S4 or S2–S3 are turned off.

As shown in Fig. 7, the output voltage and the load current ripple is very small, although, in this case, the frequency of the current is equal to the switching frequency.

As shown in Fig.8, the inverter generates no common-mode voltage; therefore, the leakage current through the parasitic capacitance of the PV would be very small.

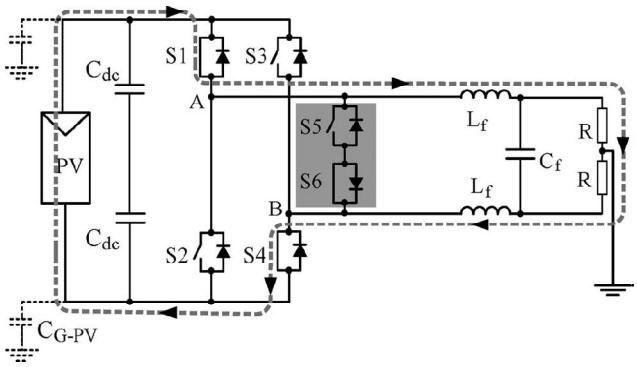

Fig. 5. HERIC topology: Active vector applied to load, using S1 and S4 during positive half-wave.

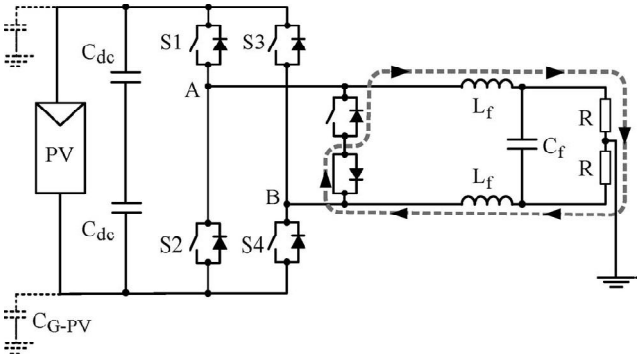

Fig.6. HERIC topology: Zero vector applied to load, using S6 during positive half-wave.

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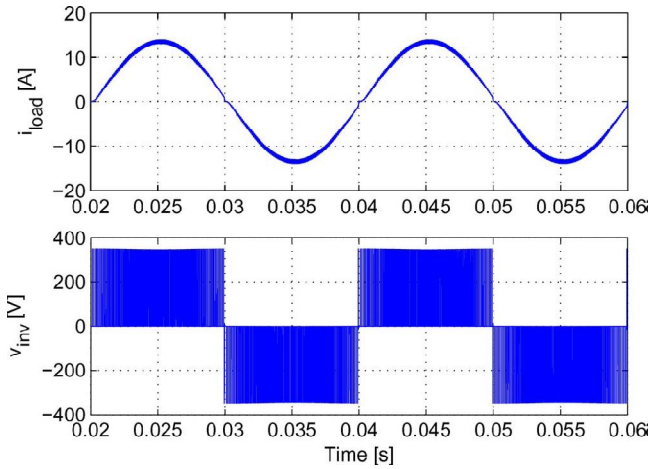

Fig. 7. HERIC topology: Load current and inverter output voltage.

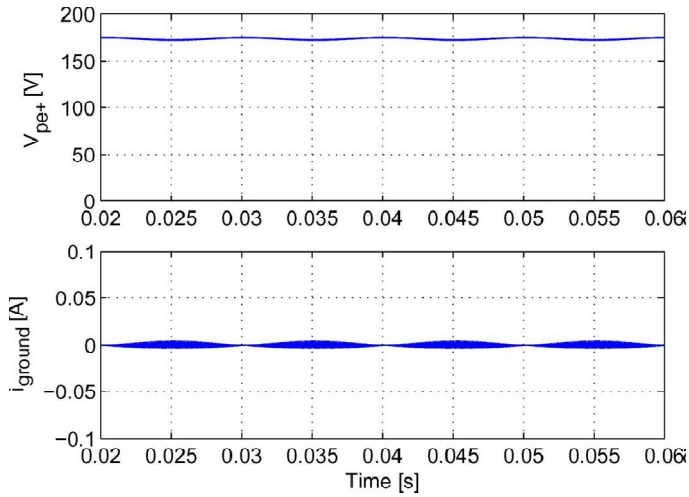

Fig. 8. HERIC topology: Voltage to ground and ground leakage current.

C. PROPOSED TOPOLOGY (HB-ZVR)

Another solution for generating the zero-voltage state can be done using a bidirectional switch made of one IGBT and one Diode Bridge. The topology is detailed in Fig. 9, showing the bidirectional switch as an auxiliary component with a gray background. This bidirectional switch is clamped to the midpoint of the dc-link capacitors in order to fix the potential of the PV array also during the zero-voltage vector when S1–S4 and S2–S3 are open. An extra diode is used to protect from short-circuiting the lower dc-link capacitor. During the positive half-wave, S1 and S4 are used to generate the active state, supplying a positive voltage to the load, as shown in Fig. 9. The zero-voltage state is achieved by turning on S5 when S1 and S4 are turned off, as shown in Fig. 10. The gate signal for S5 will be the complementary gate signal of S1 and S4, with a small dead time to avoid short-circuiting the input capacitor.

By using S5, it is possible for the grid current to flow in both directions; this way, the inverter can also feed reactive power to the grid, if necessary.

During the negative half-wave of the load voltage, S2 and S3 are used to generate the active vector and S5 is controlled using the complementary signal of S2 and S3 and generates the zero voltage state, by short circuiting the outputs of the inverter and clamping them to the midpoint of the dc-link.

During the dead time, between the active state and the zero state, there is a short period when the freewheeling current finds its path through the anti parallel diodes to the input capacitor while all the switches are turned off. This is shown in Fig. 11 and leads to higher losses, compared to the HERIC topology, where the freewheeling current finds its path through the bidirectional switch, either through S5 or S6, depending on the sign of the current.

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As shown in Fig. 10, the output voltage of the inverter has three levels, taking into account the freewheeling part during dead time. In this case also, the load current ripple is very small and the frequency is equal to the switching frequency. To show that this topology does not generate a varying common-mode voltage, *V*cm has been calculated for the switching states regarding the positive, zero, and negative vectors

$$V_{cm} = \frac{V_{AQ} + V_{BQ}}{2} \quad (1)$$

$$\text{Positive}: V_{AQ} = V_{dc};\ V_{BQ} = 0 \Rightarrow V_{cm} = \frac{V_{dc}}{2} \quad (2)$$

$$\text{Zero}: V_{AQ} = \frac{V_{dc}}{2};\ V_{BQ} = \frac{V_{dc}}{2} \Rightarrow V_{cm} = \frac{V_{dc}}{2} \quad (3)$$

$$\text{Negative}: V_{AQ} = 0;\ V_{BQ} = V_{dc} \Rightarrow V_{cm} = \frac{V_{dc}}{2}. \quad (4)$$

As detailed by (1)–(4), the common-mode voltage is constant for all switching states of the converter. Therefore, the leakage current through the parasitic capacitance of the PV would be very small, as shown in Fig. 15.

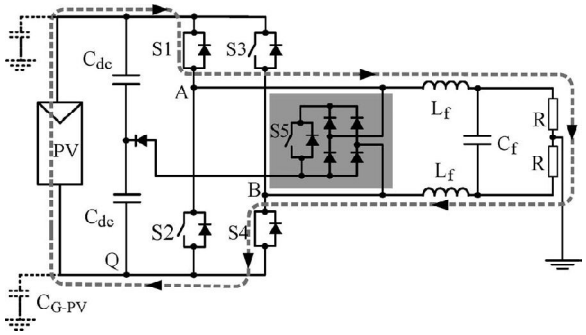

Fig. 9. HB-ZVR topology: Active vector applied to load, using S1 and S4 during positive half-wave.

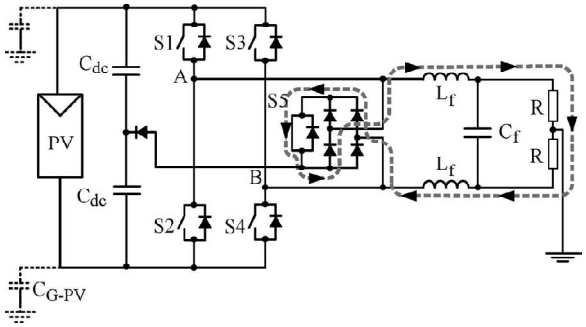

Fig. 12. HB-ZVR topology: Zero vector applied to load, using S5 during positive half-wave.

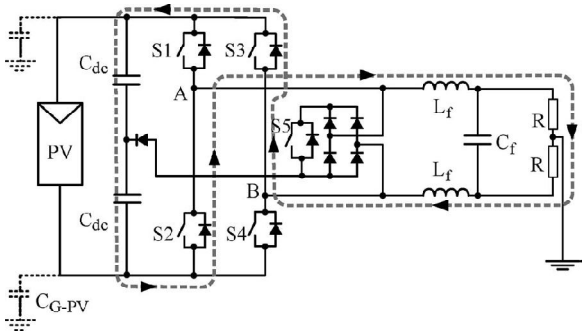

Fig. 10. HB-ZVR topology: Dead time between turnoff of S1 and S4 and turn-on of S5 during positive half-wave.

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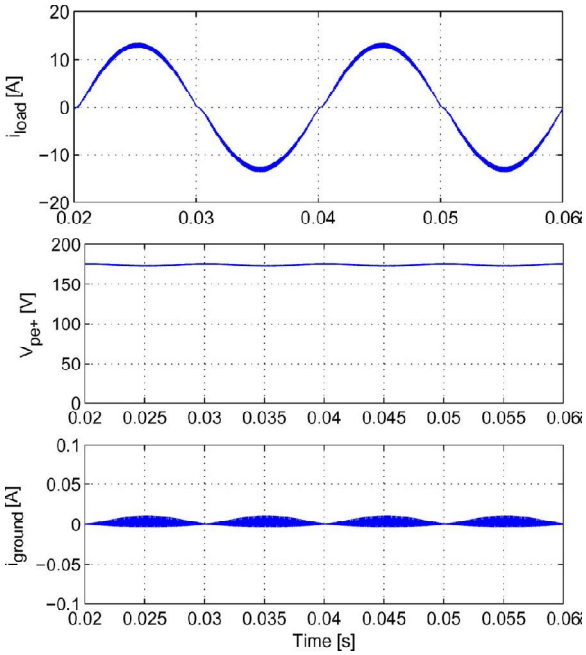

Fig. 11. HB-ZVR topology: Voltage to ground and ground leakage current.

II. EXPERIMENTAL RESULTS

TABLE I
SIMULATION AND EXPERIMENTAL PARAMETERS.

Normal Grid Voltage	$V_g = 230\ V$
Normal Grid Frequency	$\omega_0 = 2\pi \times 50\ rad/s$
Grid Impedance	$L_g = 2\ mH,\ R_g = 0.04\ \Omega$
Rated Power	$P_n = 1\ kW$
Switching Frequency	$f_{sw} = 10\ kHz$
LCL-Filter	$L_{if} = 3.6\ mH,\ L_{gf} = 708\ \mu H,\ C_f = 2.35\ \mu F$
Sag Generator	$R_S = 19.3\ \Omega,\ R_L = 19.9\ \Omega$
PI based Power Controllers	$k_{pp} = 1.5,\ k_{ip} = 52$ of $G_P(s)$ - active power $k_{pq} = 1,\ k_{iq} = 50$ of $G_Q(s)$ - reactive power
PR+HC Current Controller	$k_p = 20,\ k_r = 2000,\ k_{rh1,5,7} = 5000$

To compare the behaviour of the different inverters, all three topologies have been tested using the same components. PM75DSA120 Intelligent Power Modules with maximum ratings of 1200 V and 75 A from Mitsubishi as IGBTs and DSEP 30-06BR with maximum ratings of 600 V and 30 A as diodes from IXYS have been used in the diode bridge of the proposed topology.

The modular based setup shown in Fig. 12 makes it possible to test the different topologies, namely, full bridge with bipolar or unipolar modulation, the HERIC topology, and the proposed HB-ZVR, using the same components.

A. HALF-BRIDGE WITH UNIPOLAR SWITCHING

The main advantage of the HB inverter with unipolar switching is that the output voltage has three levels and the frequency of the output voltage is the double of the switching frequency, thereby increasing the efficiency of the inverter and decreasing the size of the output filter. However, the major drawback of this topology is the high-frequency common-mode voltage, which makes it unsuitable to be used for transformer-less PV systems.

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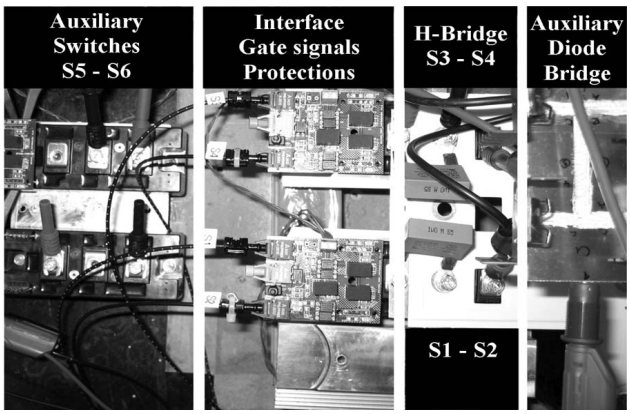

Fig. 12. Experimental setup: Modular solution.

As shown in Fig. 3, the unipolar PWM strategy used in the case of the HB topology generates a high-frequency common mode voltage, measured between the dc+ terminal of the dc-link and ground. This common-mode voltage has very high amplitudes both at dc and the switching frequency. In addition, a low-frequency component can be seen on the measured voltage, which is caused by the 100-Hz single-phase power variation.
This varying common-mode voltage generates a very high ground leakage current that is only limited by the parasitic capacitance of the PV array.

B. HERIC (Experiment)

As presented in the simulation results (Section II-B), the HERIC topology generates a constant common-mode voltage, by disconnecting the PV from the load (grid) during the state of the zero vector, when the output of the inverter is short-circuited. This separation assures that the common-mode voltage acting on the parasitic capacitance of the PV array does not change in time, therefore keeping the leakage current at very low values, well below the standard requirement of 300 mA, given by VDE-0126-1-1, the German standard for grid-connected PV systems.

C. HB-ZVR (Experiment)

As mentioned in Section II-C, the HB-ZVR topology generates the zero-voltage vector in a similar way as the HERIC topology, but using another solution for the bidirectional switch configuration. Of course, the common-mode behavior of the topology is similar, as was the case of the HERIC topology. As shown in Fig. 13, the output voltage seems to vary for different values of source voltage obtained from the photovoltaic array.

Table-II

Inverter Input Pulse Delay Time (μs)	Output Current(mA)	Output Voltage (V)
0.256	0.58	78.94
0.361	0.456	75.86
0.485	0.32	73.67
0.67	0.221	71.12
0.78	0.11	70.02

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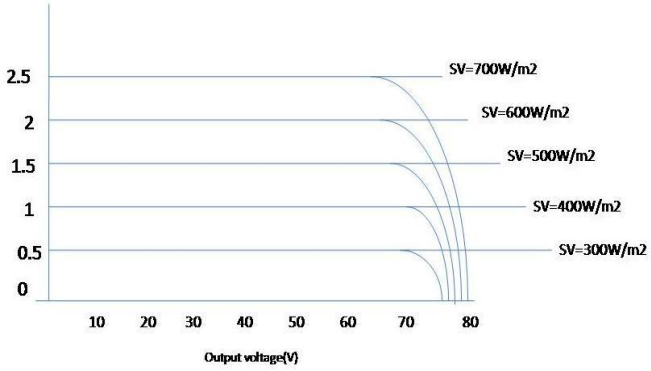

Fig. 13. Output voltage variation with output current for various values of solar voltage

Table-III

Inverter Input Pulse Delay Time (μs)	Output Current (mA)	Output Voltage (V)
0.256	0.58	78.94
0.361	0.456	75.86
0.485	0.32	73.67
0.67	0.221	71.12
0.78	0.11	70.02

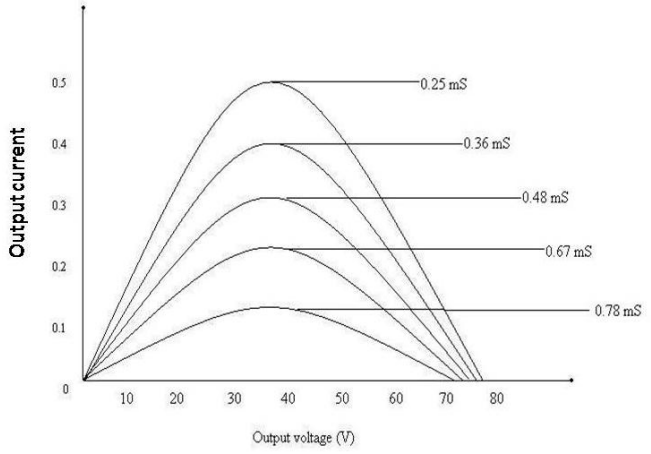

Fig. 14. The variation of output voltage for a constant source voltage.

IV. EFFICIENCY

In the case of a single-phase grid connection, the required minimum dc-link input voltage of the inverter, in the European case, has to be at least 350 V; otherwise, a boost stage is required. The tests have been done with an input voltage of *V*dc = 350 V.

The HERIC topology, as also suggested by its name, has very high conversion efficiency throughout the whole working range and has the best efficiency within the compared topologies, as detailed in Table I and also shown in Fig. 16. The HB-ZVR topology has a slightly lower efficiency, due to the fact that the bidirectional switch is controlled with the switching frequency, while in the case of the HERIC topology, the bidirectional switch is only switched with the mains frequency. With a maximum efficiency of 94.88%, it is a very attractive solution for transformer-less PV

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systems. The HB-Bipolar topology has the lowest efficiency, due to them high losses as a result of the two-level voltage output.

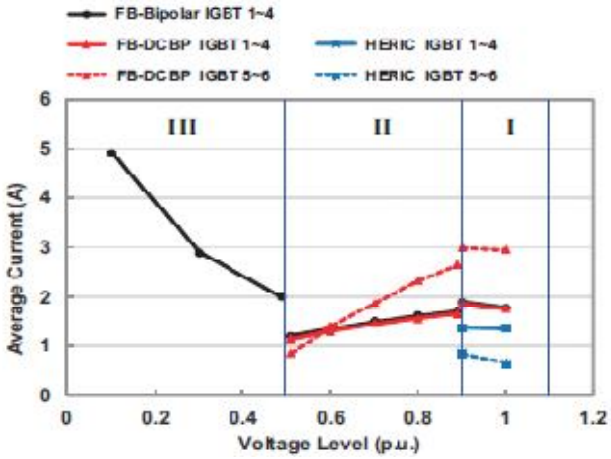

Table-IV

EFFICIENCY AT DIFFERENT INPUT POWER WITH V_{dc} = 350 V

	500W	1000W	1500W	2000W	2500W	2800W
HB-Bip	84,37%	90,27%	92,49%	93,66%	94,28%	94,51%
HERIC	93,45%	94,71%	95,31%	95,6%	95,85%	95,94%
HB-ZVR	90,38%	92,79%	93,78%	94,39%	94,76%	94,88%

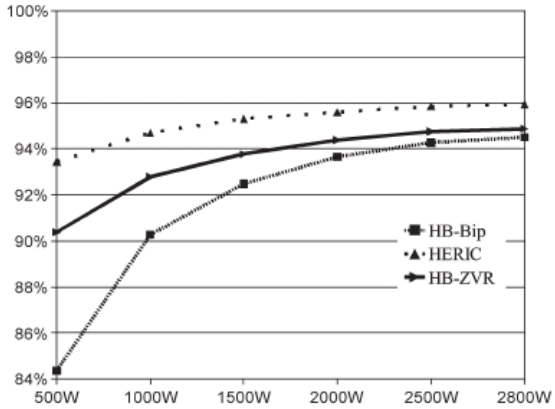

Fig.16. Efficiency curve of the different topologies (Vdc = 350 V).

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V. SIMULATION WAVEFORM

Output voltage vs currents when Solar voltage=300

Table-III

Solar voltage	output voltage (V)	output current (mA)
300	10	0.51
300	20	0.51
300	30	0.51
300	40	0.51
300	50	0.45
300	60	0.33
300	70	0.22
300	72	0.05

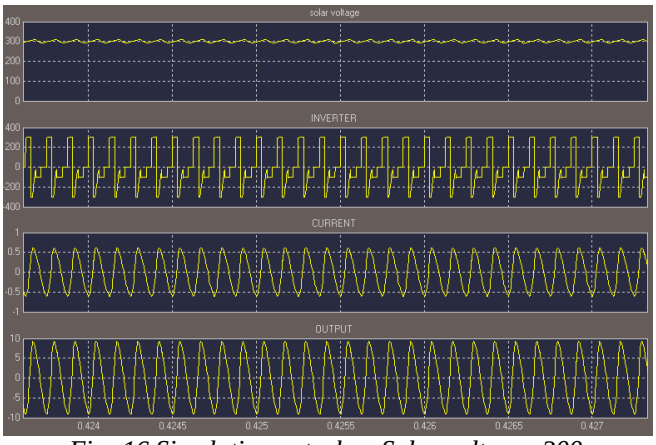

Fig: 16 Simulation out when Solar voltage=300

VI. CONCLUSION

This Non transformer inverters offer a better efficiency, compared to those inverters that have a galvanic isolation. On the other hand, in case the transformer is omitted, the generated common-mode behavior of the inverter topology greatly influences the ground leakage current through the parasitic capacitance of the PV.

Bipolar PWM generates a constant common-mode voltage, but the efficiency of the converter is low, due to the two level output voltage.

By using unipolar PWM modulation, the output of the converter will have three levels, but in this case, the generated common-mode voltage will have high-frequency components, which will lead to very high ground leakage currents.

In this paper we have verified a non transformer topology and given an alternative solution for the bidirectional switch, used to generate the zero-voltage state. The constant common-mode voltage of the HB-ZVR topology and its high efficiency make it an attractive solution for non transformer PV applications.

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