ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 2, Issue 10, October 2013

INTENSIFYING REDUNDANT TECHNIQUE FOR EXTENUATION OF SINGLE EVENT UPSET SENSITIVITY

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ABSTRACT: To detect and correct the errors in the Flow diagram of all digital systems using RAPTOR.By analysing the characteristics of PAD and structured flowchart, and a structure identification and coding algorithm are put forward for structured flow diagram and PAD. Finally a integrated development platform is developed using such algorithms, including flowchart modelling, code automatic generation Fault tolerance technique using TMR for exposure and expulsion the soft errors in the digital systems. Faults are detected and eliminated without interrupting the normal functioning of the circuit. Single point of failure, is eliminated and implemented as a fault tolerant using a Triple Modular Redundancy (TMR). Conventional lockstep scheme uses duplication with comparison (DWC), the presence of fault is detected, but it fails to indicate the location of fault which is overcome in enriched lockstep by triple modular redundancy (TMR). TMR technique incorporates both transient and permanent faults. The new intensifying lockstep scheme requires significantly shorter recovery time than conventional lock step. It uses significantly less number of slices.

Keywords*:* Structured Flow chart, Fault tolerance, Single-Event Upset (SEU), Triple Modular Redundancy (TMR),problem analysis diagram, integrated development platform.

I.INTRODUCTION

Flow chart describes the control logic of a program by top-down process. For PAD (problem analysis diagram),it has the capability of top-down and left-right. So we can say if flowchart is a one-dimension chart, then PAD is a two-dimensional chart[1]. The basic idea of redundancy is to implemented multiple copies of the same circuit, and compare the outputs of each circuits. Disparity in these outputs indicates the occurrence of an error. Redundancy technique can be implemented at various levels such as circuits, systems etc. This process of switching is a simple process when both the designs meet the system restrictions identically [2]. Logic paths in between the flip-flops are composed of hard-wired, non-reconfigurable gates. Hence they are immune to SEUs. A fully fault tolerant system has the ability to detect and then corrects the hardware occurrence and return the system to its normal functionality.

An optimal design will minimize the amount of extra logic required to detect and then correct the occurrence of the fault An extreme temperature change is one of the reasons in which fault tolerance is necessary for devices operating in harsh operating environments, as found, for example, in space and military applications[13][6]. Faults are separated into two categories: Permanent and Transient [8]. Permanent faults that exist in logic circuits are normally identified during offline testing by the manufacturer of the IC, so the transient fault is of major concern after a chip is in the hands of the consumer. The ability to simulate the occurrence of a transient fault in the VHDL description of a system is extremely important to verify the performance of an on-line testable system.

In this paper section II focus on single-event upsets (SEU) and types of upsets. Then SEU mitigation techniques were discussed. In section III proposed method IV, the experimental & results are discussed V. Finally, the paper was concluded in section

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II SINGLE EVENT UPSET MITIGATION TECHNIQUES

It is a process of applying design techniques to strengthen the functional integrity of the circuit, and protect it from the effect of any Single Event Upset. Fault-tolerant methods [6], [8] used to mitigate logic errors in FPGA based on redundancy technique are as follows. **RAPTOR** for detect & correct the error in the flow diagram of digital systems. **Duplication with Comparison (DWC)** for detecting faults and **Triple Modular Redundancy (TMR)** with majority voter for masking fault.

❖ RAPTOR Tool using DWC Technique for testing the Flow Chart

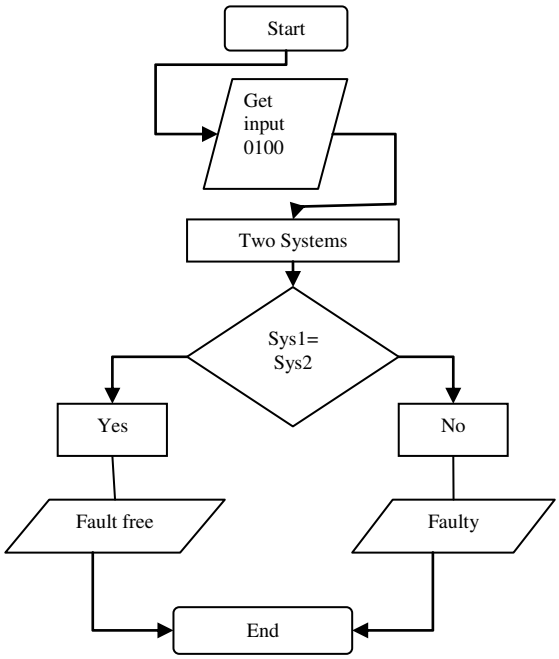
RAPTOR Tool is used to verify the DWCflow chart, each symbols are checked whether its suitable or not thenThis tool is used to all the digital circuits. This step is very important in testing field. its beginning step of testing. To detect and correct the errors in the Flow diagram of all digital systems using RAPTOR. By analyzing the characteristics of PAD and structured flowchart, and a structure identification and coding algorithm are put forward for structured flow diagram and PAD. Finally a integrated development platform is developed using such algorithms, including flowchart modeling, code automatic generation

ALGORITHM

****The following steps are first step in testing****

- Start the system design.
- Give input to the circuits (Both the circuits are accept same input value).
- Check both the circuit outputs; if output is mismatching its Faulty else fault free.
- This Flow Diagram is draw by RAPTOR Tool.
- Simulate the flow chart & evaluate each symbol.
- Run the flow chart.

FLOW CHART-DWC



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ISSN (Online): 2278 – 8875

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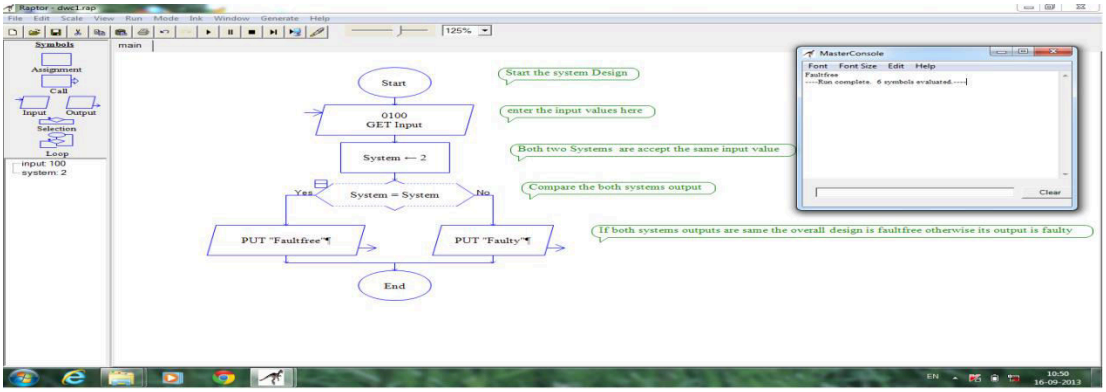
✓ **Result of Duplication with Comparison Flow Chart**



Design the system for Duplication with Comparison

Duplication with Comparison (DWC) is a detecting technique, in which the circuit to be protected is replicated twice and the results produced by the original circuit and the outputs of replicated circuits are compared to detect faults is given in figure 1. The implementation of DWC at processor level, supported by Xilinx ISE.

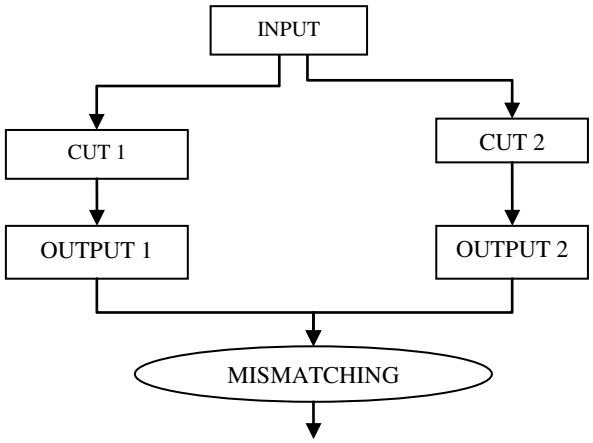


Figure 1 Duplication with Comparison (DWC)

Two identical circuits CUT1 and CUT2 receive the same inputs and simultaneously execute the same instructions, their results are compared step by- step at each clock cycle. Circuit CUT2 generates the reference results to be compared against those of CUT1 that provides the system output. Basically, DWC is able to detect but not to correct errors and also fails to indicate the fault location, since it cannot point out the faulty circuit. However, it could be capable to tolerate temporary faults, provided that it is supported by some re-execution procedure. In case of FPGA implementation, the system needs also to be reconfigured to recover correct functionalities.

III TRIPLE MODULAR REDUNDANCY TECHNIQUE

Triple Modular Redundancy (TMR) is the most reliable safeguard for total device failure as it rapidly detects and corrects SEUs.Three copies of the same circuit are connected to a "majority voter" which is used to obtain the fault free output.It operates withthe main aim of removing all single points of failure from the circuit. Each set of the triplicated circuit has its own set of inputs, to avoid errors occurring due to propagation of wrong inputs.

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❖ **RAPTOR Tool using TMR Technique for testing the Flow Chart**

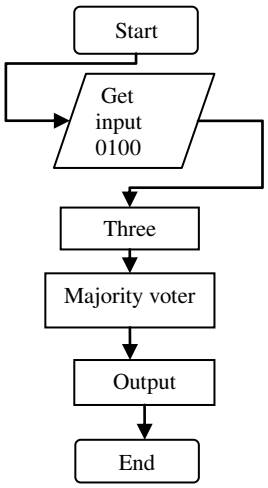
RAPTOR Tool is used to verify the TMR flow chart, each symbols are checked whether its suitable or not thenThis tool is used to all the digital circuits. This step is very important in testing field. its beginning step of testing. To detect and correct the errors in the Flow diagram of all digital systems using RAPTOR. By analyzing the characteristics of PAD and structured flowchart, and a structure identification and coding algorithm are put forward for structured flow diagram and PAD. Finally a integrated development platform is developed using such algorithms, including flowchart modeling, code automatic generation.

ALGORITHM -TMR

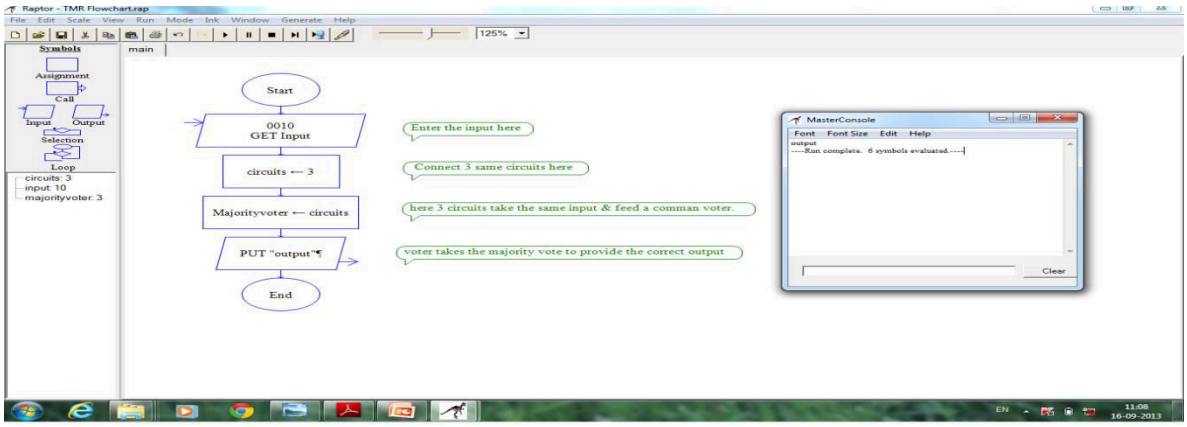
****The following steps are first process in testing****

- Start the system design.
- Give input to the circuits (All three circuits are accept same input value and feed a common voter).
- The Voter takes a majority vote to provide the correct output.
- This Flow Diagram is draw by RAPTOR Tool.
- Simulate the flow chart & evaluate each symbol.
- Run the flow chart

FLOW CHART-TMR



✓ **Result of Triple Modular Redundant Technique Flow Chart**



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❖ **Design the System for Triple Modular Redundancy Technique**

Triple Modular Redundancy (TMR) is the most reliable safeguard for total device failure as it rapidly detects and corrects SEUs[10], [11], [12].Three copies of the same circuit are connected to a "majority voter" which is used to obtain the fault free output is shown in figure 2. This method works as long as all the faults are confined to one of the redundant blocks. The latency will be increased because of the voter in the circuit's critical path.

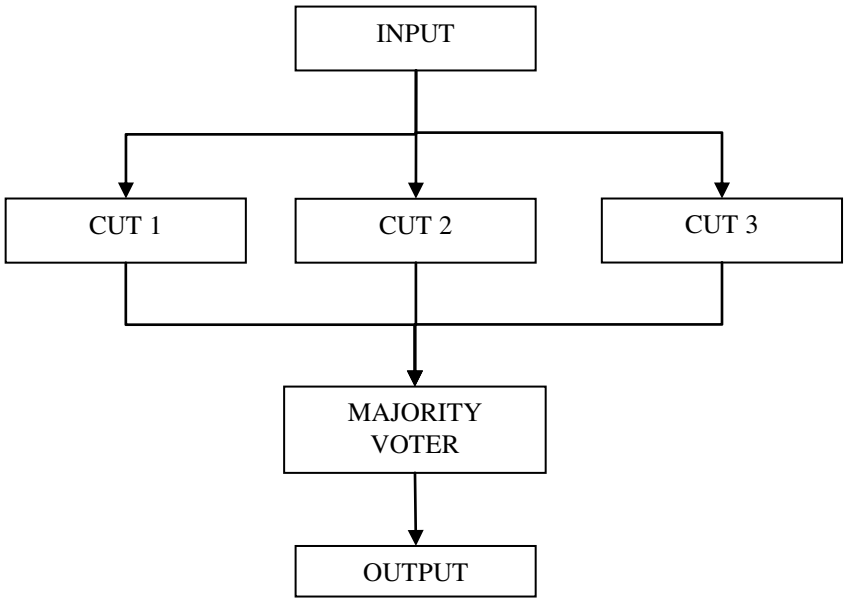

Fig 2 Triple Modular Redundancy (TMR)

TMR has a capability to protect both sequential and combinational circuits. A more efficient implementation of the TMR is focused in the sensitive logic, for example the memory cells to be protecting again SEU . It operates withthe main aim of removing all single points of failure from the circuit. Each set of the triplicated circuit has its own set of inputs, to avoid errors occurring due to propagation of wrong inputs.

The block diagram of the TMR adder circuit

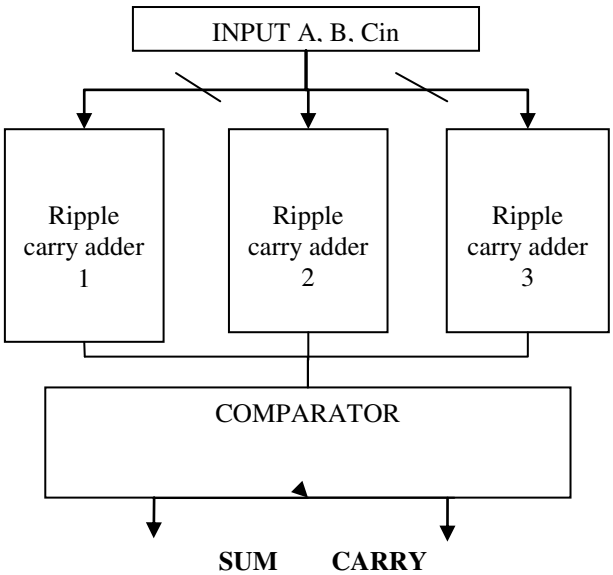

Figure 3 TMR adder circuit using ripple carry

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The triple modular redundant ripple carry adder (TMR-RCA) is used as the reference circuit. This adder is the simplest approach for both detecting and correcting faults. using the ripple carry adders is shown in Figure 3. The technique involved in information redundancy includes the use of error-correcting codes. Fault occur in any one of the adder is compared with the fault-free adders, in order to indicate the faulty one.
TMR has a capability to protect both sequential and combinational circuits. A more efficient implementation of the TMR is focused in the sensitive logic, for example the memory cells to be protecting again SEU is shown in figure 4. It operates with the main aim of removing all single points of failure from the circuit. Each set of the triplicated circuit has its own set of inputs, to avoid errors occurring due to propagation of wrong inputs.

Enhanced Lockstep Architecture

The basic lockstep scheme [7] uses the realization of DWC at the processor level. Unfortunately, it can only detect errors without indicating the faulty module. In order to alleviate this limitation, the new Enhanced Lockstep scheme is shown in Figure 3, which provided with the mean to identify the faulty circuit. It allows continuing the execution with the remaining fault-free circuit.
This technique involves with the operation of two identical circuits with synchronized clocking. A mismatching between the output values of the circuit indicates the occurrence of SEU. Recovery actions such as reinitializing and switching to safe mode are implemented. Figure 7 shows the architecture of the fault-tolerant system, whose two main blocks are Enhanced Lockstep scheme and the fault-tolerant (FT) Configuration Engine. Error Correcting Code (ECC) is used for detection and identification of single and double-bit errors in the given data.
The reset input may be tied to logic 0 for free-running SEU detection and correction in the circuit that do not require access to the configuration memory during normal operation.[12] Two identical circuits CUT1and CUT2 and are the most essential part of the Enhanced Lockstep scheme. Their outputs are identical during fault-free functioning, any mismatching indicating error(s). If there is an error indication, the output signals of the PLB bus and the peripheral outputs are compared by the Comparator/Multiplexer (COMP MUX). If there is a mismatching occurs between any of the two circuits, a signal will be generated. When an error is detected between the circuits, since all the resources of two circuits are blended together it, there is no possibility of differentiating the faulty circuit.

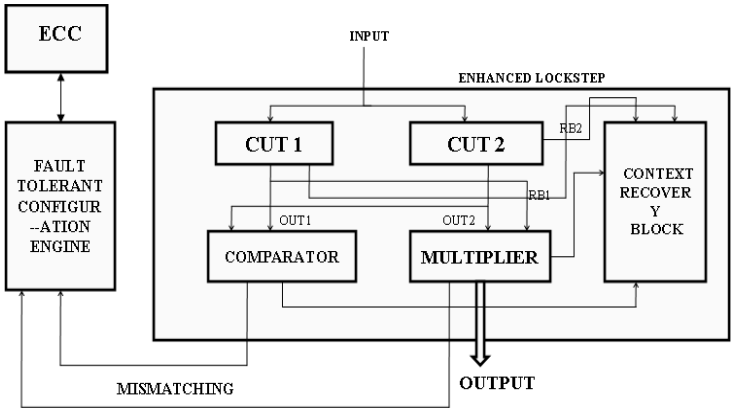

Fig 4 Enhanced Lock Step Scheme

In order to distinguish the faulty circuit, two blocks are used are the Comparator (COMP) and Multiplier (MUX). COMP that indicates any mismatch between the outputs Out1 and Out2 of CUT1 and CUT2 (containing the PLB and final output signals). [14] And the MUX, which connects one of the circuit to the system output, so that if one of them is reported to be faulty, the other is switched on. The switching is an atomic operation executed in one clock cycle. Once the error is localized by the FT Configuration Engine the affected processor is reconfigured to eliminate its configuration upset. Synchronization process is used for the newly reconfigured one to the same state as the correct one, thus enabling them to continue executingthe same task in lockstep again. The recovery process of the Enhanced Lockstep scheme is handled by the Context Recovery Block (CRB).

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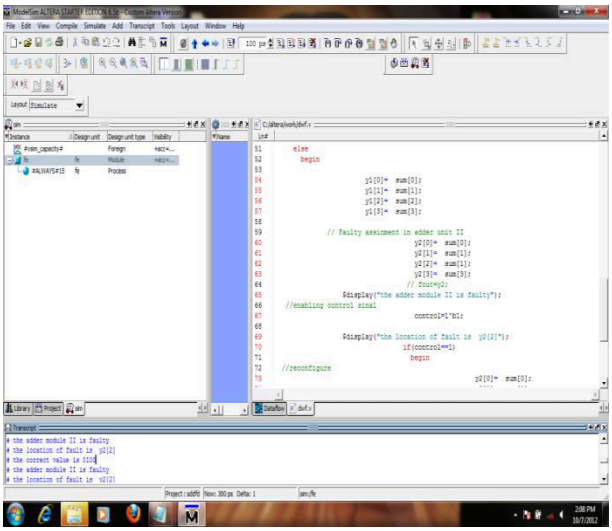
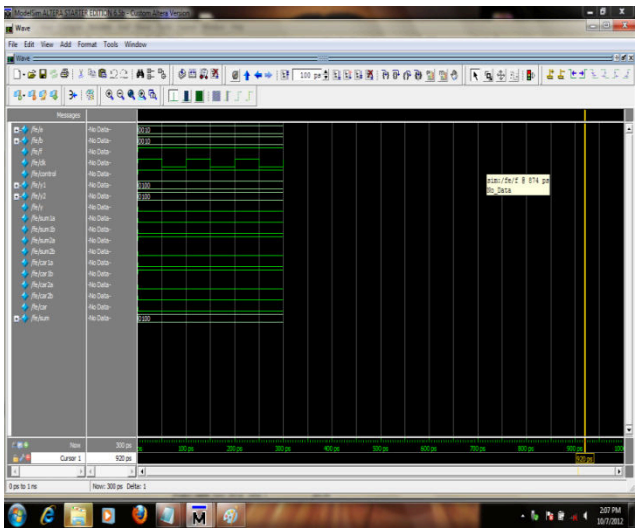
IV RESULTS& IMPLEMENTATION

✓ **Ripple Carry Adder verilog codingOutput Waveform**





✓ **Table 1 Enhanced lockstep scheme**

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	17	960	1%
Number of 4 input LUTs	31	1920	1%
Number of bonded IOBs	50	66	75%
Number of GCLKs	1	24	4%

The performance analysis of enhanced lockstep scheme technique based on time, area, numbers of slices used are given in the tables. Table 1 shows the device utilization and the simulation time s 15.925.

V CONCLUSION

Conventional lockstep scheme uses duplication with comparison (DWC), the presence of fault is detected, but it fails to indicate the location of fault which is overcome in enriched lockstep by triple modular redundancy (TMR).Enhanced lockstep scheme uses triple modular redundancy (TMR) as a fault tolerant to detect and eliminate transient faults. It reduces both area and time consumption considerably. The errors can be reduced, performing the previous technological considerations, to sets of bits which are candidate to flip at the same time. The performance and efficiency of the circuit can be improved and the simulation time is reduced.

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BIOGRAPHY

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